

74AXP1G97

Low-power configurable multiple function gate

Rev. 1 — 25 June 2013

Preliminary data sheet

1. General description

The 74AXP1G97 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer. All inputs can be connected directly to V_{CC} or GND. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.7 V to 2.75 V. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.7 V to 2.75 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-12A.01 (wide range: 0.8 V to 1.3 V)
 - ◆ JESD8-12A.01 (normal range: 1.1 V to 1.3 V)
 - ◆ JESD8-11A.01 (1.4 V to 1.6 V)
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A.01 (2.3 V to 2.7 V)
- ESD protection:
 - ◆ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 0.6 \mu\text{A}$ (85 °C maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 2.75 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C



3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|-------|---|---------|
| | Temperature range | Name | Description | |
| 74AXP1G97GM | -40 °C to +85 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm | SOT886 |
| 74AXP1G97GN | -40 °C to +85 °C | XSON6 | extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm | SOT1115 |
| 74AXP1G97GS | -40 °C to +85 °C | XSON6 | extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm | SOT1202 |

4. Marking

Table 2. Marking

| Type number | Marking code ^[1] |
|-------------|-----------------------------|
| 74AXP1G97GM | RV |
| 74AXP1G97GN | RV |
| 74AXP1G97GS | RV |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

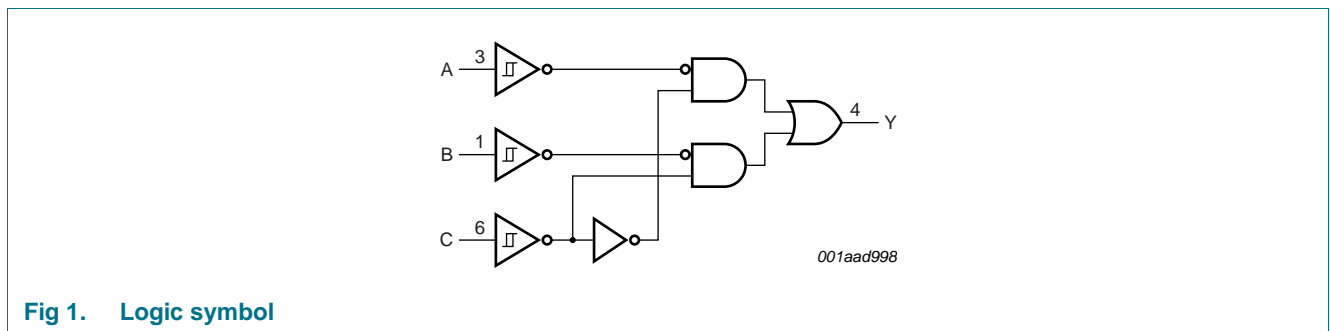
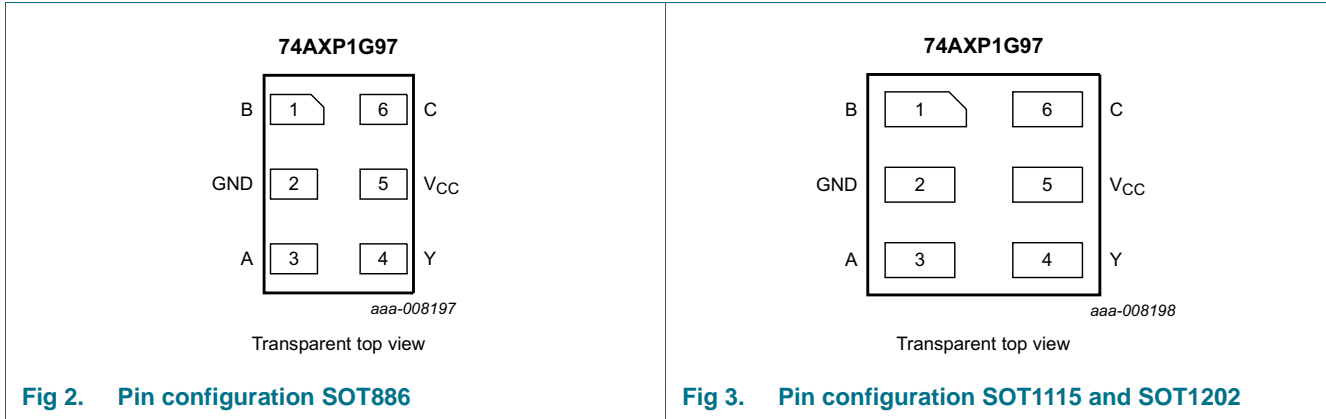


Fig 1. Logic symbol

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------|
| B | 1 | data input |
| GND | 2 | ground (0 V) |
| A | 3 | data input |
| Y | 4 | data output |
| V _{CC} | 5 | supply voltage |
| C | 6 | data input |

7. Functional description

Table 4. Function table^[1]

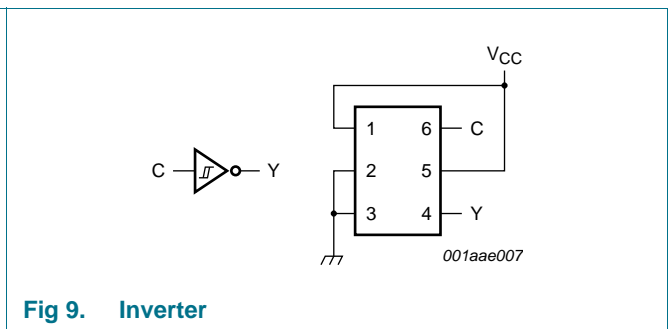
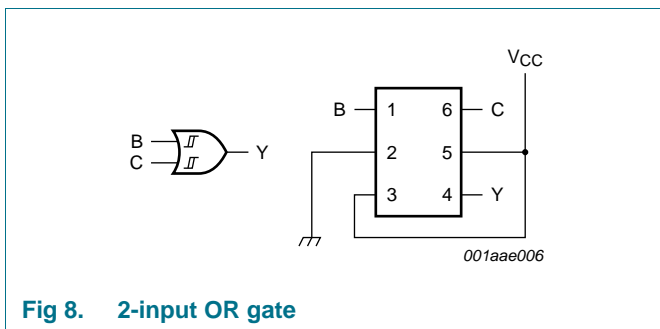
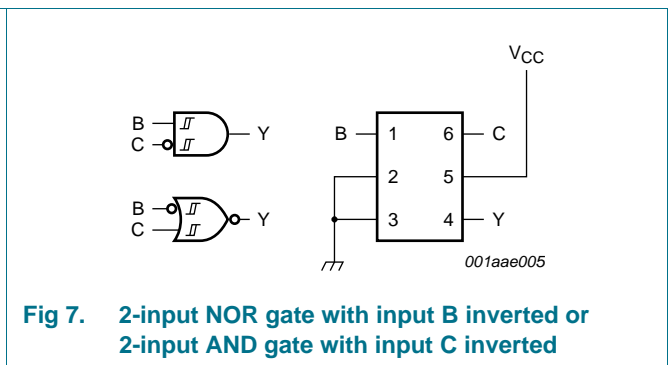
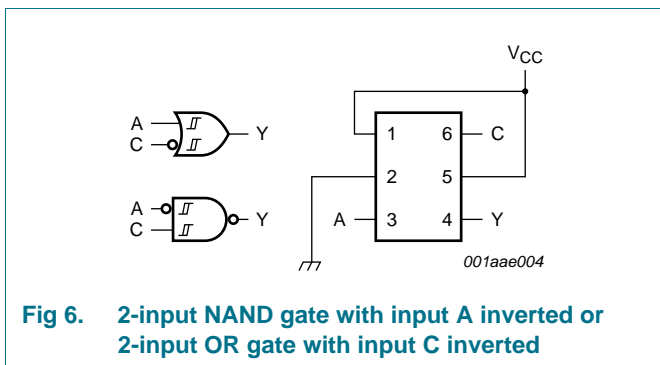
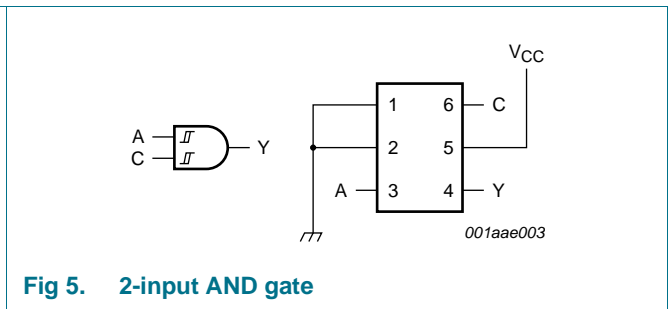
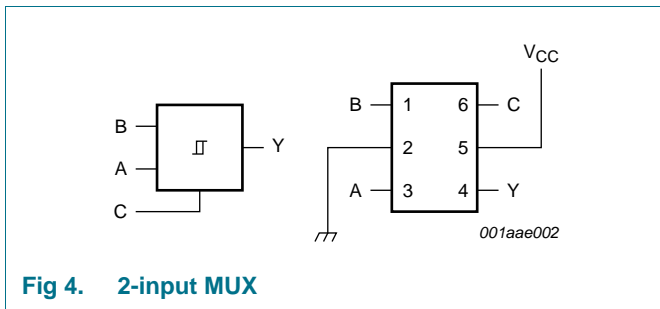
| Input | | | Output |
|-------|---|---|--------|
| C | B | A | Y |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |

[1] H = HIGH voltage level;
L = LOW voltage level.

7.1 Logic configurations

Table 5. Function selection table

| Logic function | Figure |
|--------------------------------------|-------------------------------|
| 2-input MUX | see Figure 4 |
| 2-input AND | see Figure 5 |
| 2-input OR with one input inverted | see Figure 6 |
| 2-input NAND with one input inverted | see Figure 6 |
| 2-input AND with one input inverted | see Figure 7 |
| 2-input NOR with one input inverted | see Figure 7 |
| 2-input OR | see Figure 8 |
| Inverter | see Figure 9 |
| Buffer | see Figure 10 |



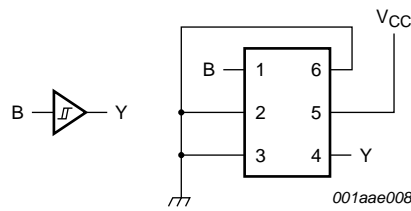


Fig 10. Buffer

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|----------|----------|------|
| V_{CC} | supply voltage | | -0.5 | 3.3 | V |
| I_{IK} | input clamping current | $V_I < 0\text{ V}$ | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | 3.3 | V |
| I_{OK} | output clamping current | $V_O < 0\text{ V}$ | -50 | - | mA |
| V_O | output voltage | Active mode and Power-down mode | [1] -0.5 | 3.3 | V |
| I_O | output current | $V_O = 0\text{ V to }V_{CC}$ | - | ± 20 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C to }+85\text{ °C}$ | - | 250 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------|--|-----|----------|------|
| V_{CC} | supply voltage | | 0.7 | 2.75 | V |
| V_I | input voltage | | 0 | 2.75 | V |
| V_O | output voltage | Active mode | 0 | V_{CC} | V |
| | | Power-down mode; $V_{CC} = 0\text{ V}$ | 0 | 2.75 | V |
| T_{amb} | ambient temperature | | -40 | +85 | °C |

10. Static characteristics

Table 8. Static characteristics

$V_{CC} = 0.7\text{ V}$ to 2.75 V , unless otherwise specified; At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$ | | | | Unit | |
|------------------|--------------------------------------|--|--|-----------|--------------|--------------|---------------|---------------|
| | | | Min | Typ 25 °C | Max 25 °C | Max 85 °C | | |
| V_{T+} | positive-going threshold voltage | see Figure 11 and Figure 12 $V_{CC} = 0.75\text{ V}$ to 0.85 V | $0.35V_{CC}$ | - | $0.75V_{CC}$ | $0.75V_{CC}$ | V | |
| | | $V_{CC} = 1.1\text{ V}$ to 1.95 V | $0.4V_{CC}$ | - | $0.7V_{CC}$ | $0.7V_{CC}$ | V | |
| | | $V_{CC} = 2.3\text{ V}$ to 2.7 V | 0.9 | - | 1.7 | 1.7 | V | |
| V_{T-} | negative-going threshold voltage | see Figure 11 and Figure 12 $V_{CC} = 0.75\text{ V}$ to 0.85 V | $0.25V_{CC}$ | - | $0.65V_{CC}$ | $0.65V_{CC}$ | V | |
| | | $V_{CC} = 1.1\text{ V}$ to 1.95 V | $0.3V_{CC}$ | - | $0.6V_{CC}$ | $0.6V_{CC}$ | V | |
| | | $V_{CC} = 2.3\text{ V}$ to 2.7 V | 0.7 | - | 1.5 | 1.5 | V | |
| V_H | hysteresis voltage | see Figure 11 and Figure 12 $V_{CC} = 0.75\text{ V}$ to 0.85 V | $0.1V_{CC}$ | - | $0.5V_{CC}$ | $0.5V_{CC}$ | V | |
| | | $V_{CC} = 1.1\text{ V}$ to 1.95 V | $0.1V_{CC}$ | - | $0.4V_{CC}$ | $0.4V_{CC}$ | V | |
| | | $V_{CC} = 2.3\text{ V}$ to 2.7 V | 0.2 | - | 1.0 | 1.0 | V | |
| V_{OH} | HIGH-level output voltage | $I_O = -20\text{ }\mu\text{A}$ | $V_{CC}-0.05$ | - | - | - | V | |
| | | $I_O = -100\text{ }\mu\text{A}$; $V_{CC} = 0.75\text{ V}$ | $V_{CC}-0.1$ | - | - | - | V | |
| | | $I_O = -2\text{ mA}$; $V_{CC} = 1.1\text{ V}$ | 0.825 | - | - | - | V | |
| | | $I_O = -3\text{ mA}$; $V_{CC} = 1.4\text{ V}$ | 1.05 | - | - | - | V | |
| | | $I_O = -4.5\text{ mA}$; $V_{CC} = 1.65\text{ V}$ | 1.2 | - | - | - | V | |
| | | $I_O = -8\text{ mA}$; $V_{CC} = 2.3\text{ V}$ | 1.7 | - | - | - | V | |
| V_{OL} | LOW-level output voltage | $I_O = 20\text{ }\mu\text{A}$ | - | - | 0.05 | 0.05 | V | |
| | | $I_O = 100\text{ }\mu\text{A}$; $V_{CC} = 0.75\text{ V}$ | - | - | 0.1 | 0.1 | V | |
| | | $I_O = 2\text{ mA}$; $V_{CC} = 1.1\text{ V}$ | - | - | 0.275 | 0.275 | V | |
| | | $I_O = 3\text{ mA}$; $V_{CC} = 1.4\text{ V}$ | - | - | 0.35 | 0.35 | V | |
| | | $I_O = 4.5\text{ mA}$; $V_{CC} = 1.65\text{ V}$ | - | - | 0.45 | 0.45 | V | |
| | | $I_O = 8\text{ mA}$; $V_{CC} = 2.3\text{ V}$ | - | - | 0.7 | 0.7 | V | |
| I_I | input leakage current | $V_I = 0\text{ V}$ to 2.75 V ; $V_{CC} = 0\text{ V}$ to 2.75 V | [1] | - | <tbid> | ± 0.1 | ± 0.5 | μA |
| I_{OFF} | power-off leakage current | V_I or $V_O = 0\text{ V}$ to 2.75 V ; $V_{CC} = 0\text{ V}$ | - | - | ± 0.1 | ± 0.5 | μA | |
| ΔI_{OFF} | additional power-off leakage current | V_I or $V_O = 0\text{ V}$ to 2.75 V ; $V_{CC} = 0\text{ V}$ to 0.2 V | - | - | ± 0.1 | ± 0.5 | μA | |
| I_{CC} | supply current | $V_I = 0\text{ V}$ or V_{CC} ; $I_O = 0\text{ A}$ | [1] | - | <tbid> | 0.3 | 0.6 | μA |
| ΔI_{CC} | additional supply current | $V_I = V_{CC} - 0.5\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 2.5\text{ V}$ | - | - | 100 | 150 | μA | |

[1] All typical values are measured at $V_{CC} = 1.2\text{ V}$.

10.1 Waveform transfer characteristics

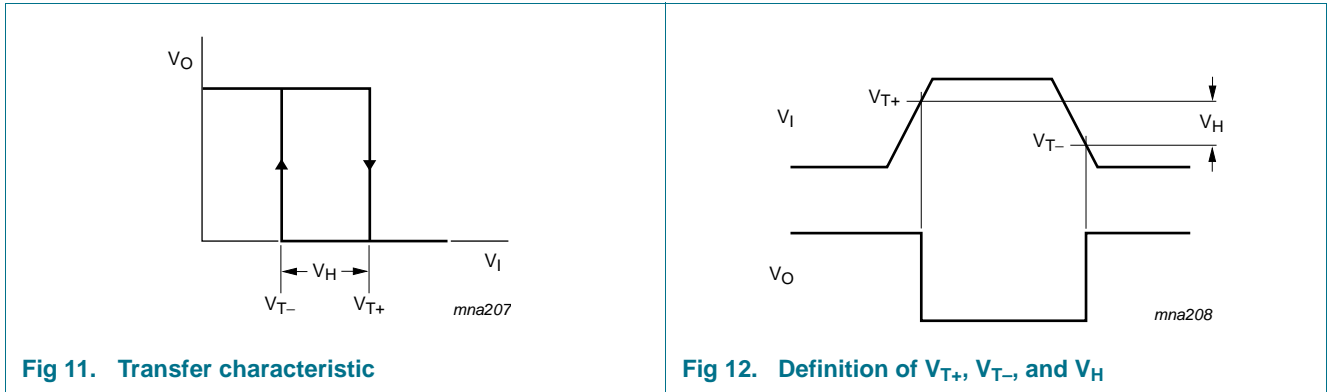


Fig 11. Transfer characteristic

Fig 12. Definition of V_{T+} , V_{T-} , and V_H

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 19.

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | Unit |
|-----------------|--------------------|--|--------------------------|--------------------|-----|-------------------------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{pd} | propagation delay | A, B and C to Y; see Figure 13 [2][3] | | | | | | |
| | | V _{CC} = 0.75 V to 0.85 V | 3.6 | 12.3 | 41 | 3.2 | 95 | ns |
| | | V _{CC} = 1.1 V to 1.3 V | 2.4 | 4.5 | 7.5 | 2.1 | 8.0 | ns |
| | | V _{CC} = 1.4 V to 1.6 V | 2.0 | 3.4 | 5.2 | 1.6 | 5.6 | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.7 | 2.8 | 4.3 | 1.4 | 4.6 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.4 | 2.2 | 3.4 | 1.1 | 3.6 | ns |
| t _t | transition time | V _{CC} = 2.7 V; see Figure 13 [4] | 1.0 | - | - | - | - | ns |
| C _I | input capacitance | V _I = 0 V or V _{CC} ; V _{CC} = 0 V to 2.75 V | - | 1 | - | - | - | pF |
| C _O | output capacitance | V _O = 0 V; V _{CC} = 0 V | - | 2 | - | - | - | pF |

Table 9. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 19](#).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | Unit |
|-----------------|-------------------------------|--|--------------------------|--------------------|-----|-------------------------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = 0 V to V _{CC} ^[5] | | | | | | |
| | | V _{CC} = 0.75 V to 0.85 V | - | 3.0 | - | - | - | pF |
| | | V _{CC} = 1.1 V to 1.3 V | - | 2.9 | - | - | - | pF |
| | | V _{CC} = 1.4 V to 1.6 V | - | 3.0 | - | - | - | pF |
| | | V _{CC} = 1.65 V to 1.95 V | - | 3.2 | - | - | - | pF |
| | | V _{CC} = 2.3 V to 2.7 V | - | 3.7 | - | - | - | pF |

- [1] All typical values are measured at nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] For additional propagation delay values at different load capacitances see [Figure 14](#) to [Figure 18](#).
- [4] t_t is the same as t_{THL} and t_{TLH}.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11.1 Waveforms and graphs

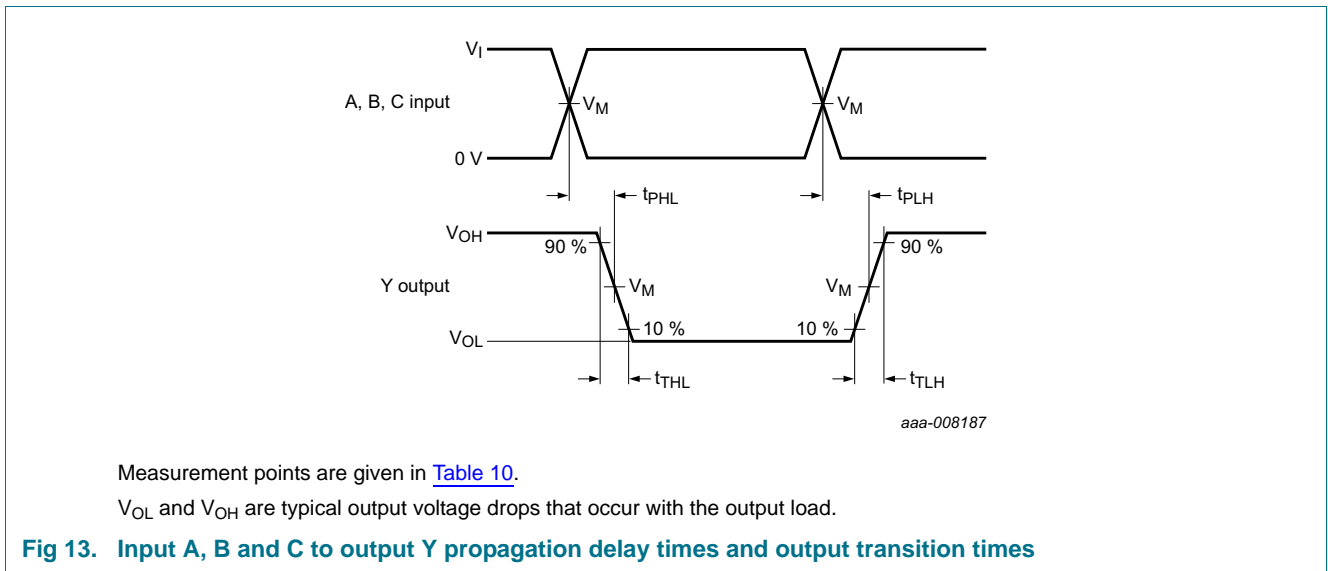
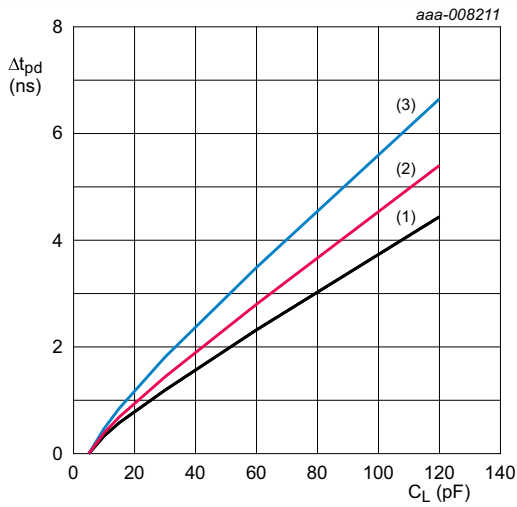


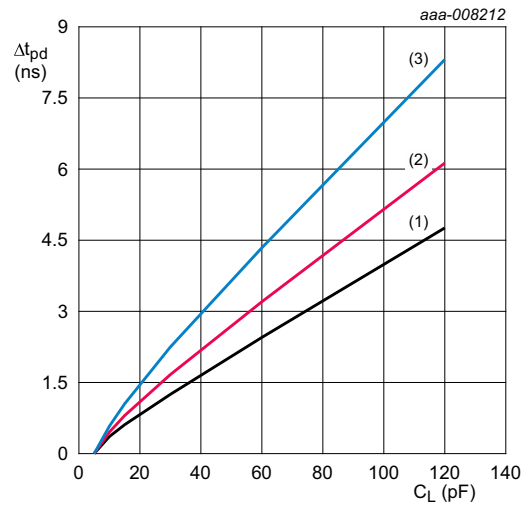
Table 10. Measurement points

| Supply voltage | Output | Input | | |
|------------------|-----------------------|-----------------------|-----------------|---------------------------------|
| V _{CC} | V _M | V _M | V _I | t _r = t _f |
| 0.75 V to 2.75 V | 0.5 × V _{CC} | 0.5 × V _{CC} | V _{CC} | ≤ 3.0 ns |



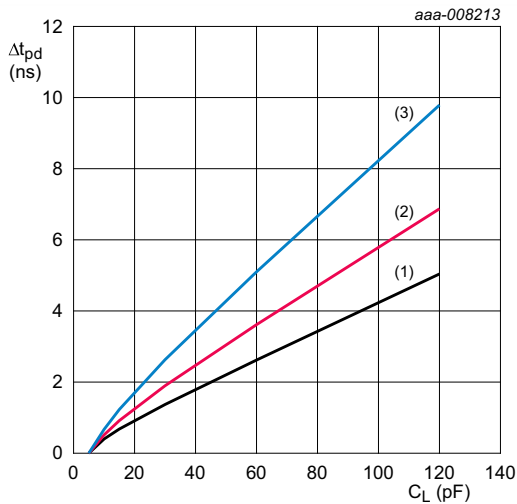
- $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.
- (1) Minimum: $V_{CC} = 2.3\text{ V}$ to 2.7 V
 - (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 2.5\text{ V}$
 - (3) Maximum: $V_{CC} = 2.3\text{ V}$ to 2.7 V

Fig 14. Additional propagation delay versus load capacitance



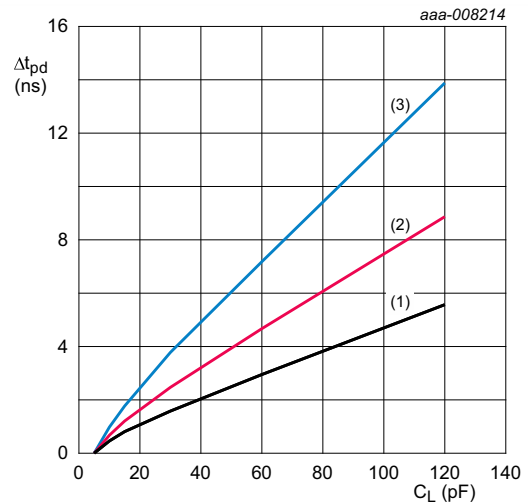
- $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.
- (1) Minimum: $V_{CC} = 1.65\text{ V}$ to 1.95 V
 - (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 1.8\text{ V}$
 - (3) Maximum: $V_{CC} = 1.65\text{ V}$ to 1.95 V

Fig 15. Additional propagation delay versus load capacitance



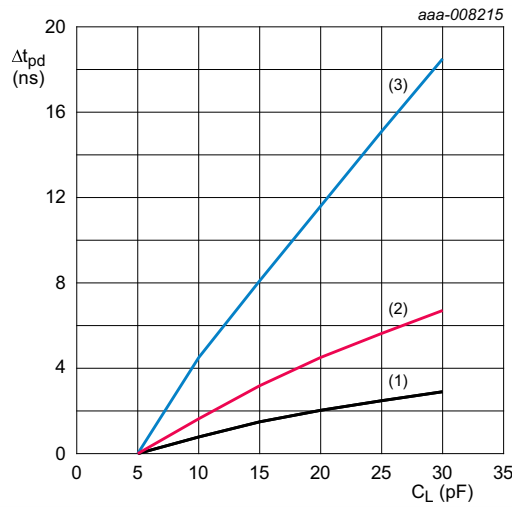
- $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.
- (1) Minimum: $V_{CC} = 1.4\text{ V}$ to 1.6 V
 - (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 1.5\text{ V}$
 - (3) Maximum: $V_{CC} = 1.4\text{ V}$ to 1.6 V

Fig 16. Additional propagation delay versus load capacitance



- $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.
- (1) Minimum: $V_{CC} = 1.1\text{ V}$ to 1.3 V
 - (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 1.2\text{ V}$
 - (3) Maximum: $V_{CC} = 1.1\text{ V}$ to 1.3 V

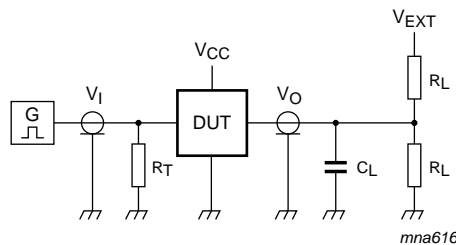
Fig 17. Additional propagation delay versus load capacitance



$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

- (1) Minimum: $V_{CC} = 0.75\text{ V}$ to 0.85 V
- (2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 0.8\text{ V}$
- (3) Maximum: $V_{CC} = 0.75\text{ V}$ to 0.85 V

Fig 18. Additional propagation delay versus load capacitance



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 19. Test circuit for measuring switching times

Table 11. Test data

| Supply voltage | Load | | V_{EXT} | | |
|------------------|-------|---------------|--------------------|--------------------|--------------------|
| V_{CC} | C_L | R_L | t_{PLH}, t_{PHL} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 0.75 V to 2.75 V | 5 pF | 10 k Ω | 0 V | 0 V | $2 \times V_{CC}$ |

12. Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

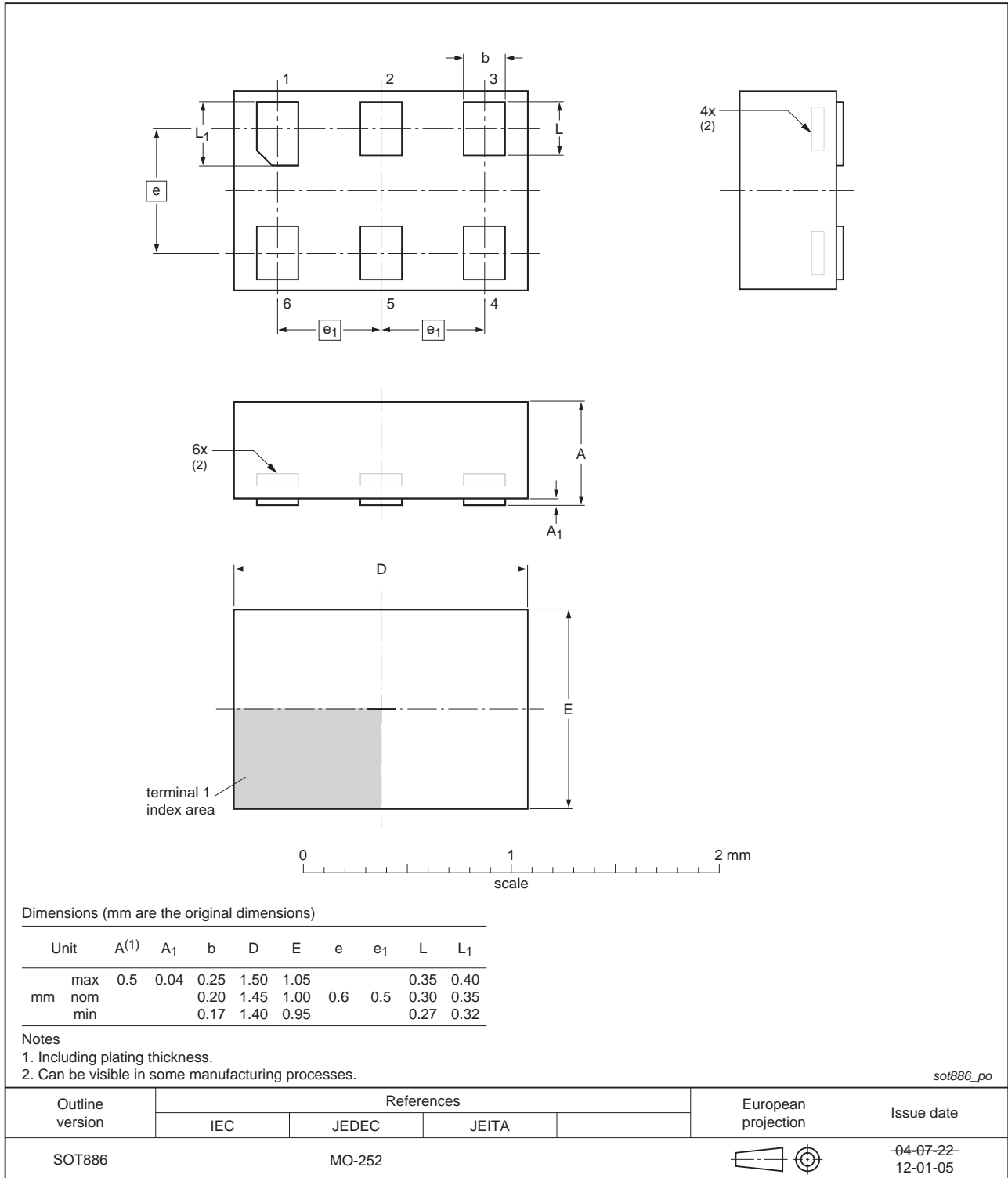


Fig 20. Package outline SOT886 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm**

SOT1115

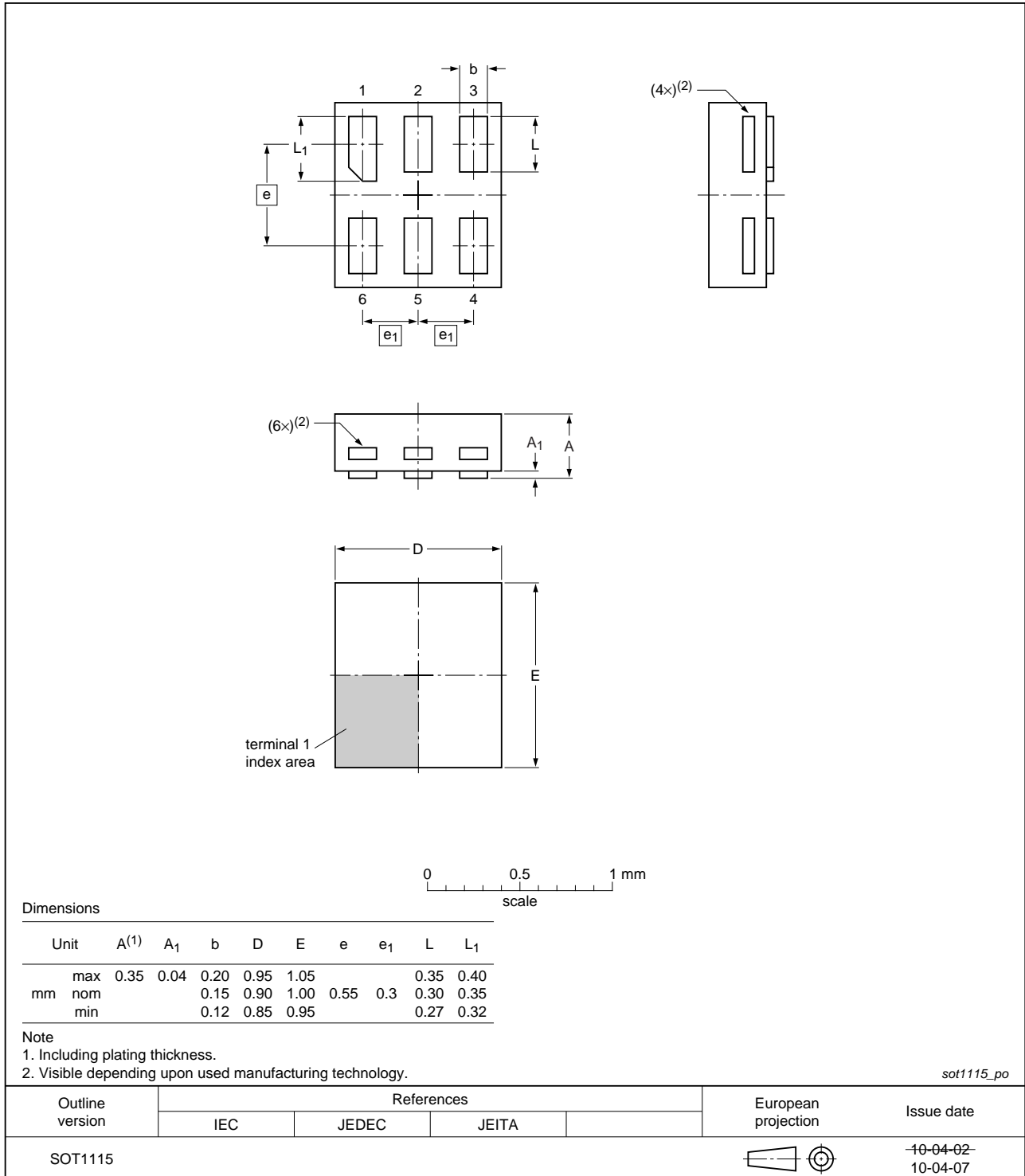


Fig 21. Package outline SOT1115 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm**

SOT1202

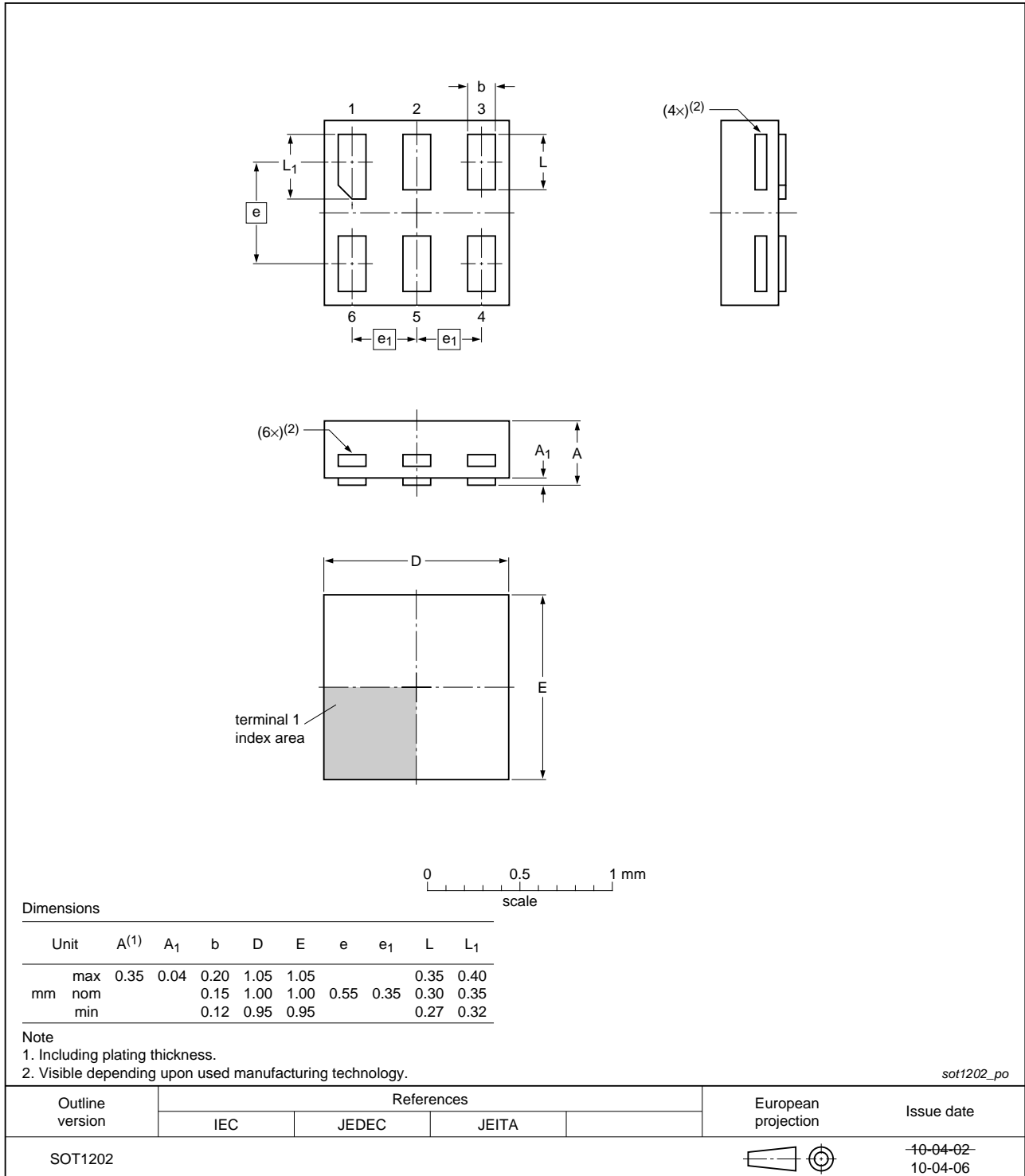


Fig 22. Package outline SOT1202 (XSON6)

13. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|-------------------------|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |

14. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|------------------------|---------------|------------|
| 74AXP1G97 v.1 | 20130625 | Preliminary data sheet | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Ordering information | 2 |
| 4 | Marking | 2 |
| 5 | Functional diagram | 2 |
| 6 | Pinning information | 3 |
| 6.1 | Pinning | 3 |
| 6.2 | Pin description | 3 |
| 7 | Functional description | 3 |
| 7.1 | Logic configurations | 4 |
| 8 | Limiting values | 5 |
| 9 | Recommended operating conditions | 5 |
| 10 | Static characteristics | 6 |
| 10.1 | Waveform transfer characteristics | 7 |
| 11 | Dynamic characteristics | 7 |
| 11.1 | Waveforms and graphs | 8 |
| 12 | Package outline | 11 |
| 13 | Abbreviations | 14 |
| 14 | Revision history | 14 |
| 15 | Legal information | 15 |
| 15.1 | Data sheet status | 15 |
| 15.2 | Definitions | 15 |
| 15.3 | Disclaimers | 15 |
| 15.4 | Trademarks | 16 |
| 16 | Contact information | 16 |
| 17 | Contents | 17 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 June 2013

Document identifier: 74AXP1G97