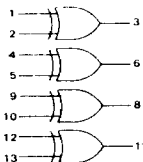
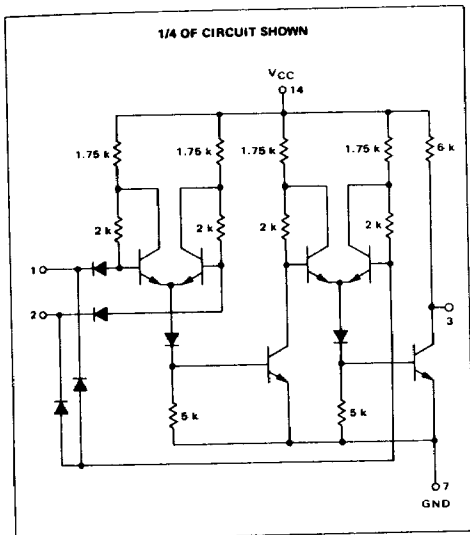


QUAD 2-INPUT  
EXCLUSIVE "OR" GATE

MDTL MC930/830 series

MC1912F • MC1812F,P

This device consists of four 2-input gates, each performing the logical EXCLUSIVE OR function. Added logic flexibility provided by this device helps to optimize system designs.



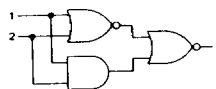
Positive Logic:  $3 = 1 \oplus 2 + \bar{1} \oplus 2$

Input Loading Factor = 2  
Output Loading Factor = 8  
Total Power Dissipation:

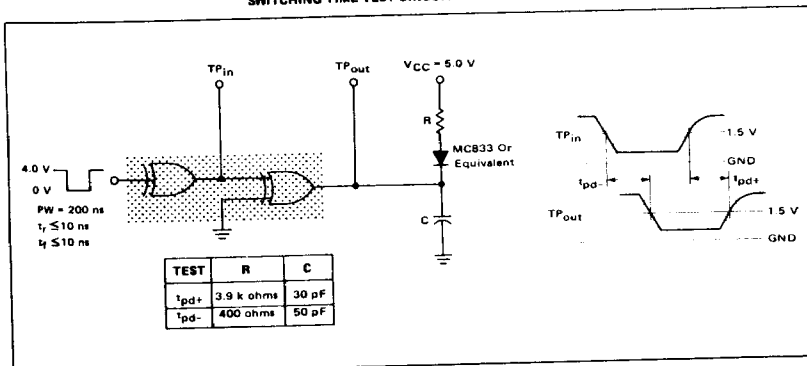
MC1912/MC1812	
Both Inputs High	115 mW
Both Inputs Low	130 mW
One Low One High	95 mW

Propagation Delay Time = 40 ns typ

LOGIC DIAGRAM  
1/4 OF DEVICE SHOWN



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



86



## PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

**Table 1** DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D

