

MM54HC27/MM74HC27



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# MM54HC27/MM74HC27 Triple 3-Input NOR Gate

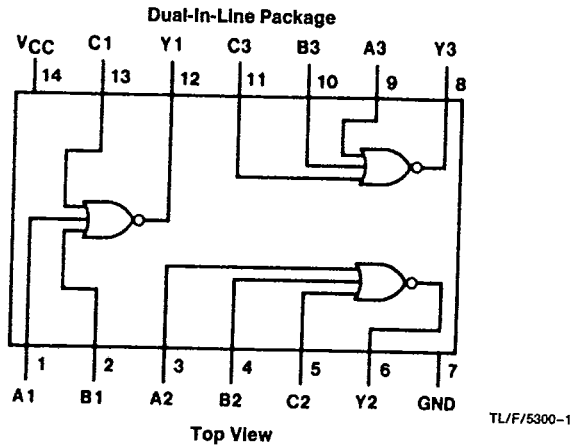
## General Description

These NOR gates utilize advanced silicon-gate CMOS technology, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

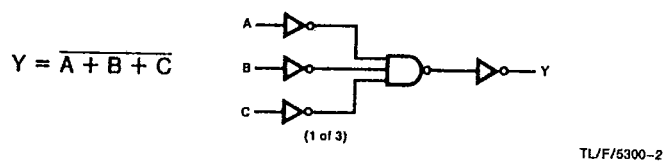
## Features

- Typical propagation delay: 8 ns
- Wide operating supply voltage range: 2-6V
- Low input current:  $< 1 \mu A$
- Low quiescent supply current: 20  $\mu A$  maximum (74HC Series)
- Fanout of 10 LS-TTL Loads

## Connection and Logic Diagrams



Order Number MM54HC27\* or MM74HC27\*  
\*Please look into Section 8, Appendix D for availability of various package types.



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**Absolute Maximum Ratings** (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V <sub>CC</sub> )	-0.5 to +7.0V
DC Input Voltage (V <sub>IH</sub> )	-1.5 to V <sub>CC</sub> +1.5V
DC Output Voltage (V <sub>OUT</sub> )	-0.5 to V <sub>CC</sub> +0.5V
Clamp Diode Current (I <sub>IK</sub> , I <sub>OK</sub> )	±20 mA
DC Output Current, per pin (I <sub>OUT</sub> )	±25 mA
DC V <sub>CC</sub> or GND Current, per pin (I <sub>CC</sub> )	±50 mA
Storage Temperature Range (T <sub>STG</sub> )	-65°C to +150°C
Power Dissipation (P <sub>D</sub> )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T <sub>L</sub> )	
(Soldering 10 seconds)	260°C

**Operating Conditions**

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	Min	Max	Units
Supply Voltage (V <sub>CC</sub> )	2	6	V
DC Input or Output Voltage (V <sub>IH</sub> , V <sub>OUT</sub> )	0	V <sub>CC</sub>	V
Operating Temp. Range (T <sub>A</sub> )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t <sub>r</sub> , t <sub>f</sub> )			
V <sub>CC</sub> =2.0V		1000	ns
V <sub>CC</sub> =4.5V		500	ns
V <sub>CC</sub> =6.0V		400	ns

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C			Units	
				74HC		54HC		
				T <sub>A</sub> = -40 to 85°C		T <sub>A</sub> = -55 to 125°C		
				Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V <sub>IL</sub>	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V <sub>OH</sub>	Minimum High Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V <sub>IN</sub> = V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V <sub>OL</sub>	Maximum Low Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0V		±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0V		2.0	20	40	μA

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.  
**Note 2:** Unless otherwise specified all voltages are referenced to ground.  
**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.  
**Note 4:** For a power supply of 5V ± 10% the worst case output voltages (V<sub>OH</sub> and V<sub>OL</sub>) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5V and 4.5V respectively. (The V<sub>IH</sub> value at 5.5V is 3.85V.) The worst case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0V values should be used.  
 \*\*V<sub>IL</sub> limits are currently tested at 20% of V<sub>CC</sub>. The above V<sub>IL</sub> specification (30% of V<sub>CC</sub>) will be implemented no later than Q1, CY'89.

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**AC Electrical Characteristics**  $V_{CC}=5V, T_A=25^{\circ}C, C_L=15\text{ pF}, t_r=t_f=6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay		8	15	ns

**AC Electrical Characteristics**  $V_{CC}=2.0V\text{ to }6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A=25^{\circ}C$		74HC	54HC	Units
						$T_A=-40\text{ to }85^{\circ}C$	$T_A=-55\text{ to }125^{\circ}C$	
				Typ	Guaranteed Limits			
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
$t_{TLH}, t_{THL}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per gate)		36				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .