

74LV32A

Quad 2-input OR gate

Rev. 1 — 19 December 2018

Product data sheet

1. General description

The 74LV32A is a quad 2-input OR gate.

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

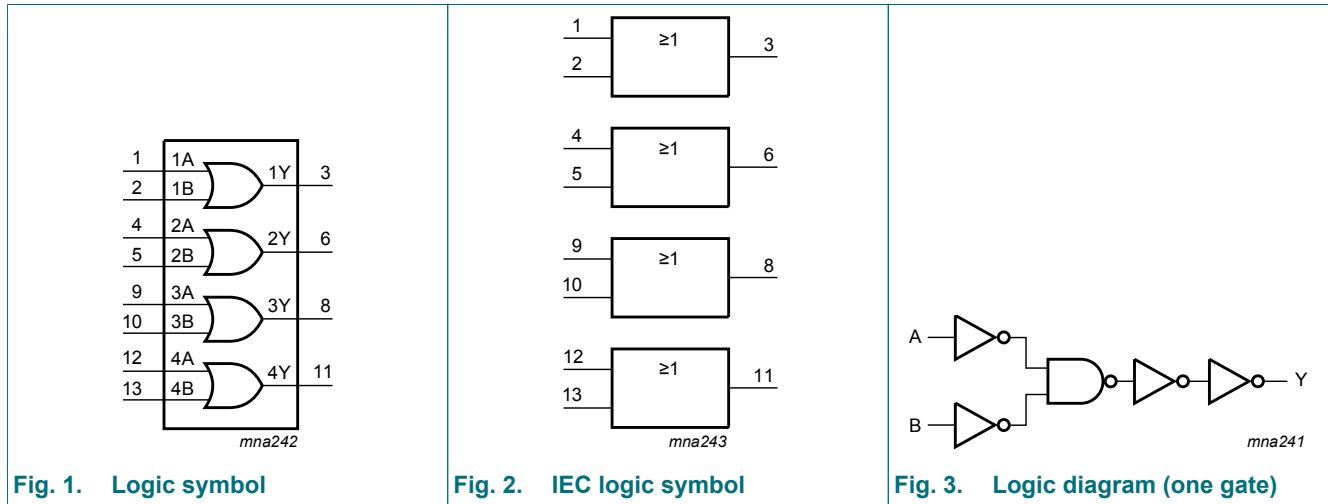
- Wide supply voltage range from 2.0 V to 5.5 V
- Maximum t_{pd} of 9.5 ns at 5 V
- Typical $V_{OL(p)} < 0.8$ V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Typical $V_{OH(v)} > 2.3$ V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - MM: MM JESD22-A115-B exceeds 200 V
 - HBM: ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 4 kV
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2 kV
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

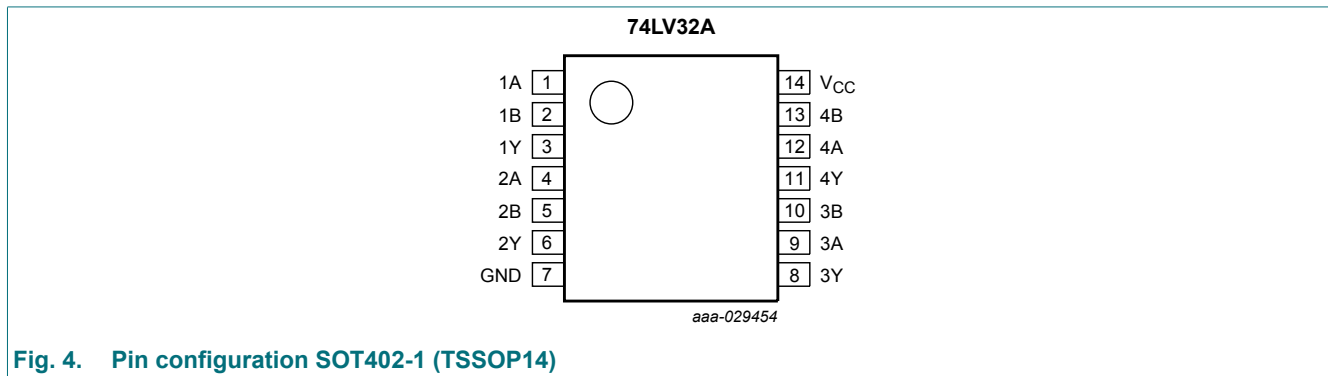
| Type number | Package | | | Version |
|-------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | |
| 74LV32APW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|----------------|
| 1A, 2A, 3A, 4A | 1, 4, 9, 12 | data input |
| 1B, 2B, 3B, 4B | 2, 5, 10, 13 | data input |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

| Input | | Output |
|-------|----|--------|
| nA | nB | nY |
| L | L | L |
| X | H | H |
| H | X | H |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-------------------------------|----------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | [1] -0.5 | +7.0 | V |
| V_O | output voltage | output HIGH or LOW state | [2] -0.5 | $V_{CC} + 0.5$ | V |
| | | output power-down | [2] -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ±35 | mA |
| I_{CC} | supply current | | - | 70 | mA |
| I_{GND} | ground current | | -70 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [4] - | 500 | mW |

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

[3] This value is limited to 7 V maximum.

[4] For SOT402-1 package: above 116 °C, the value of P_{tot} derates linearly at 7.3 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|----------|------|
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | output HIGH or LOW state | 0 | - | V_{CC} | V |
| | | output power-down | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | - | - | 200 | ns/V |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | - | 100 | ns/V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------|---------------------------|---|--------------|-----|-------------|------------------|-------------|-------------------|-------------|---------------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | - | - | 1.5 | - | - | - | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | - | - | V |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | - | - | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2\text{ V}$ | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | V |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $V_{CC} = 2.0\text{ V to }5.5\text{ V}; I_O = -50\text{ }\mu\text{A}$ | $V_{CC}-0.1$ | - | - | $V_{CC}-0.1$ | - | $V_{CC}-0.1$ | - | V |
| | | $V_{CC} = 2.3\text{ V}; I_O = -2\text{ mA}$ | 2 | - | - | 2 | - | 2 | - | V |
| | | $V_{CC} = 3.0\text{ V}; I_O = -6\text{ mA}$ | 2.48 | - | - | 2.48 | - | 2.48 | - | V |
| | | $V_{CC} = 4.5\text{ V}; I_O = -12\text{ mA}$ | 3.8 | - | - | 3.8 | - | 3.8 | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $V_{CC} = 2.0\text{ V to }5.5\text{ V}; I_O = 50\text{ }\mu\text{A}$ | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $V_{CC} = 2.3\text{ V}; I_O = 2\text{ mA}$ | - | - | 0.4 | - | 0.4 | - | 0.4 | V |
| | | $V_{CC} = 3.0\text{ V}; I_O = 6\text{ mA}$ | - | - | 0.44 | - | 0.44 | - | 0.44 | V |
| | | $V_{CC} = 4.5\text{ V}; I_O = 12\text{ mA}$ | - | - | 0.55 | - | 0.55 | - | 0.55 | V |
| I_{OFF} | power-off leakage current | V_I or $V_O = \text{GND to }5.5\text{ V}; V_{CC} = 0\text{ V}$ | - | - | 0.5 | - | 5 | - | 5 | μA |
| I_I | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC} = 0\text{ V to }5.5\text{ V}$ | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}; V_{CC} = 5.5\text{ V}$ | - | - | 2 | - | 20 | - | 20 | μA |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|---|-------|--------|------|------------------|-----|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| t _{pd} | propagation delay | nA, nB to nY; see Fig. 5 [2] | | | | | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | | | | | | | | |
| | | C _L = 15 pF | - | 5.5 | 12.8 | 1 | 15 | 1 | 16 | ns |
| | | C _L = 50 pF | - | 7.6 | 16.2 | 1 | 19 | 1 | 20 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | | | | | | | | |
| | | C _L = 15 pF | - | 4.2 | 7.9 | 1 | 9.5 | 1 | 10.5 | ns |
| | | C _L = 50 pF | - | 5.9 | 11.4 | 1 | 13 | 1 | 14 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 3.2 | 5.5 | 1 | 6.5 | 1 | 7.5 | ns |
| | | C _L = 50 pF | - | 4.7 | 7.5 | 1 | 8.5 | 1 | 9.5 | ns |
| C _I | input capacitance | V _I = V _{CC} or GND; V _{CC} = 3.3 V | - | 2 | 6 | - | 6 | - | 6 | pF |
| C _O | output capacitance | V _O = V _{CC} or GND; V _{CC} = 3.3 V | - | 5.6 | - | - | - | - | - | pF |
| C _{PD} | power dissipation capacitance | per buffer; C _L = 50 pF; f = 10 MHz; V _I = GND to V _{CC} [3] | | | | | | | | |
| | | V _{CC} = 3.3 V | - | 9.2 | - | - | - | - | - | pF |
| | | V _{CC} = 5.0 V | - | 9.4 | - | - | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V, 3.3 V, and 5 V respectively, unless otherwise specified.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

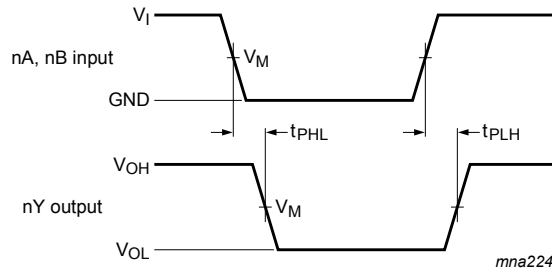
∑(C_L × V_{CC}² × f_o) = sum of outputs.

Table 8. Noise characteristics at T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|------------------------------------|---|------|------|------|------|
| V _{OL(p)} | LOW-level output voltage (peak) | V _{CC} = 3.3 V; C _L = 50 pF | - | 0.2 | 0.8 | V |
| V _{OL(v)} | LOW-level output voltage (valley) | V _{CC} = 3.3 V; C _L = 50 pF | -0.8 | -0.1 | - | V |
| V _{OH(v)} | HIGH-level output voltage (valley) | V _{CC} = 3.3 V; C _L = 50 pF | - | 3.1 | - | V |
| V _{IH(AC)} | AC HIGH-level input voltage | V _{CC} = 3.3 V; C _L = 50 pF | 2.31 | - | - | V |
| V _{IL(AC)} | AC LOW-level input voltage | V _{CC} = 3.3 V; C _L = 50 pF | - | - | 0.99 | V |

10.1. Waveforms and test circuit



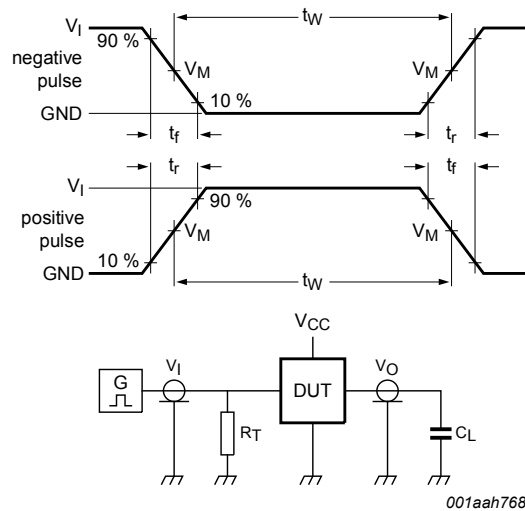
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Input (nA, nB) to output (nY) propagation delays

Table 9. Measurement points

| Input | Output |
|-------------|-------------|
| V_M | V_M |
| $0.5V_{CC}$ | $0.5V_{CC}$ |



Test data is given in [Table 10](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

| Input | | Load | Test |
|-----------------|------------|--------------|--------------------|
| V_I | t_r, t_f | C_L | |
| GND to V_{CC} | 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

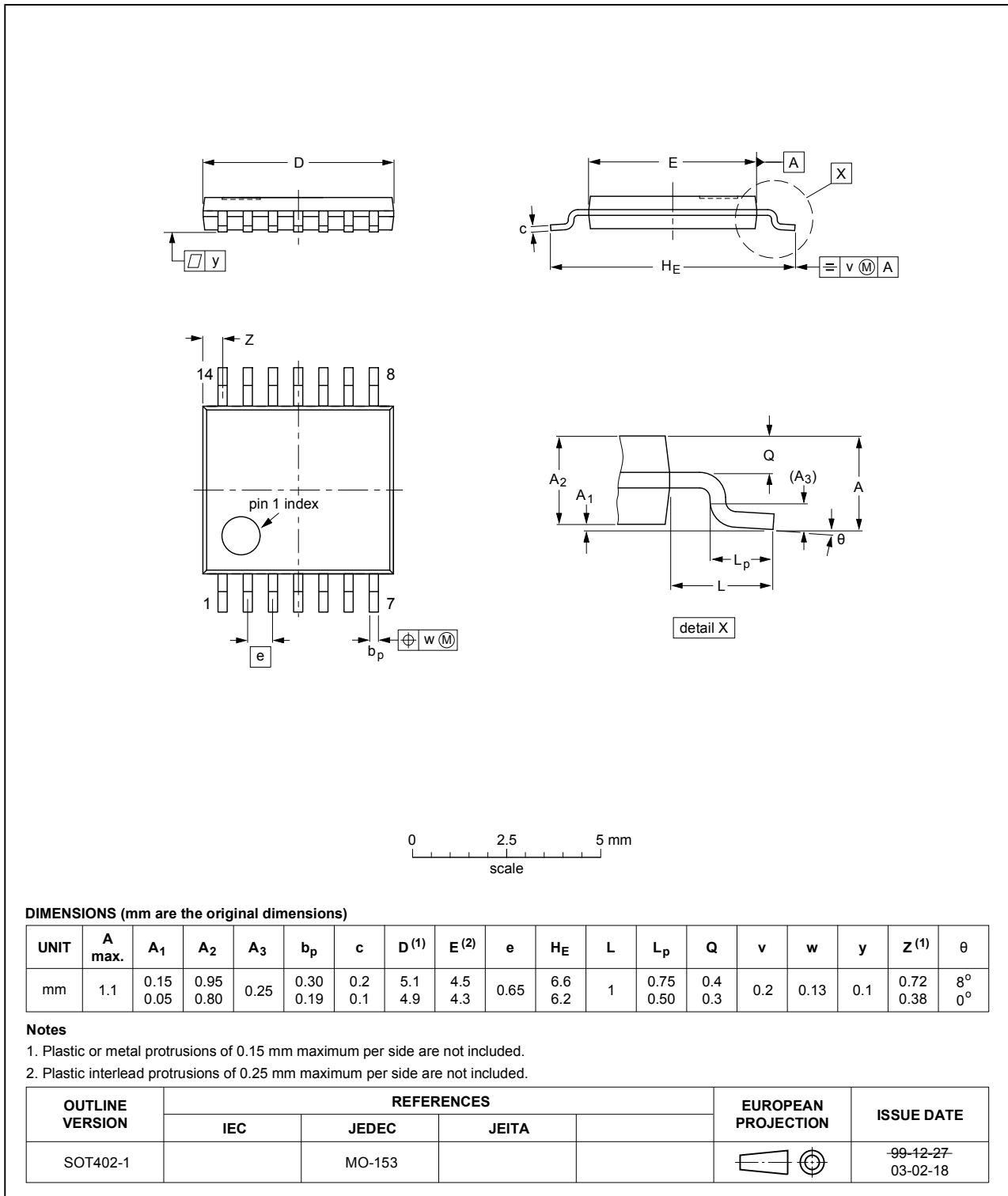


Fig. 7. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|-------------------------|
| CDM | Charge Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TBD | To Be Determined |

13. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| 74LV32A v.1 | 20181219 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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Date of release: 19 December 2018
