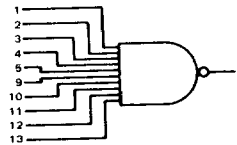
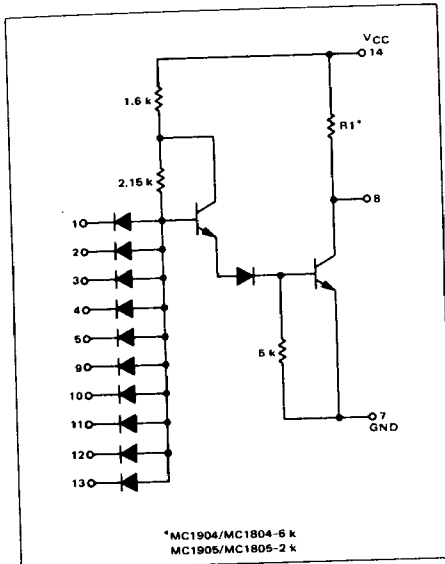


10-INPUT "NAND" GATE

MDTL MC930/830 series

MC1904F · MC1804F, P
MC1905F · MC1805F, P

This device is a 10-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.



Positive Logic: $B = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 9 \cdot 10 \cdot 11 \cdot 12 \cdot 13}$
Negative Logic: $B = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 9 \cdot 10 \cdot 11 \cdot 12 \cdot 13}$

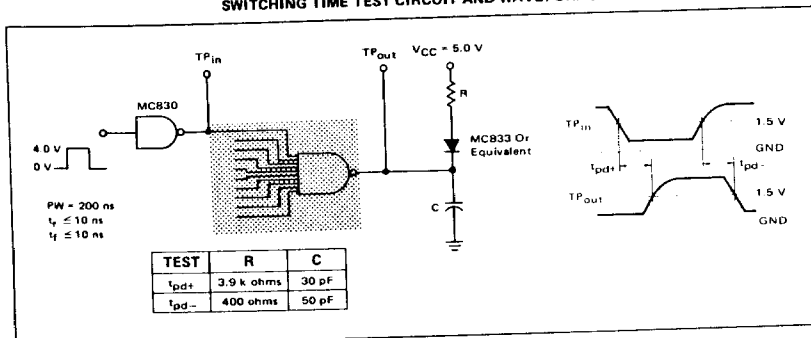
Input Loading Factor = 1

Output Loading Factor:
MC1904/MC1804 = 8
MC1905/MC1805 = 7

Total Power Dissipation:
MC1904/MC1804 = 11 mW typ/pkg
MC1905/MC1805 = 16.5 mW typ/pkg

Propagation Delay Time:
MC1904/MC1804 = 30 ns typ
MC1905/MC1805 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D

