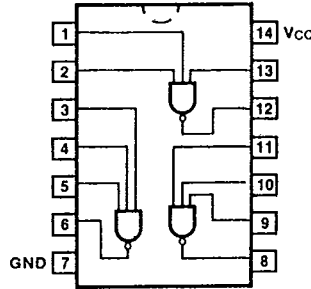


54/7412

TRIPLE 3-INPUT NAND GATE (With Open-Collector Output)

CONNECTION DIAGRAM PINOUT A



4

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	7412PC		9A
Ceramic DIP (D)	A	7412DC	5412DM	6A
Flatpak (F)	A	7412FC	5412FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS	
		Min	Max			
I _{CC} H	Power Supply Current		6.0	mA	V _{IN} = Gnd	V _{CC} = Max
I _{CC} L			16.5		V _{IN} = Open	
t _{PL} H	Propagation Delay		45	ns	Figs. 3-2, 3-4	
t _{PH} L			15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

**OC — Open Collector