

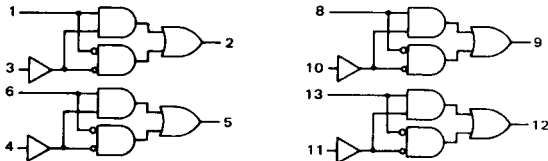
QUAD EXCLUSIVE
"NOR" GATES

MECL II MC1000/1200 series

MC1031
MC1231

Four gate arrays designed to provide four Exclusive NOR functions. The output is high if and only if the two inputs are at the same logic level.

POSITIVE LOGIC



$$2 = 1 \cdot 3 + \bar{1} \cdot \bar{3}$$

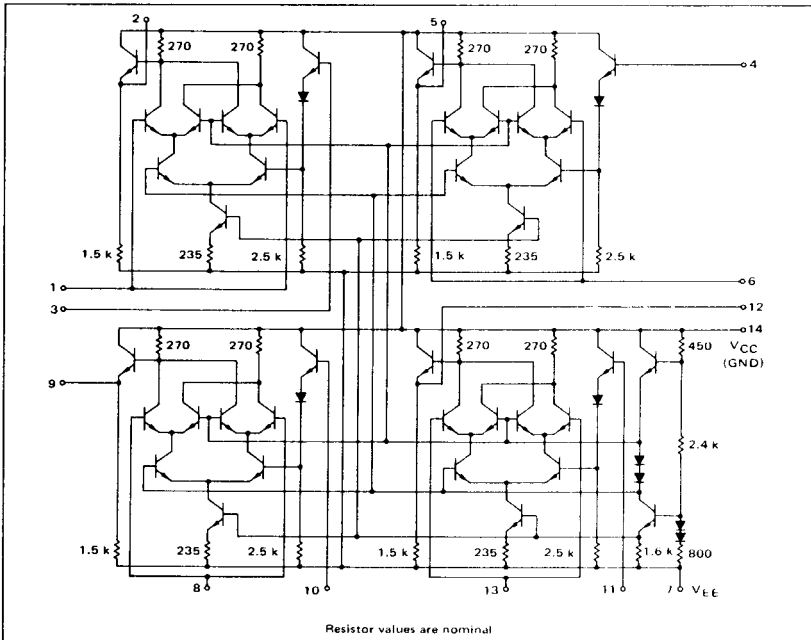
DC Input Loading Factor: Pins 1, 6, 8, 13 = 1.5

Pins 3, 4, 10, 11 = 1

DC Output Loading Factor = 25

Power Dissipation = 130 mW typical

CIRCUIT SCHEMATIC

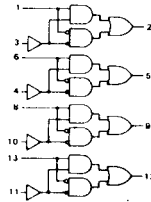


Resistor values are nominal

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MC1031, MC1231 (continued)



ELECTRICAL CHARACTERISTICS

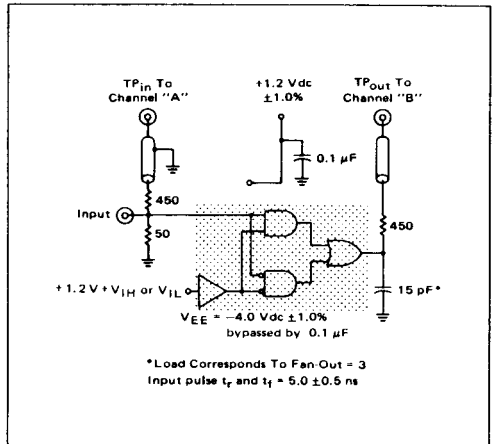
Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1231 Test Limits						MC1031 Test Limits							
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	7	-	--	-	33	-	-	mAdc	-	-	-	33	-	-	mAdc
Input Current	I_{in}	1 3	-	-	-	150 100	-	-	μ Adc μ Adc	-	-	-	150 100	-	-	μ Adc μ Adc
Input Leakage Current	I_R	1 3	-	-	-	0.4 0.2	-	2.0 1.0	μ Adc μ Adc	-	-	-	0.4 0.2	-	2.0 1.0	μ Adc μ Adc
Logical "1" Output Voltage	$V_{OH} \ddagger$	2 2	-0.990 -0.990	-0.825 -0.825	-0.850 -0.850	-0.700 -0.700	-0.700 -0.700	-0.530 -0.530	Vdc Vdc	-0.895 -0.895	-0.740 -0.740	-0.850 -0.850	-0.700 -0.700	-0.775 -0.775	-0.615 -0.615	Vdc Vdc
Logical "0" Output Voltage	V_{OL}	2 2	-1.890 -1.890	-1.580 -1.580	-1.800 -1.800	-1.500 -1.500	-1.720 -1.720	-1.380 -1.380	Vdc Vdc	-1.830 -1.830	-1.525 -1.525	-1.800 -1.800	-1.500 -1.500	-1.760 -1.760	-1.435 -1.435	Vdc Vdc
Switching Times (Fan-Out = 3) Propagation Delay	t_{1-2} t_{1-2+} t_{1+2} t_{1-2-} t_{3-2} t_{3-2+} t_{3-2-}	2	Typ 5.0	Max 8.5	Typ 5.0	Max 8.5	Typ 6.0	Max 10	ns	Typ 5.0	Max 8.5	Typ 5.0	Max 8.5	Typ 6.0	Max 9.0	ns
Rise Time	t_{2+} t_{2-}		5.0 6.0	8.5 9.0	5.0 6.0	8.5 9.0	9.5 10	9.0 10		5.0 6.0	8.5 9.0	5.0 6.0	8.5 9.0	6.0 6.0	9.0 9.5	
Fall Time	t_{2+} t_{2-}		5.0 6.0	8.5 9.0	5.0 6.0	8.5 9.0	9.5 10	9.0 10		5.0 6.0	8.5 9.0	5.0 6.0	8.5 9.0	6.0 6.0	9.0 9.5	

V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

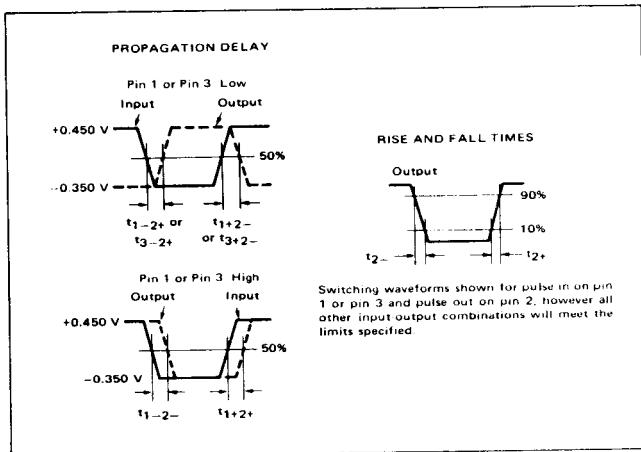
* V_{IL} or V_{IH} value as given plus ± 1.2 V

SWITCHING TIME TEST CIRCUIT @ 25°C



@ Test Temperature		TEST VOLTAGE/CURRENT VALUES				
		V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L (mAdc)
MC1231	-55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1031	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					V_{CC} (Gnd)
			V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	
Power Supply Drain Current	I_E	7	-	-	-	1, 3, 4, 6, 7, 8, 10, 11, 13	-	14
Input Current	I_{in}	1 3	-	-	1 3	3, 7	-	14
Input Leakage Current	I_R	1 3	-	-	-	1, 3, 7	-	14
Logical "1" Output Voltage	$V_{OH} \dagger$	2 2	1, 3 -	- 1, 3	-	7 7	2 2	14 14
Logical "0" Output Voltage	V_{OL}	2 2	1 3	3 1	-	7 7	-	14 14
Switching Times (Fan-Out = 3)			V_{IL}	V_{IH}	Pulse In	$V_{EE} = 4.0\ Vdc$	Pulse Out	+1.2 Vdc
Propagation Delay	t_{1+2-} t_{1-2+} t_{1+2-} t_{1-2+} t_{3+2-} t_{3-2+} t_{3+2-} t_{3-2+}	2	3 3 - - 1 1 - -	- 3 3 - - 1 1 - -	1 - 3 - - - - -	7 - - - - - - -	2 - - - - - - -	14 - - - - - - -
Rise Time	t_{2+} t_{2-}		- 3	1 -	3 -	- -	- -	- -
Fall Time	t_{2-} t_{2+}		3 -	- 1	- 3	- -	- -	- -



SWITCHING TIME WAVEFORMS

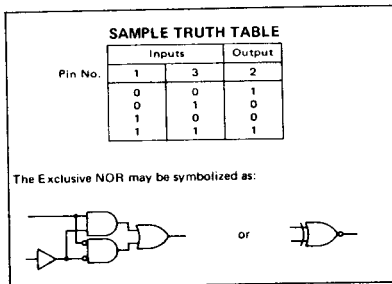
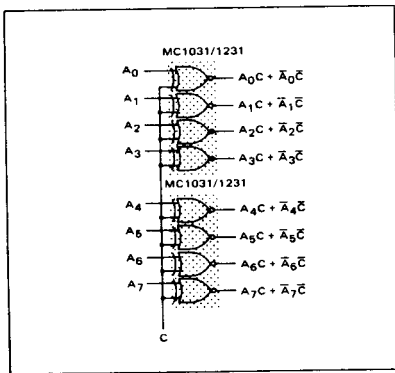
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APPLICATIONS INFORMATION

The MC1031/MC1231 quad Exclusive NOR gate is obtained by changing circuit interconnections of the MC1030/MC1230 through use of a different metal mask. The quad Exclusive NOR (\odot) is useful for data comparison, parity generation and checking, decision circuitry, code conversion circuitry, and frequency mixing. The output of each Exclusive NOR is high if the two inputs are at the same logic levels. The Exclusive NOR is the logical complement or inversion of the Exclusive OR.

Figure 1 illustrates a controlled data inverter in which parallel data can be either inverted or not inverted with a single control level.

FIGURE 1 — CONTROLLED DATA INVERTER



For example, the input information is passed directly to the output if C is at a high level. Exclusive OR gates may also be used to perform this function. The C input would be inverted for the same logic function.

Figure 2 illustrates checking the bits of a word for even parity; if the sum of the inputs is even, the output will be high. (It is also possible to mix MC1031/MC1231 quad Exclusive NOR gates and MC1030/MC1230 quad Exclusive OR gates to obtain the same function.)

FIGURE 2 — 25 ns 16-BIT PARITY CHECKER (Even Parity)

