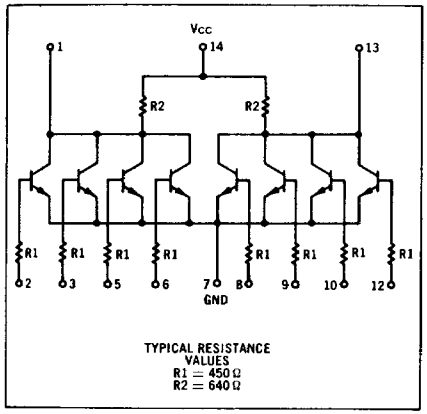
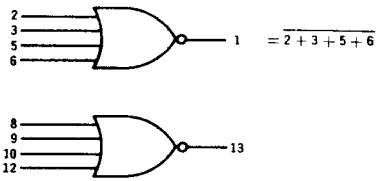
MC925 • MC825

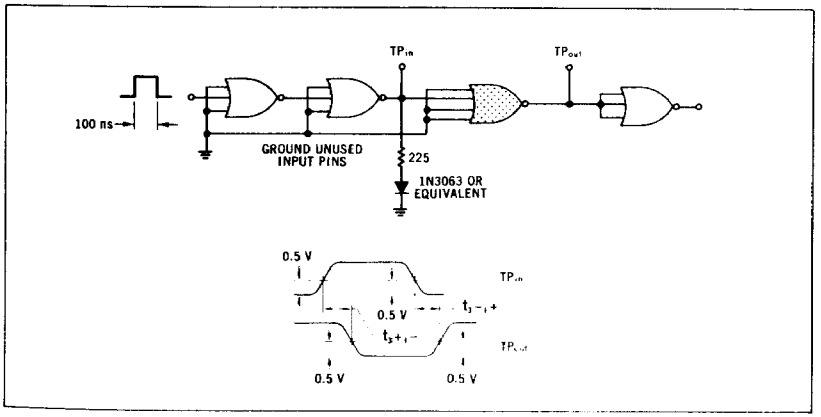
Available in TO-86 Flat Package, Add "F" Suffix.

Two 4-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC925	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC825	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC925 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC825 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2 3 5 6	- - - -	495 ↓ ↓ ↓	- - - -	435 ↓ ↓ ↓	- - - -	470 ↓ ↓ ↓	uAdc ↓	- - - -	504 ↓ ↓ ↓	- - - -	450 ↓ ↓ ↓	- - - -	450 ↓ ↓ ↓	uAdc ↓	2 3 5 6	- - - -	3,5,6 2,5,6 2,3,6 2,3,5	- - - -	14 ↓	7 ↓
Output Current	I_{A5}	1	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1	-	2,3,5,6	14	7
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	uAdc	-	100	-	225	-	225	uAdc	1	-	-	2,3,5,6	-	7
Output Voltage	V_{out}	1 ↓	- - - -	710 ↓ ↓ ↓	- - - -	300 ↓ ↓ ↓	- - - -	320 ↓ ↓ ↓	mVdc ↓	- - - -	574 ↓ ↓ ↓	- - - -	400 ↓ ↓ ↓	- - - -	370 ↓ ↓ ↓	mVdc ↓	- - - -	2 3 5 6	- - - -	- - - -	14 ↓	3,5,6,7 2,5,6,7 2,3,6,7 2,3,5,7
Saturation Voltage	$V_{CE(sat)}$	1 ↓	- - - -	200 ↓ ↓ ↓	- - - -	210 ↓ ↓ ↓	- - - -	280 ↓ ↓ ↓	mVdc ↓	- - - -	290 ↓ ↓ ↓	- - - -	260 ↓ ↓ ↓	- - - -	340 ↓ ↓ ↓	mVdc ↓	- - - -	- - - -	2 3 5 6	- - - -	14 ↓	3,5,6,7 2,5,6,7 2,3,6,7 2,3,5,7
Switching Time	t	3+1- 3-1+	- -	- -	- -	20 28	- -	- -	ns ns	- -	- -	- -	20 28	- -	- -	ns ns	Pulse In 3 3	Pulse Out 1 1	- -	- -	14 14	2,5,6,7 2,5,6,7

Ground inputs of gate not under test. Other pins not listed are left open.

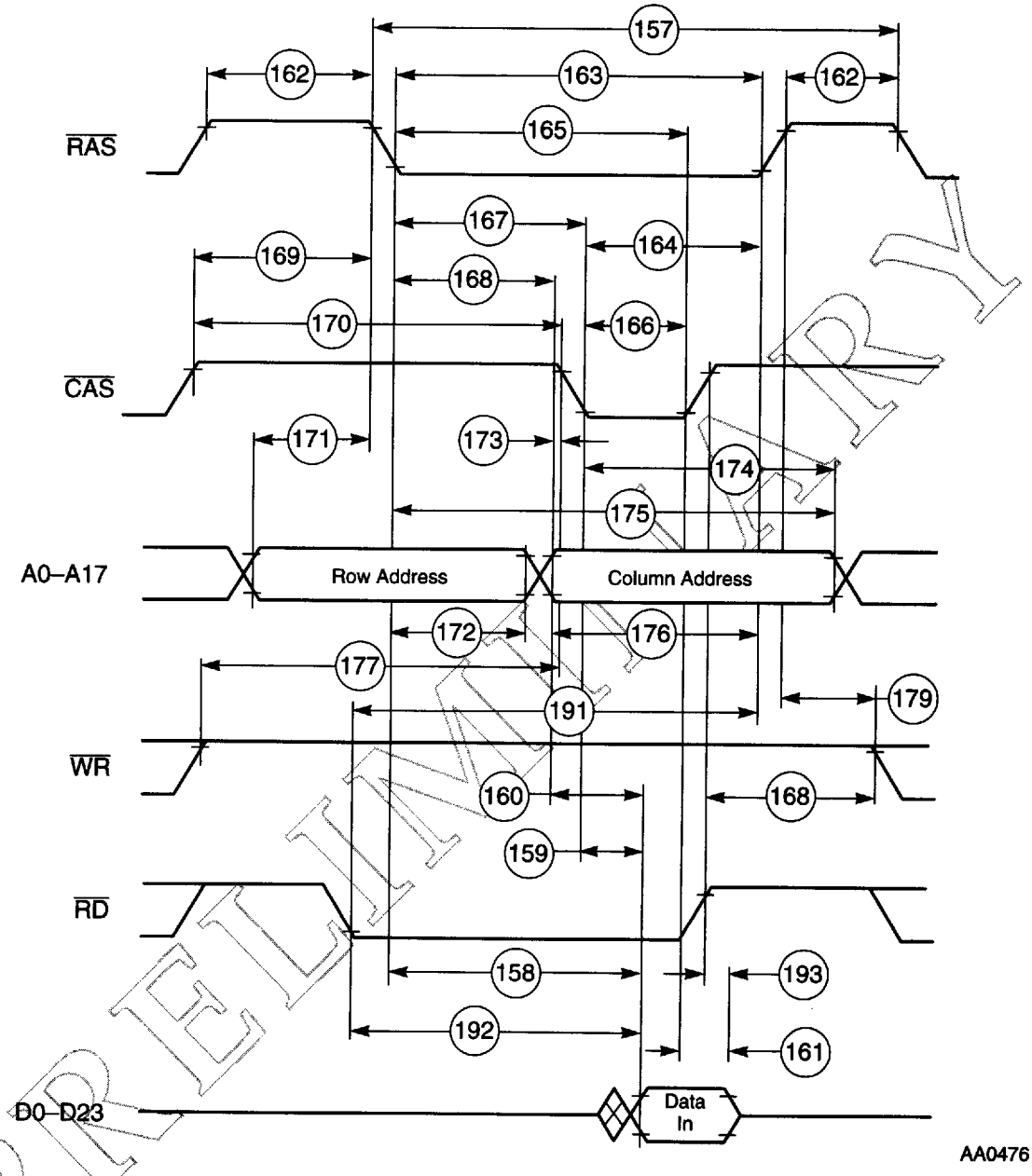


Figure 2-18 DRAM Out-of-Page Read Access