# Technical Overview

## Description

The Harris HC/HCT series of high speed CMOS integrated circuits (QMOS) includes a functionally complete set of LSTTL equivalent types and selected equivalent CMOS CD4000 series types. The CD4000 series types selected are unique to the CMOS process. These types are readily produced by the highly versatile CMOS technology, but cannot be implemented by the more restrictive bipolar technology. Each CMOS circuit function is offered in two basic logic series, as follows:

**CD54/74HCTXXXX-Series Types.** These feature LSTTL input voltage level compatibility and provide high speed CMOS direct drop-in replacements of LSTTL devices.

**CD54/74HCXXXX-Series Types.** These feature CMOS input voltage level compatibility and are intended for use in new second generation all CMOS systems.

In addition, Harris offers a third category, CD54/74HCUXX, which includes unbuffered types intended for linear or high speed oscillator applications.

The HC/HCT family consists of a comprehensive set of buffers, transceivers, and registers that are popular in computer systems. A wide variety of popular logic, MUXs, encoders/decoders, counters, arithmetic units, mulitvibrators, display drivers, and phase-lock loops complete the family.

Shown below is a breakdown of the HC/HCT family by logic function:

**THE HC/HCT FAMILY**

**Device Function**

- Inverters/Buffers/Bus Drivers
- Flip-Flops/Latches
- Bus Transceivers
- Registers
- Counters
- Decoders/Encoders
- Multiplexers (Analog and Digital)
- Multivibrators
- Schmitt Triggers
- Phase-Lock Loops
- Bilateral Switches
- Arithmetic Circuits
- Gates

NOTE: Each function is available in both an HCT and HC version.

## Features

- Functionally and Pin Compatible with Industry 54 and 74 LSTTL-Series and CD4000B-Series Types
- CMOS Outputs for Maximum Noise Margins
- Fanout (Over Temperature):
  Standard Outputs - 10 LSTTL Loads
  Bus-Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Ranges
  CD74HC/HCT/HCU. . . . . -55°C to +125°C
  CD54HC/HCT/HCU. . . . . -55°C to +125°C
- Balanced Propagation and Transition Times
- Significant Power Reduction Compared to LSTTL Logic

**Series Features**

CD54HCXXXX and CD74HCXXXX Series

- 2V to 6V Operation
- High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% at $V_{CC}$ = 5V

CD54HCTXXXX and CD74HCTXXXX Series

- 4.5V to 5.5V Operation
- Direct LSTTL Input Logic Compatibility: $V_{IL}$ 0.8V(Max), $V_{IH}$ = 2.0V (Min)
- CMOS Input Compatibility: $I_{IL}$, $I_{IH}$ ≤1μA at $V_{OL}$, $V_{OH}$

**Quantitative Comparison of HC/HCT and LSTTL Logic Types**

Harris HC and HCT logic types have many outstanding advantages when compared with the conventional high current LSTTL logic types which these types can replace in existing and new equipment designs that require devices operating at frequencies in the 20MHz to 30MHz range. Table 1 compares significant operating characteristics of the HC/HCT vs LSTTL logic families.

**TABLE 1. QUANTITATIVE COMPARISON OF HC/HCT AND LSTTL LOGIC TYPES**

| PARAMETERS | 74 SERIES HC/HCT | | | 74 SERIES LSTTL | |
|---|---|---|---|---|---|
| QUIESCENT POWER | | | | | |
| Per Gate | 0.025mW | | | 5.5mW | |
| Per FF | 0.05mW | | | 10mW | |
| 4 Stage Counter | 0.4mW | | | 95mW | |
| Per Transceiver/Buffer | 0.1mW | | | 60mW | |
| OPERATING POWER | | | | | |
| | FREQUENCY | | | FREQUENCY | |
| | 0.1MHz | 1MHz | 10MHz | 0.1 to 1MHz | 10MHz |
| Per Gate | 0.2mW | 2mW | 20mW | 5.5mW | 20mW |
| Per FF | 0.15mW | 1.5mW | 15mW | 10mW | 15mW |
| 4 Stage Counter | 0.24mW | 2.4mW | 24mW | 95mW | 120mW |
| Per Transceiver /Buffer | 0.25mW | 2.5mW | 25mW | 60mW | 90mW |
| OPERATING SUPPLY VOLTAGE | | | | | |
| | (HC) 2V to 6V (HCT) 4.5V to 5.5V | | | 4.75V to 5.25V | |

**TABLE 1. QUANTITATIVE COMPARISON OF HC/HCT AND LSTTL LOGIC TYPES (Continued)**

| PARAMETERS | | 74 SERIES HC/HCT | 74 SERIES LSTTL |
|---|---|---|---|
| OPERATING TEMPERATURE RANGE | | | |
| | | -40°C to +85°C | 0°C to +70°C |
| NOISE MARGIN AT 5V | | | |
| LS to LS | (Hi/Low) | - | 0.7V/0.4V |
| HC to HC | | 1.4V/1.4V | - |
| HCT to HCT | | 2.9V/0.7V | - |
| INPUT SWITCHING VOLTAGE VARIATION WITH TEMPERATURE | | | |
| | | $V_S \pm 60mV$ | $V_S \pm 200mV$ |
| OUTPUT DRIVE CURRENT | | | |
| Source Current at $V_{OH} = 2.4V$ | | -8mA | -400µA |
| Sink Current | Std. Logic ($V_{OL}$) | 4mA (0.33V) | 4mA (0.4V) |
| | BUS Logic ($V_{OL}$) | 6mA (0.33V) | 12mA (0.4V) |
| | $V_{OL} = 0.5V$ | 12mA | 24mA |
| TYPICAL OUTPUT TRANSITION TIME (Note 1) | | | |
| $t_{TLH}$ | | 6ns | 15ns |
| $t_{THL}$ | | 6ns | 6ns |
| TYPICAL GATE PROPAGATION DELAY (Note 1) | | | |
| $t_{PHL}/t_{PLH}$ $V_{CC} = 5V, C_L = 15pF$ | | 8ns/8ns | 8ns/11ns |
| TYPICAL FF PROPAGATION DELAY | | | |
| $t_{PHL}$ $V_{CC} = 5V, C_L = 15pF$ | | 14ns | 22ns |
| $t_{PLH}$ $V_{CC} = 5V, C_L = 15pF$ | | 14ns | 15ns |
| TYPICAL CLOCK RATE OF AN FF | | | |
| | | 50MHz | 33MHz |
| INPUT CURRENT | | | |
| $I_{IL}$ | | -1µA | -0.4mA to -0.8mA |
| $I_{IH}$ | | 1µA | 40µA |
| THREE-STATE OUTPUT LEAKAGE CURRENT | | | |
| | | ±5µA | ±20µA |
| RELIABILITY | | | |
| %/1000 hours at 60% Confidence | | 0.0019 Harris Report | 0.008 RADC Report |

NOTE:

1. Loading coefficient = 0.055ns/pF (both HC/HCT and LSTTL).

## IC Structure

The high speeds and low quiescent power dissipation that characterize the Harris HC/HCT family are made possible by utilizing a 3µ, self-aligned silicon gate CMOS process. The 3µ process minimizes the internal parasitic capacitances of the circuit, which results in increased switching speed.

The polysilicon gates of the transistors are deposited over a thin gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the implantation. The source and drain are automatically aligned to the gate, hence the expression "self-aligned-gate" process. In this manner, gate-to-source and gate-to-drain capacitances are minimized. Junction capacitances, which are proportional to the junction area, are also reduced because of the shallower diffusions. Figure 1 shows the parasitic capacitances in a CMOS inverter.

In contrast, the source and drain areas in a metal-gate CMOS process are formed before the gate is deposited.

Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. These conditions result in higher overlap capacitances than those present in QMOS devices. The metal-gate process also employs deeper diffusions than those in the QMOS process and, consequently, has larger junction capacitances.

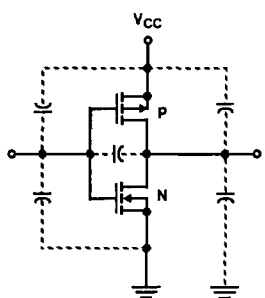



**FIGURE 1. PARASITIC CAPACITANCES IN A CMOS INVERTER**

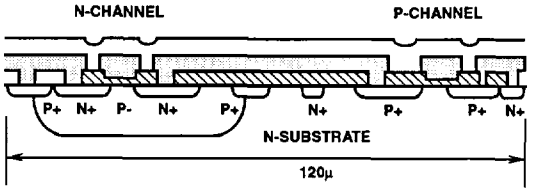
The QMOS structure features a 3µ gate length; the CD4000 series structure has a gate length of 7µ. The equation for the drain current of a MOSFET is:

$$I_{DS} = K' \frac{\text{width}}{\text{length}} [(\text{Gate Voltage}) - (\text{Threshold Voltage})]^2$$

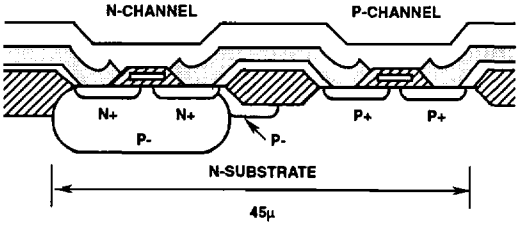
where K ′ is the "beta" of the MOSFET. Therefore, a shorter gate length results in higher drive capability, which in turn increases the speed at which a transistor can charge or discharge capacitance.

The polysilicon in a silicon-gate process is also an interconnect layer, thus, there are three levels of interconnect (diffusion, polysilicon, and metal) instead of the two layers (diffusion and metal) present in a metal gate process. This

situation aids in making a more compact die. Figure 2 compares the cross sections of the 7μ metal-gate CMOS structure and the 3μ QMOS structure.




A. CD4000B SERIES




B. QMOS

FIGURE 2. CROSS-SECTIONAL VIEW OF:
(A.) 7μ CD4000B SERIES STRUCTURE
(B.) 3μ QMOS STRUCTURE

## Input Characteristics

The inputs of QMOS devices are voltage level sensitive, and do not require current, except for input leakage. The definitive switching characteristics for the HC and HCT versions are illustrated in Figure 3 and Figure 4, respectively.

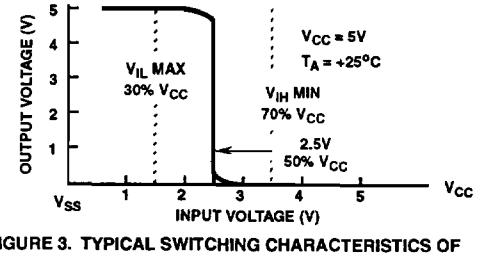



FIGURE 3. TYPICAL SWITCHING CHARACTERISTICS OF HARRIS HC SERIES TYPES

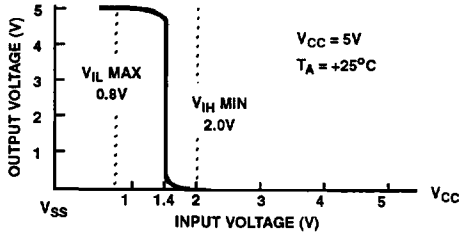



FIGURE 4. TYPICAL SWITCHING CHARACTERISTICS OF HARRIS HCT SERIES TYPES

System designers require the actual Min/Max range of expected input switching voltage over the temperature range of -55°C to +125°C. This vital information is contained in the curves of Figure 5 and Figure 6 for the HC and HCT families, respectively.

The unbuffered HCU04 hex inverter has one stage of active inverting logic from input to output and, therefore, is a special case for input switching voltage as shown in Figure 7.

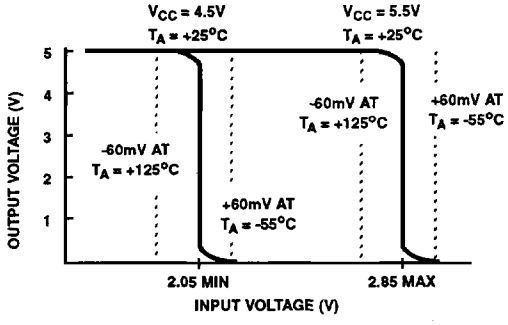



FIGURE 5. ACTUAL MIN/MAX SWITCHING CHARACTERISTICS OF HARRIS HC SERIES TYPES

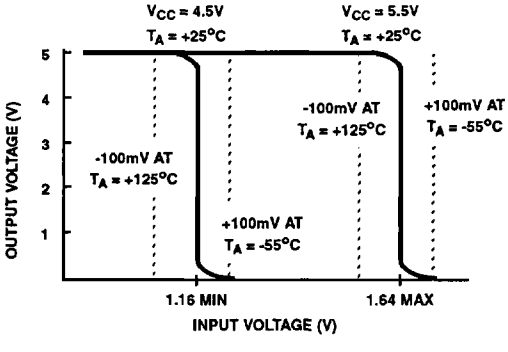



FIGURE 6. ACTUAL MIN/MAX SWITCHING CHARACTERISTICS OF HARRIS HCT SERIES TYPES

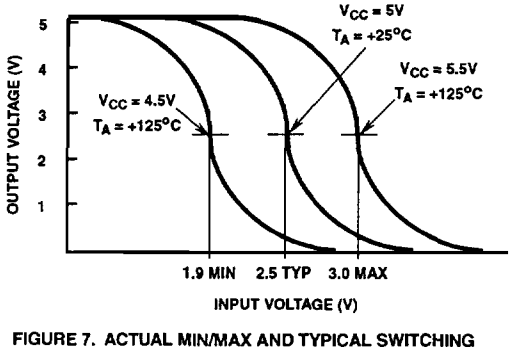



FIGURE 7. ACTUAL MIN/MAX AND TYPICAL SWITCHING CHARACTERISTICS OF THE HCU04 UNBUFFERED HEX INVERTER

### Noise Immunity and Noise Margin

Table 2A shows the HC, HCT, and HCU input noise immunity and noise margin for use in those applications where like members of the HC, HCT, and HCU families interface with each other at a nominal supply voltage of 5V. Output voltages are also shown.

**TABLE 2A. NOISE IMMUNITY AND NOISE MARGIN ($V_{CC}$ = 5V)**

| | HC | HCT | HCU |
|---|---|---|---|
| $V_{IL}$ Max | 1.5V | 0.8V | 1V |
| $V_{IH}$ Min | 3.5V | 2V | 4V |
| $V_{OL}$ Max | 0.1V | 0.1V | 0.5V |
| $V_{OH}$ Min | 4.9V | 4.9V | 4.5V |
| Noise Margin Low ($V_{NML}$) | 1.4V | 0.7V | 0.5V |
| Noise Margin High ($V_{NMH}$) | 1.4V | 2.9V | 0.5V |

Table 2B shows noise immunity and noise margin voltages for standard HCT devices interfacing with LSTTL logic types with a fully loaded HCT or LSTTL output at $V_{CC}$ = 4.5V, and a temperature range of 0°C to +70°C. This limited LSTTL temperature range is the only convenient temperature range when using LSTTL characteristics.

Whenever the HCT output drives either an LS or HCT input, there is an improvement in noise margin over the LSTTL family driving itself or driving HCT. This improvement is especially true for noise margin high where the superior output sourcing current of the rail-to-rail QMOS output swing is far superior to the limited totem-pole pull-up output voltage of LSTTL.

**TABLE 2B. NOISE IMMUNITY AND NOISE MARGIN FOR HCT AND LS DEVICE INTERFACING**

| | HCT | LSTTL | HCT→LS | LS→HCT | LS→LS | HCT→HCT |
|---|---|---|---|---|---|---|
| $V_{IL}$Max | 0.8V | 0.8V | - | - | - | - |
| $V_{IH}$Min | 2V | 2V | - | - | - | - |
| $V_{OL}$Max | 0.33V | 0.4V | - | - | - | - |
| $V_{OH}$Min | 4.4V | 2.7V | - | - | - | - |
| $V_{NML}$ | - | - | 0.47V | 0.4V | 0.4V | 0.7V |
| $V_{NMH}$ | - | - | 2.4V | 0.7V | 0.7V | 2.4V |

### Input Current

Figure 8 is a plot of typical HC/HCT device input current vs. temperature for a $V_{CC}$ of 6V. This actual performance of under 1.5nA over the temperature range of -55°C to +125°C contrasts with maximum family and JEDEC standard input leakage current limit of 100nA for T = -55°C to +25°C, and a limit of 1µA at $T_A$ = +85°C and +125°C. The reason for this difference in performance vs ratings is high speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the limits are end-of-life, thus allowing some leakage current shift due to minor externally introduced foreign material or moisture.

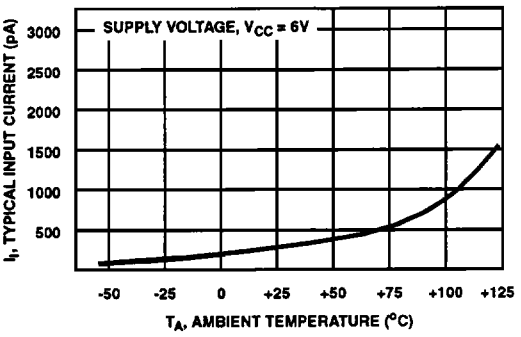



**FIGURE 8. TYPICAL HC/HCT INPUT CURRENT vs TEMPERATURE**

### Input Termination

The very low HC/HCT input current and hence, high input resistance is primarily due to low-level leakage currents of the input ESD protection diodes shown in Figure 9. This excellent input buffering characteristic of CMOS logic ICs is fundamental to the wide range of very low power applications from pure logic to wide range RC oscillators, high Q crystal oscillators, etc. However, in no situation should this high input resistance be left floating or unterminated. Inputs may be tied directly to $V_{CC}$ or GND via resistors of up to 1MΩ; the upper limit is only related to AC noise immunity, i.e., pick up.

Comparing HC/HCT unused input terminations to LSTTL logic, puts the flexibility of QMOS into a very positive light. It is a stated LSTTL design rule that unused inputs be terminated to $V_{CC}$ via a 1.2kΩ resistor and not tied directly to GND or $V_{CC}$ nor left floating.

One additional note on HC/HCT input terminations. There are several bidirectional (transceiver) logic types in the QMOS family with common I/O pins. These I/O pins do not have the input poly resistor (R) of Figure 9. Hence, these pins cannot be terminated directly to $V_{CC}$ or GND. A terminating resistor to $V_{CC}$ or GND of 10kΩ is recommended.

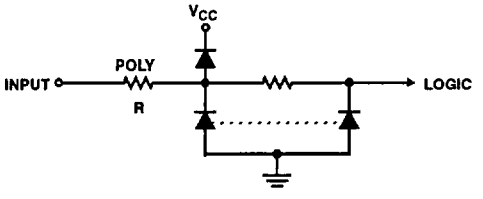



**FIGURE 9. RESISTOR DIODE PROTECTION NETWORK USED ON INPUTS OF HC/HCT DEVICES TO PROTECT DEVICE GATE OXIDE FROM ELECTROSTATIC DISCHARGE DAMAGE (ESD)**

### Input/Output ESD Protection

HC/HCT device inputs have a resistor-diode protection network, shown in Figure 9, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels typically greater than 2kV in all modes pertaining to the input, as shown in Figure 10. The

2kV figure was arrived at by testing devices in the ESD test circuit shown in Figure 11 while conforming to the MIL-I-38535 requirements.

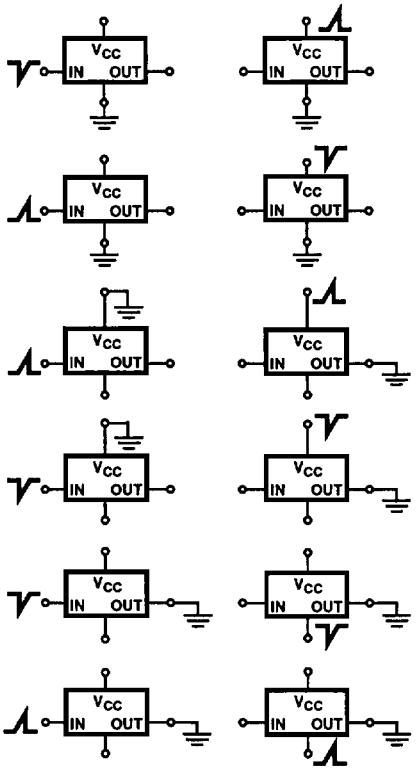
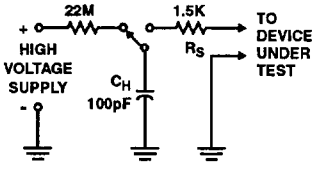



FIGURE 10. HC/HCT ESD TEST MODES

The recommended handling practices for QMOS devices are similar to those described in Application Note AN6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits". See Section 8, "How to Use AnswerFAX", of this selection guide.




$C_H$ = HUMAN BODY CAPACITANCE TO GROUND
$R_S$ = BODY SOURCE RESISTANCE

FIGURE 11. TEST CIRCUIT USED TO MEASURE ELECTROSTATIC DISCHARGE (ESD) IN HC/HCT CIRCUITS. THE RISE TIME AT THE OUTPUT TERMINAL SHOULD BE 13ns ± 2ns

**Input Interaction**

Another effect of the input-protection network is the imposition of a parasitic transistor between adjacent input pins. Figure 12 shows this transistor.

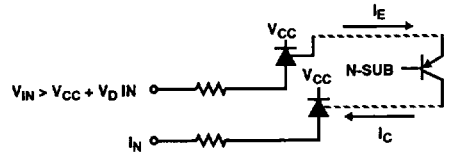
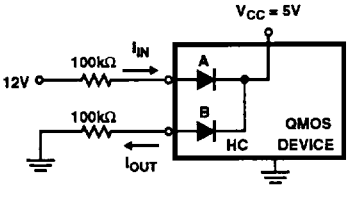



FIGURE 12. PARASITIC TRANSISTOR CAUSED BY INPUT-PROTECTION NETWORK

This parasitic transistor may cause undesirable interaction between adjacent inputs if the input level is greater than $V_{CC}$ + $V_{DIODE}$. QMOS devices minimize the alpha ($\alpha = I_E/I_C$) to less than 0.05. This feature of QMOS inputs permits proper logic operation in the presence of transients and also allows high to low voltage translation via series input resistors. The typical value of $\alpha$ for QMOS ICs is 0.001. Figure 13 illustrates how control of $\alpha$ in QMOS devices provides for safe conversion of 12V control logic levels to 5V HC system logic simply by insertion of a 100kΩ resistor in each input. The only disadvantage is that logic signals are delayed by 1μs to 2μs and therefore, this scheme works well only with rather slow 12V control logic as for example, in automotive applications. When the input diodes are used as clamps for logic level translation, the input current should be kept to 2mA or less.




$$I_I = \frac{6.3V}{100k\Omega} = 63\mu A$$

$$I_O = \alpha I_I = 0.05 \times 63\mu A = 3.15\mu A$$

$$V_{IL(B)} = 3.15\mu A \times 100k\Omega = 0.315V$$

$$V_{IL}MAX\,(SPEC) = 1.5V$$

NOISE MARGIN = 1.5V − 0.315V = 1.2V APPROX

FIGURE 13. 12V TO 5V LOGIC LEVEL CONVERSION AT HC INPUTS USING 100KΩ SERIES RESISTORS

**Input-Voltage Considerations and Maximum Forward-Diode Input Current Limits**

As a general rule, CMOS logic devices employing input clamp diodes (Figure 9) to minimize ESD effects should be operated between the power supply rails. If the input series polysilicon resistor shown in Figure 9 is not considered, then the rule is: $-0.5V \le V_{IN} \le (V_{CC} + 0.5V)$.

This rule is the industry standard (JEDEC Std. No. 7) and is intended to keep users from damaging devices because the devices of some HC/HCT device manufacturers do not have the built-in input series polysilicon resistor. Harris HC/HCT data sheets continue to show the conservative rating established by JEDEC. However, Harris HC/HCT device inputs are capable of meeting the following rating:
$-1.5V \le V_{IN} \le V_{CC} + 1.5V$.

Furthermore, Harris devices, except for special cases such as transceivers and analog switches or multiplexer signal inputs, can reliably operate with the ±1.5V rule without logic errors. Beyond ±1.5V, maximum forward current poses a second limitation with respect to the $V_{CC}$ and GND rail. This QMOS and JEDEC rating is ±20mA of transient current maximum forced into inputs or outputs.

## Latch-Up

### Definition

Latch-up within CMOS IC structures may be initiated or triggered by voltage overshoot or undershoot at inputs, outputs, or supply terminals. A high transient voltage or current at any one or combination of these terminals may initiate turn-on of an SCR-type 4-layer diode parasitic bipolar device, as shown in the simplified diagram of Figure 14. This parasitic structure, when triggered on, keeps the supply voltage below the $V_{CC}$ voltage and thus permits a high supply current of several hundred mA to flow (see Figure 14). The resistor values of $r_C$, $r_{BB}{}^{-1}$, $r_{BB}{}^{-2}$ are dependent on circuit layout geometry and p+ and n+ doping levels.

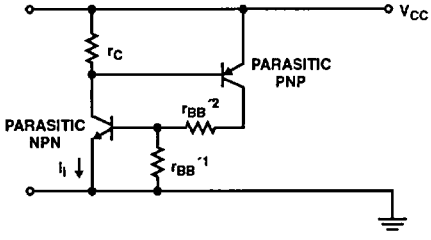



FIGURE 14. SIMPLIFIED DIAGRAM OF CMOS 4-LAYER DIODE STRUCTURE

The lower the value of these resistors, the less voltage drop that will occur. A much higher trigger current, therefore, will be required to induce turn on of the SCR structure shown in Figure 14.

Also important are established layout rules and process parameters that minimize the current gain (Beta) of the parasitic NPN and PNP transistors shown in Figure 14.

### Latch-Up Capability

The trigger current that could potentially trigger latch-up of QMOS ICs is typically ±80mA at any input or output terminal. Measurements are made at all terminals (see next section for preferred measurement technique), so that these terminals have a minimum acceptable latch current of ±40mA. The absolute maximum rating in the QMOS data sheet and in the industry JEDEC Standard No. 7 is ±20mA. The possibility for transient currents in applications are more likely to appear at input terminals where interfaces could cause voltage transients. The voltage required to induce the ±40mA measured capability and the ±80mA typical capability of QMOS ICs as illustrated in Figure 15, is established by the QMOS built-in 120Ω minimum current-limiting polysilicon resistor at logic inputs.

Equations:

$V_T = I_T R + V_D + V_{CC}$
$-V_T = -I_T R - V_D$

$R = 120\Omega$
$V_D = 0.7V$
$V_{CC} = 4.5V$

Values:

$V_T = 40mA \times 0.12K\Omega + 0.7V + 4.5V = 10V$ Min
$V_T = 80mA \times 0.12K\Omega + 0.7V + 4.5V = 14.8V$ Typ
$-V_T = -40mA \times 0.12K\Omega - 0.7V = -5.2V$ Min
$-V_T = -80mA \times 0.12K\Omega - 0.7V = -10.3V$ Typ

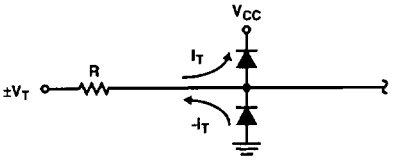



FIGURE 15. INPUT LATCH TRANSIENT VOLTAGE DETERMINATION

As developed in Figure 15, the minimum and typical $\pm V_T$ transient input voltages required to induce either ±40mA or ±80mA are relatively large, and far greater than the transients induced in 5V systems where 2V or 3V of ringing transients can be induced via wiring inductance effects. This ±40mA QMOS capability is truly a "latch-up free" condition for operation in a 2V to 6V system. If transients are induced in a particular application beyond +10V/-5.2V, then the use of external series-limiting resistors are advised to keep transient currents below ±40mA. Another consideration is unused inputs. If unused QMOS inputs are tied to a $V_{CC}$ of +5.5V and the $V_{CC}$ of the QMOS IC is temporarily grounded, for example, in a 2-power supply system, or when PC cards are replaced with power on, no possibility of latch-up will exist because the input current will be limited to ±40mA via the built-in 120Ω polysilicon series resistor.

### Measuring Latch-Up Sensitivity

### Caution

The test methods that follow can damage devices if the following **precautions are not strictly observed**.

- Apply currents for 1ms Min to 5s Max.
- Limit power supply currents to 200mA.
- Allow a cool-down period between successive tests to be equal to or greater than the time that is required to apply trigger current.
- These tests may be safely adapted to bench-testing with meters or use of a curve tracer.

1. Static Input or Output Triggering for Latch-up

$V_{CC}$ Supply to 200mA

For input triggering, connect other inputs to $V_{CC}$ or GND

All valid logic conditions are subject to test.

For Output Triggering (Figure 16C and Figure 16D)

- $-I_O$ - Active Outputs Must Be Set Low
- $+I_O$ - Active Outputs Must Be Set High
- Three-State Outputs - Also Set Output To High Impedance State

Apply trigger current first (Figure 17)

- Apply $\pm I_I$ or $\pm I_O$ (Figure 16)
- Raise $V_{CC}$ to $\pm V_{CC}$ Max
- After the Trigger Duration, Reduce Trigger Current to Zero
- If $I_{CC}$ is Less than Its Quiescent Value, the Device is not Latched.

If the quiescent value of $I_{CC}$ is out of specification, the input and output structure should be electrically checked to determine if the I/O circuitry is damaged and latch-up did not occur. Further device analysis may be required to verify if latch-up did indeed occur.

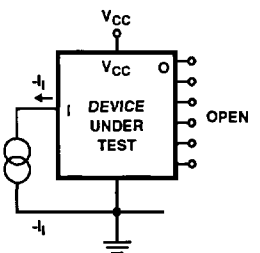



FIGURE 16A.

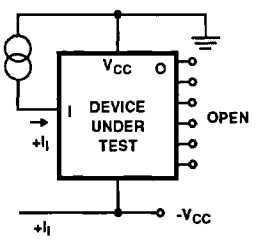



FIGURE 16B.

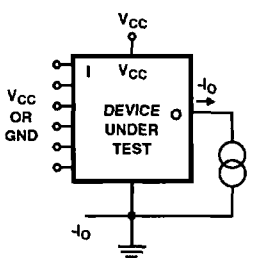



FIGURE 16C.

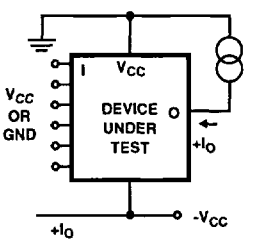



FIGURE 16D.

FIGURE 16. TEST SET-UP FOR POSITIVE AND NEGATIVE TRIGGER CURRENT

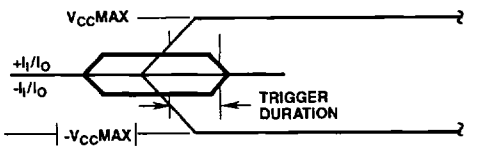



FIGURE 17. LATCH TEST WAVEFORMS

2. $V_{CC}$ Triggered Latch-Up Test by Over-Voltage on $V_{CC}$ (Figure 18)

Latch-up can occur if the voltage of the power supply is raised above the absolute maximum supply voltage rating.

Apply a $V_{CC}$ over-voltage of 2X $V_{CC}$ Max referenced to GND using a 100mA limited supply.

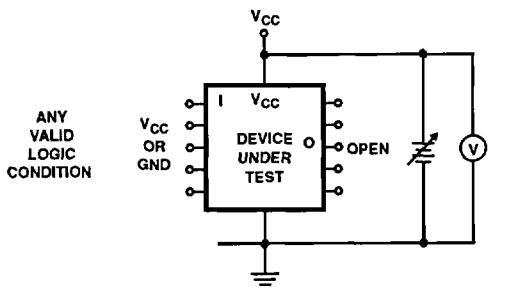
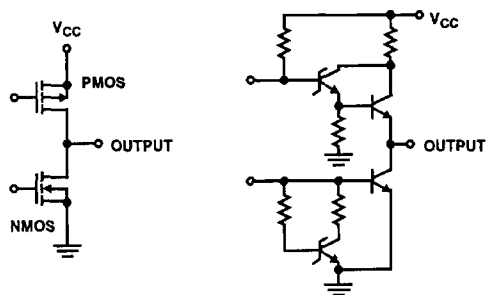



FIGURE 18. TEST SET-UP FOR $V_{CC}$ OVER-VOLTAGE LATCH TRIGGER

Measure the $V_{CC}$ voltage. If it is less than $V_{CC}$ Max, the part has latched.

## Output Characteristics

QMOS outputs make use of a complementary symmetry transistor configuration, which is different from the LSTTL totem-pole output; both outputs are shown in Figure 19. QMOS outputs meet the voltage level requirements necessary to interface to QMOS inputs, and the drive and current requirements needed to interface to bipolar inputs; i.e., TTL, LS, ALS, AS, FAST, etc.




A. CMOS OUITPUT B. LSTTL OUTPUT

FIGURE 19. COMPARISON OF HC/HCT (A.) AND LSTTL (B.)

The outputs of the QMOS devices are classified into two categories: standard and bus drive. The two outputs differ in the output transistor widths needed to meet JEDEC standard drive and current requirements. Both standard outputs and bus drive outputs may be active (two-state) or three-state with a high-impedance mode added and where both the PMOS and NMOS transistors are off. Another type of QMOS output is the open-drain output of the HC/HCT 03 Quad NAND gate shown in Figure 20. This output has no intrinsic or added diode connected to $V_{CC}$ at the output. The output of this device may be connected to an external load terminated at up to 10V. Thus, outputs can be pulled up above a nominal 5V supply for up-level voltage conversion.

The HC/HCT03 is the only QMOS gate type whose outputs can be used for a "wired OR" arrangement.

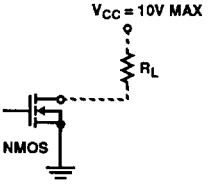



**FIGURE 20. HC/HCT 03 OUTPUT CIRCUIT**

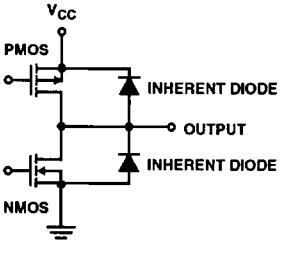



**FIGURE 21. INHERENT DIODES PROTECTING HC/HCT OUTPUTS**

### Output Protection

The outputs in a QMOS device are protected from ESD damage by diodes. Figure 21 shows these diodes. These intrinsic diodes are effective because of the large geometries (widths) of the output transistors. These diodes are the drain to n-substrate junction of the p device and the drain to p-well junction of the n device. This network provides protection to voltage levels typically greater than 3kV in all ESD discharge modes pertaining to the output (see Figure 10).

### Output Currents

QMOS outputs are specified for both CMOS and LSTTL loads. CMOS inputs are voltage sensitive and the only current is leakage current. The output voltage test for CMOS interfacing is specified for $I_O$ at ±20µA (20 CMOS loads). The outputs are also specified at $I_O$ = 4mA (10 LSTTL loads) and 6mA (15 LSTTL loads) for standard and bus-drive outputs, respectively. The corresponding $V_{OL}$ Max and $V_{OH}$ Min for the outputs, are illustrated in Table 3.

The maximum current per output pin $I_O$ is ±25mA and ±35mA for standard and bus-drive outputs, respectively. This maximum current rating is specified when the outputs are in their active regions: $-0.5V < V_O < V_{CC} + 0.5V$. The maximum current rating per power pin, $V_{CC}$ or ground, is 50mA and 70mA, respectively, for standard or bus-drive outputs.

When the output voltage exceeds $V_{CC}$ or is below ground by greater than 500mV, the output protection diodes turn on and conduct current. The maximum diode transient current, $I_{OK}$, should not exceed ±40mA to avoid latch-up as described earlier.

**TABLE 3. OUTPUT DRIVE SPECIFICATIONS**

| | | TEST CONDITIONS/LIMITS ($V_{CC}$ 4.5V) | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | $I_O$ | +25°C | -40°C to +85°C | -55°C to +125°C | UNIT |
| High-Level Output Voltage | $V_{OH}$ Min | -20µA | 4.4 | 4.4 | 4.4 | V |
| | | -4mA | 3.98 | 3.84 | 3.7 | V |
| | | -6mA (Bus) | 3.98 | 3.84 | 3.7 | V |
| Low-Level Output Voltage | $V_{OL}$ Max | 20µA | 0.1 | 0.1 | 0.1 | V |
| | | 4mA | 0.26 | 0.33 | 0.4 | V |
| | | 6mA (Bus) | 0.26 | 0.33 | 0.4 | V |

### Output-Current and Interfacing Capability

A comparison of the output drive capabilities for QMOS with those of LSTTL is as follows:

LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This specification assures that the worst case low and high input thresholds will be met and the existing margins of noise immunity preserved.

QMOS capability is expressed as source/sink current at a specified output voltage. Since QMOS requires virtually no input current, the unit load concept does not apply.

With a specified output drive of 0.4mA at 0.4V, the QMOS to QMOS interface capability exceeds 1000ULs, and with a 20µA/0.1V specification, the QMOS capability is 20ULs. Each standard QMOS output has a drive capability of ten LSTTL loads and maintains a $V_{OL}$ of 0.4V over the full temperature range. Bus driver outputs can drive 15 LSTTL loads under the same conditions.

TABLE 4. COMPARISON OF OUTPUT DRIVE CAPABILITIES

| LS DEVICE | OUTPUT DRIVE | HC/HCT EQUIVALENT | OUTPUT TYPE | OUTPUT | DRIVE |
|---|---|---|---|---|---|
| 74LS00 | 4mA 10UL | 74HC00 | Standard | 4mA | 10UL |
| 74LS138 | 4mA 10UL | 74HC138 | Standard | 4mA | 10UL |
| 74LS245 | 12mA 30UL | 74HC245 | Bus | 6mA | 15UL |
| 74LS374 | 12mA 30UL | 74HC374 | Bus | 6mA | 15UL |

The output drive capabilities of QMOS expressed in LSTTL unit loads are shown in Table 4.

### Output Curves

Output current derating versus temperature is shown in Figure 22 and is valid for all types of output. Output source and sink drives at $V_{CC}$ = 2V, 4.5V, and 6V are given in Figure 23 to Figure 26 which show output currents versus output voltages. These curves indicate the typical output current at +25°C and minimum output currents that can be expected at +25°C, +85°C, and +125°C, and can also serve as a design aid in interface applications and for calculating transmission line effects on charging highly capacitive loads.

Note to Figure 22 to Figure 25: The expected minimum curves are included as an aid to equipment designers, and are tested only at the points indicated on device data sheets.

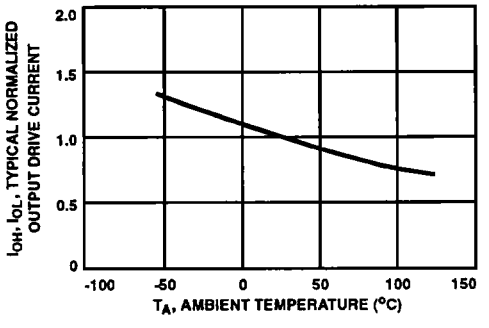



FIGURE 22. OUTPUT CURRENT DERATING vs AMBIENT TEMPERATURE

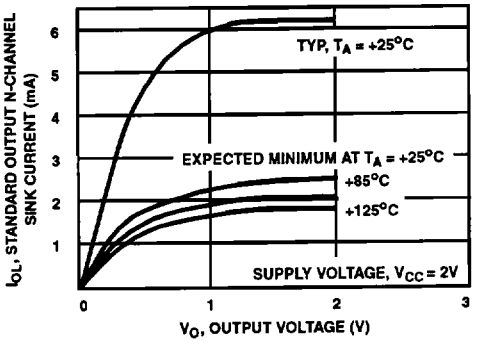



FIGURE 23A.

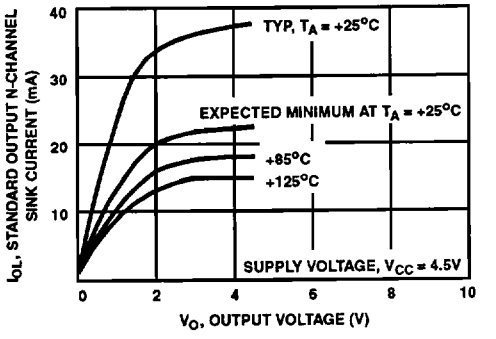



FIGURE 23B.

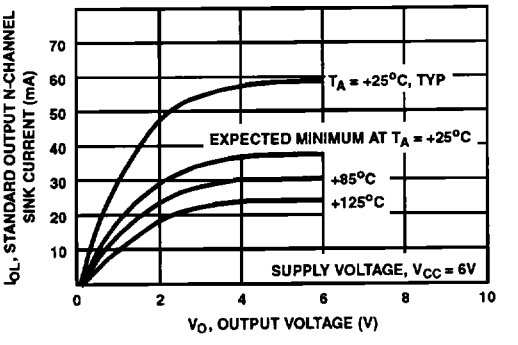



FIGURE 23C.

FIGURE 23. STANDARD OUTPUT N-CHANNEL SINK CURRENT ($I_{OL}$) FOR $V_{CC}$ = 2V, 4.5V, AND 6V

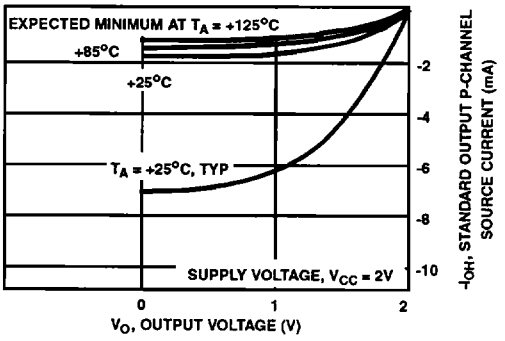



FIGURE 24A.

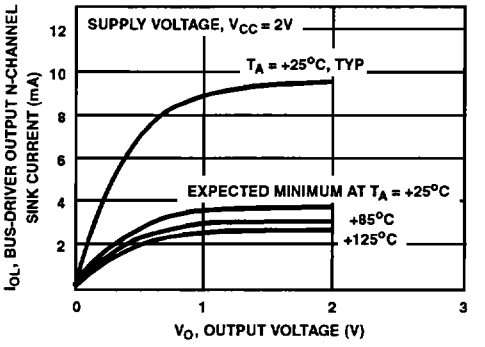



FIGURE 25A.

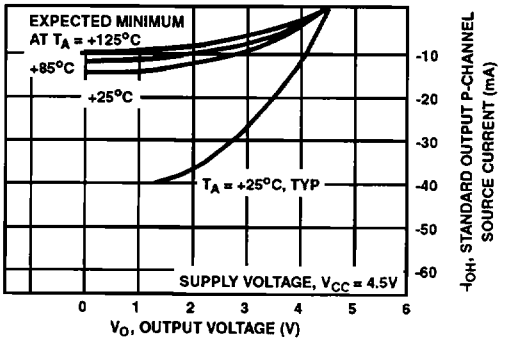



FIGURE 24B.

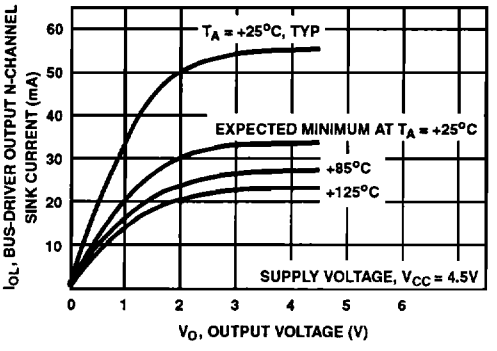



FIGURE 25B.

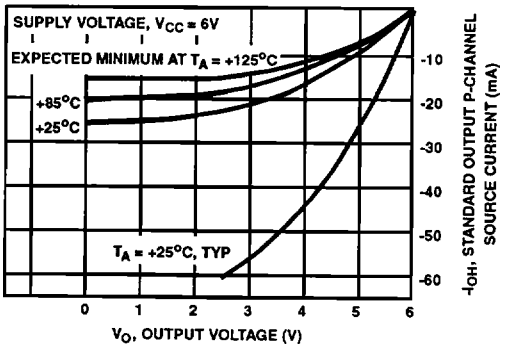



FIGURE 24C.

FIGURE 24. STANDARD OUTPUT P-CHANNEL SOURCE CURRENT ($-I_{OH}$) FOR $V_{CC}$ = 2V, 4.5V, AND 6V

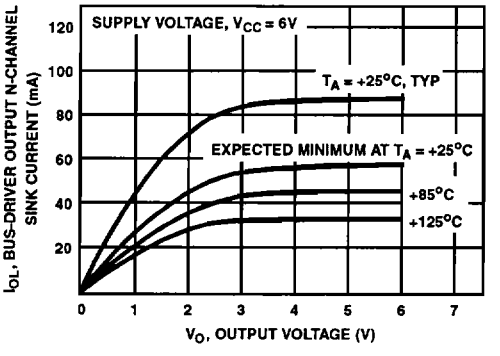



FIGURE 25C.

FIGURE 25. BUS-DRIVER OUTPUT N-CHANNEL SINK CURRENT ($I_{OL}$) FOR $V_{CC}$ = 2V, 4.5V, AND 6V

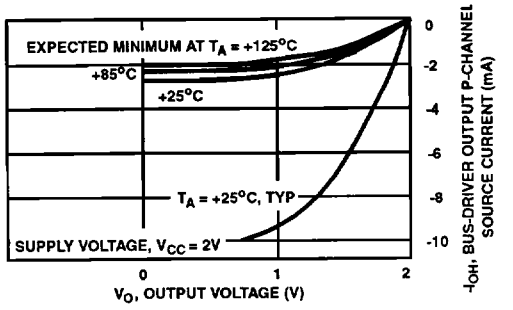



FIGURE 26A.

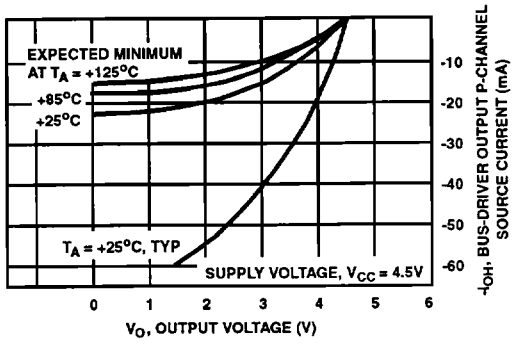



FIGURE 26B.

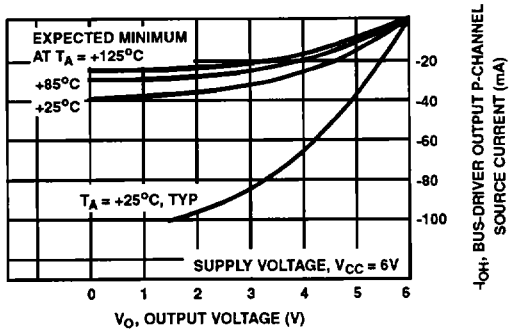



FIGURE 26C.

FIGURE 26. BUS-DRIVER OUTPUT P-CHANNEL SOURCE CURRENT ($-I_{OH}$) FOR $V_{CC}$ = 2V, 4.5V, AND 6V

## Dynamic Characteristics

The Harris QMOS family is designed to meet the dynamic switching speeds and operating frequency of low power Schottky TTL. When compared to metal gate CD4000 and 74C series CMOS, QMOS shows a 10 to 1 improvement in AC performance. QMOS types feature balanced propagation delays and transition times specified at conditions similar to LSTTL at a nominal $V_{CC}$ = 5V and $C_L$ = 15pF, so that the user can relate to the equivalent LSTTL specification. Switching speed limits for QMOS are given at a more realistic $V_{CC}$ of 4.5V and a $C_L$ of 50pF. Test waveforms for the HC and HCT types are shown at the end of this section.

### Capacitive Load ($C_L$) Determination

The external capacitive loading ($C_L$) seen by a QMOS output is required to calculate the propagation delay and operating power dissipation of a logic function. The three components of $C_L$ at a logic node are:

1. n $C_{IN}$ where n is the fanout.
2. m $C_{OUT}$ where m is the number of three-state outputs on a logic bus.
3. $C_{STRAY}$ which is the effective wiring and interconnect capacitance.

$$C_L = n\,C_{IN} + (m - 1)\,C_{OUT} + C_{STRAY} \quad \text{(EQ. 1)}$$

$C_{IN}$ is shown in Figure 27 for typical HCT and HC type inputs. Note that $C_{IN}$ has peak values at the respective switch points of HCT (1.4V) and HC (2.5V). Capacitance on either side of the peak is a summation of package, lead frame, reverse biased input diode, and CMOS gate-to-source/drain capacitance. The peak capacitance results from the Miller multiplication of C gate-to-drain in the high-gain linear transition region. The values of $C_{IN}$ that most typically represent the average loading effect are 4pF for HCT inputs and 3pF for HC inputs. $C_{IN}$ for HCT inputs is higher than that for HC inputs because of the required large gate-to-source/drain capacitance of the large NMOS device widths.

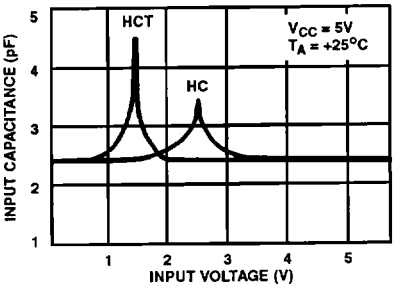



FIGURE 27. $C_{IN}$ AS A FUNCTION OF $V_{IN}$

Output capacitance ($C_{OUT}$) is typically 10pF for both HCT and HC-type bus-driver outputs when these versions are in their high-impedance state, the only state where $C_{OUT}$ loading is a factor.

The wiring and interconnect capacitance ($C_{STRAY}$) is determined by estimates of interconnect capacitance and wiring capacitance. These capacitances are highly variable because of differences in interwiring techniques. An often used high speed wiring technique utilizes strip line with 100Ω characteristic impedance. $C_{STRAY}$ in this case, is typically 20pF per foot. Capacitances of sockets and connectors are available from their manufacturers.

In a bus system, $C_{STRAY}$ is the largest single $C_L$ component, as the following example illustrates:

Bus Specification:

No. of fanouts (n) = 10

No. of bus drivers (m) = 5

From Equation 1:

$C_L$ = 10 x 2.5pF + 4 x 10pF + 7 x 20pF
= 25pF + 40pF +140pF = 205pF

### Propagation Delays vs Supply Voltage

The dynamic performance of a CMOS device is related to its drain characteristics. The drain characteristics are related to the thresholds and gate-to-source voltage potential, $V_{GS}$. The $V_{GS}$ voltage is equal to the power supply voltage, $V_{CC}$. Therefore, a reduction in $V_{CC}$ adversely affects the drain characteristics which, in turn increases the propagation delays. An increase in $V_{CC}$ decreases the propagation delays.

The voltage range of the HCT version is 5V ± 10%. Over this range, the effects of propagation delays on performance are minimal. However, the voltage range recommended for the HC version is 2V to 6V. Over such a wide range, the effects on dynamic performance of propagation delay and operating frequency (Figure 28) are appreciable.

### Propagation Delay vs Capacitance

Propagation delay vs capacitance for the Harris family of HC/HCT types is similar to that of LSTTL types which HC/HCT types may replace in present or new applications.

To determine a propagation delay maximum limit at any value of capacitive loading up to 300pF, the following equation is used:

$$t_{PD}(C_L) = t_{PD}(50pF) + t(C_L)\,[C_L - 50pF] \qquad \text{(EQ. 2)}$$

Where:

$t_{PD}(C_L)$ = maximum propagation delay at the desired $C_L$

$t_{PD}(50pF)$ = maximum propagation delay from device data sheet at 2V, 4.5V, or 6V (See Table 5).

$t(C_L)$ Maximum (ns/pF) multiplying factor from the following table:

| | $t(C_L)$ (ns/pF) | |
|---|---|---|
| $V_{CC}$ | STD. OUTPUT | BUS OUTPUT |
| 2V | 0.272 | 0.187 |
| 4.5V | 0.102 | 0.068 |
| 6V | 0.082 | 0.056 |

### Propagation Delay vs Temperature

Because an increase in temperature causes a decrease in electron and hole mobilities, a temperature increase will cause an increase in propagation delays. Correspondingly, AC performance improves with lower temperatures. Typically, speeds derate linearly from 25°C at about -0.3%/°C.

The propagation delay, therefore, can be computed at any temperature between -55°C and +125°C by using the following relationship:

$$t_{PD}(T) = t_{PD}(25°C)\,(1 + [(T(°C)-25)\,(0.003ns/°C)]) \qquad \text{(EQ. 3)}$$

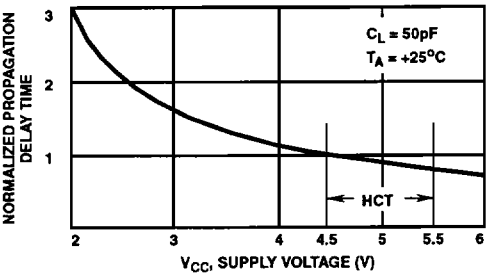



FIGURE 28A.

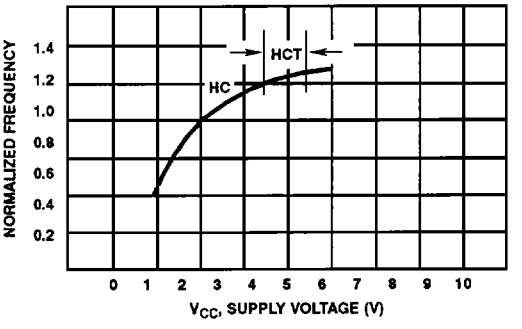



FIGURE 28B.

FIGURE 28. TYPICAL SWITCHING SPEED CHARACTERISTIC vs SUPPLY VOLTAGE NORMALIZED TO 4.5V

### Output Transition Times

Table 5 shows the Harris standard and maximum ratings for output transition times applicable to all standard and bus-driver outputs. Typical values are approximately 1/2 the maximum values. Practical unspecified minimum values are 1/4 the limit values.

TABLE 5. OUTPUT TRANSITION TIME LIMITS FOR $C_L$ = 50pF

| | | MAXIMUM OUTPUT TRANSITION TIMES (ns) | | |
|---|---|---|---|---|
| OUTPUT | $V_{CC}$ (V) | $T_A$ = +25°C | $T_A$ = +85°C | $T_A$ = +125°C |
| Standard | 2 | 75 | 95 | 110 |
| | 4.5 (Note 1) | 15 | 19 | 22 |
| | 6 | 13 | 16 | 19 |
| Bus Driver | 2 | 60 | 75 | 90 |
| | 4.5 (Note 1) | 12 | 15 | 18 |
| | 6 | 10 | 13 | 15 |

NOTE:

1. Specification for CD54HCT and CD74HCT types.

### Output Transition Time vs Capacitive Loading

To determine the maximum output transition time on any capacitive loading up to 300pF, the following formula is used:

$$t_T(C_L) = t_T(50pF) + t'(C_L)\,[C_L - 50pF] \qquad \text{(EQ. 4)}$$

Where:

$t_T(C_L)$ = Maximum Transition Time at the Desired $C_L$

$t_T(50pF)$ Limit at 2V, 4.5V, or 6V(Table 5)

$t_TN(C_L)$ = (ns/pF) Multiplying Factor from the Following Table:

| | $t'(C_L)$(ns/pF) | |
|---|---|---|
| $V_{CC}$ | STD OUTPUT | BUS OUTPUT |
| 2V | 0.544 | 0.374 |
| 4.5V | 0.204 | 0.131 |
| 6V | 0.170 | 0.110 |

**Transition Time vs Temperature**

Transition time at HC/HCT outputs typically changes by -0.3%/°C. Equation 3 used to compute increase in propagation delay with temperature (see above), can also be used to compute transition time at any temperature by simply substituting $t_T$ for $t_{PD}$.

**Clock Pulse Considerations**

All HC/HCT flip-flops and counters contain master-slave devices with level sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of voltage threshold levels for clocking is an improvement over AC-coupled clock inputs, however, these levels make these devices somewhat sensitive to clock-edge rates. The threshold level is typically 50% of $V_{CC}$ for HC devices, and 28% of $V_{CC}$ for HCT devices (1.4V at $V_{CC}$ = 5V). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground. This condition results in a noise transient that is equal to the algebraic sum of internal and external ground plane noise. When a number of loaded outputs change at the same time, it is possible for the chip ground reference level (and therefore, the clock reference level) to rise by as much as 500mV. If the clock input of a positive-edge triggered device is at or near its threshold during a noise transient period, multiple triggering can occur. To prevent this condition, the rise and fall times of the clock inputs should be less than 500ns at $V_{CC}$ 4.5V, the data sheet maximum value.

In the HC/HCT family, several flip-flops have a Schmitt-trigger circuit at their clock input. This circuit increases the maximum permissible rise/fall time on the clock waveform. The Harris flip-flop types HC/HCT 73, 74,107,109 and 112, have special Schmitt-trigger circuits which increase their tolerance to slow rise/fall times and to high levels of ground noise.

Maximum permissible input-clock pulse-frequency ratings on each clocked device type data sheet requires a 50% duty cycle input clock. At these rated frequencies, the outputs will swing rail-to-rail, assuming no DC load on the outputs. This feature is a very conservative and highly reliable method of rating clock-input-frequency limits which for HC/HCT devices, equal or exceed LSTTL ratings.

## Power Consumption

The power consumption of a HC/HCT device is composed of two components: one static, the other dynamic. The static component is the result of quiescent current caused principally by reverse junction leakage. The dynamic component results from transient currents required to charge and discharge the capacitive loads on logic elements, that is, transient currents caused by internal and external capacitance, and transients resulting from the overlapping of active p and n transistors. Internal chip power consumption is represented by the value $C_{PD}$.

Two equations are used to compute the total IC power consumption. The first, Equation A is applicable to an HC or HCT device when the inputs are driven from GND to $V_{CC}$ (rail-to-rail), as follows:

$$P = P_{DC} + P_{AC}$$

$$P = I_{CC}V_{CC} + C_{PD}V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_O \quad \text{(EQ. A)}$$

Where:

$I_{CC}$ = Quiescent Current (Ref. Table 6)

$V_{CC}$ = Supply Voltage

$f_i$ = Input Frequency

$f_O$ = Output Frequency

$C_{PD}$ = Device Equivalent Capacitance

$C_L$ = Load Capacitance

The second, Equation B is applicable only to an HCT device where specific input pins are driven at LSTTL levels defined as $V_{IN} = V_{CC} - 2.1V$:

$$P = P_{DC} + P_{AC}$$

$$P = I_{CC}V_{CC} + \Delta I_{CC}V_{CC}D + C_{PD}V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_O \quad \text{(EQ. B)}$$

Where:

$\Delta I_{CC}$ = Added DC Current when $V_{IN} = V_{CC} - 2.1V$ (LSTTL level)

D = Duty Cycle of Clock (% of Time HIGH)

**TABLE 6. TEMPERATURE - DEPENDENT RATINGS**

| | LIMIT | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C | | -40°C TO +85°C | -55°C TO +125°C | |
| | $V_{IN}$ | $V_{CC}$ | TYP | MAX | 74HCT MAX | 54HCT MAX | UNITS |
| $\Delta I_{CC}$ Additive DC Current Per Input Pin (1-Unit) | $V_{CC}$ - 2.1V | 4.5V to 5.5V | 100 | 360 | 450 | 490 | µA |

TABLE 7. HC/HCT AND LSTTL MAXIMUM QUIESCENT CURRENT AT $V_{CC}$ = 5V

| DEVICE COMPLEXITY | HC/HCT TYPICAL 25°C | HC/HCT LIMIT 25°C | HC/HCT LIMIT 85°C | HC/HCT LIMIT 125°C | LSTTL 125°C |
|---|---|---|---|---|---|
| SSI | 2nA | 2μA | 20μA | 40μA | 4.4mA |
| FF | 4nA | 4μA | 40μA | 80μA | 8mA |
| MSI | 8nA | 8μA | 80μA | 160μA | 10mA to 95mA |

The temperature dependent ratings for $I_{CC}$ are given in the table below:

| HCT LOAD TABLE BY TYPE SHOWN ON EACH DATA SHEET | | |
|---|---|---|
| | Input | Unit Multiplier |
| Example: | All | X0.6 |

The dynamic power due to outputs is the sum of the AC power at each output. The user must independently determine the $C_L$ and the average frequency at each output. The latter requires estimating the average frequency of data nodes in a logic system. For example, for HC/HCT counter types, each output is inherently operating at different frequencies.

The source of the $C_{PD}$ or device equivalent-power-dissipation capacitance is made up of 2 sources of internal device power consumption:

1. Power consumed by charge and discharge of internal device capacitance.
2. Power consumed through current switching transients.

Figure 29 illustrates the typical $I_{CC}$ vs $V_{IN}$ characteristic of HC type devices. Note that when $V_{IN}$ = 0.1V or ($V_{CC}$ -0.1V), zero current flows. Thus, no $\Delta I_{CC}$ component is required for computing the power consumption of HC device types. However, the transient switching components of an IC consume power and are a part of the $C_{PD}$ value.

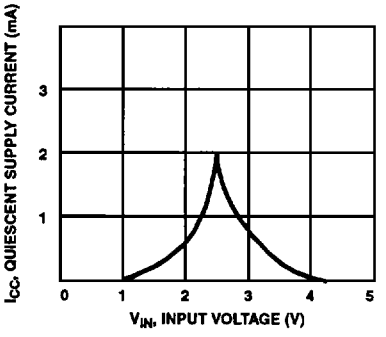



FIGURE 29. $I_{CC}$ vs $V_{IN}$ FOR HARRIS HC TYPES

Figure 30 illustrates the typical $I_{CC}$ vs $V_{IN}$ characteristic of HCT type devices. Again, if input voltages are 0.1V or ($V_{CC}$ -0.1V), no $\Delta I_{CC}$ value exists. Also for $V_{IN}$ = 0.4V, $\Delta I_{CC}$ is zero. If $V_{IN}$, however, is an LSTTL logic high level of ($V_{CC}$ -2.1V) or approximately 3V for $V_{CC}$ = 5V, then significant $\Delta I_{CC}$ does exit and is indicated in Equation B as the $\Delta I_{CC}$ component.

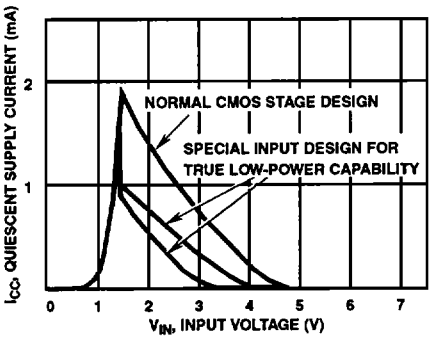



FIGURE 30. $I_{CC}$ vs $V_{IN}$ FOR HCT TYPES

The special input design of Harris HCT types greatly reduces the value of $\Delta I_{CC}$ such that the added power is very small; for example, Harris HCT power is minimal compared to LSTTL power. If this special input circuitry were not used, the $\Delta I_{CC}$ values would be relatively high as demonstrated by the dashed line in Figure 30, and the HCT type would not have very low power when compared to LSTTL.

NOTE: The low value of $I_{CC}$ is due to a special input design that provides a true low-power HCT capability.

Because appreciable current flows during device input switching as shown in Figure 29 and Figure 30, it is important to maintain fast input rise and fall times. The JEDEC and Harris recommended maximum input rise and fall times are:

1000ns for $V_{CC}$ = 2V; 500ns for $V_{CC}$ = 4.5V; 400ns for $V_{CC}$ = 6V

Since maximum output transition times are 15ns for the standard logic types and 12ns for bus drivers, a designer must only be concerned with exceeding the rise and fall times shown above for interfacing or linear mode operation in applications such as RC oscillators, crystal oscillators, and amplifiers using the HCU04 types.

When Schmitt-trigger types HC/HCT14 and 132 are used for either shaping up slow signals or as RC oscillators, power is increased due to prolonged through-current. For further information on oscillators and their power consumption, refer to Application Note AN7337, "Astable Multivibrator Design Using High Speed QMOS IC's". See Section 8, "How to Use AnswerFAX", of this selection guide.

The adverse effects of power transitions is another reason to maintain input rise and fall times under the recommended limits. Longer transitions may cause oscillations of logic circuits (and hence, logic errors) or premature triggering depending on system $V_{CC}$ and GND noise, which are amplified when input signals hover near the switching voltages illustrated in Figure 29 and Figure 30. To reduce the effects of slower transitions, the use of Schmitt-trigger types is recommended.

### Comparison to LSTTL Power

The dynamic power consumption of HC/HCT devices is frequency dependent, but it should be noted that LSTTL power consumption is also frequency dependent at frequencies greater than 1MHz. At frequencies less than 1MHz, the dynamic component is negligible compared to the static

component. The average power consumption of HC/HCT and LSTTL equivalents is illustrated in Figure 31 for four device types. Because all of the functions in a multi-functional LSTTL device are biased when power is applied, the HC/HCT device characteristics are plotted for a single function and for the total package for the purposes of comparison.

Some observations from Figure 31 are:

1. For SSI gate types, the HC/HCT power approaches LSTTL power at about 1MHz.
2. For higher complexity types such as the Harris HC/ HCT 138 3-of-8 line decoder/demultiplexer shown in Figure 31C, HC/HCT power approaches LSTTL power at above 10MHz.
3. Figure 31 implies continuous operation at the frequencies shown, however, most practical applications of logic in microcomputer systems have variable operation or data/address signal rates. The average operating frequency is much below the peak operating frequency particularly in the 100KHz region where power savings over LSTTL are several orders of magnitude.

## Power-Supply Considerations

### Power-Supply Voltages

The Harris HC and HCU versions have a power supply range of 2V to 6V; the absolute maximum voltage rating is 7V. The ability to use Harris HC types with a 2V supply makes these devices particularly useful in battery-operated equipment, especially systems including memories that feature 2V standby operation. The absolute maximum supply or ground current, per pin, is ±50mA for types with standard output drive, and ±70mA for types with bus driver outputs.

The operating supply voltage range for Harris CD74HCT types is 4.5V to 5.5V, 5V ± 10%. These figures indicate that there is more tolerance in the regulation of the low current system supply than is the case with other technologies. The maximum voltage indicated for HC and HCU versions also applies to HCT versions. The advantages of using HC/HCT/HCU with its wider voltage supply range are illustrated in Figure 32.



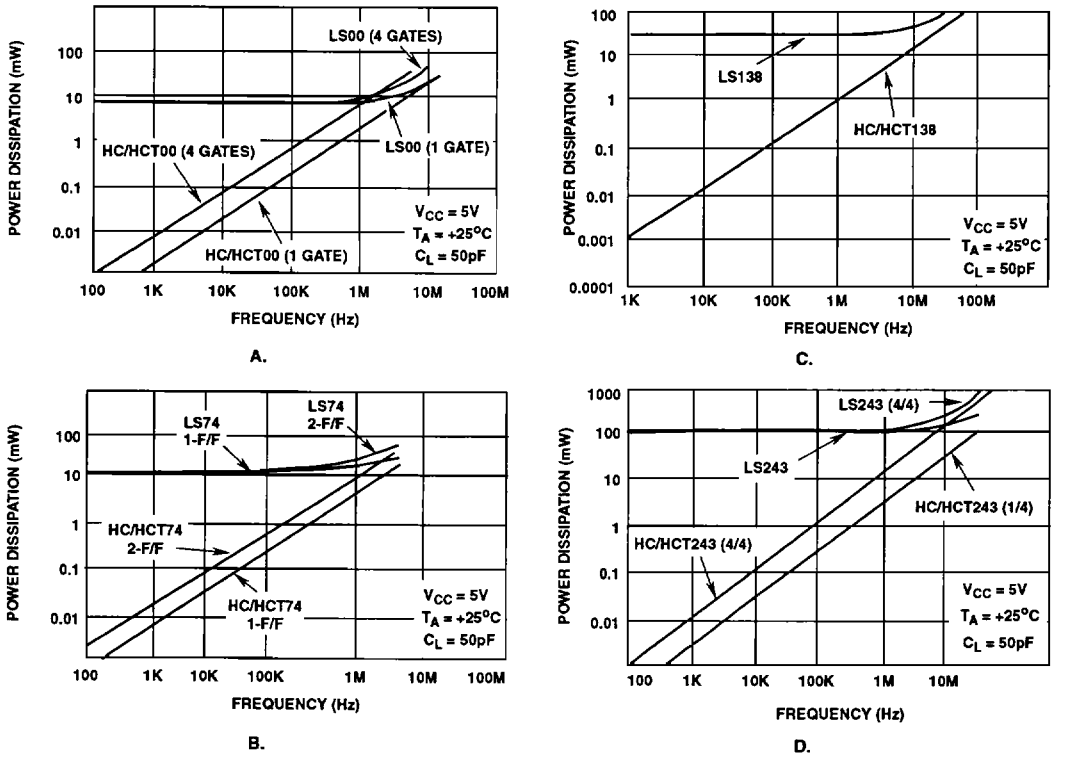



FIGURE 31. POWER vs FREQUENCY GRAPHS FOR (A.) LS/HC/HCT00; (B.) LS/HC/HCT74; (C.) LS/HC/HCT138; (D.) LS/HC/HCT243

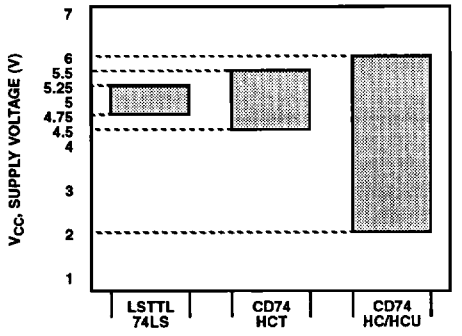



**FIGURE 32. POWER SUPPLY RANGES FOR CD74HCT, CD74HC AND CD74HCU VERSIONS OF THE HARRIS FAMILY OF DEVICES AND 74LS SERIES TYPES.**

### Battery Back-Up

Battery back-up can be easily implemented in systems of Harris HC/HCU devices. An example of this arrangement is shown in Figure 33. The minimum battery voltage required is only 2V plus one diode drop.

In the example, Harris High-to-Low Level Shifters (HC4049 or HC4050) are used to prevent the flow of positive input currents into the system due to input voltage levels greater than one diode drop above $V_{CC}$. If the circuit design is such that input voltages can exceed $V_{CC}$, then external resistors should be included to limit input currents to 2mA. External resistors may also be necessary in the output circuits to limit currents to 2mA, if the output can be pulled above $V_{CC}$ or below GND. These currents are due to inherent $V_{CC}$/GND diodes that are present in all outputs, including three-state outputs.

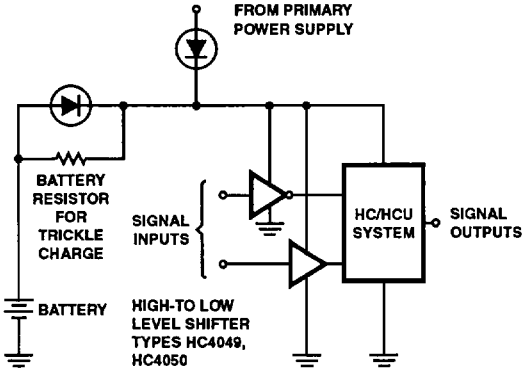



**FIGURE 33. EXAMPLE OF AN HC/HCU SYSTEM WITH BATTERY BACK-UP**

### Power Supply Regulation and Decoupling

The wide power supply range of 2V to 6V may suggest that voltage regulation is not necessary, but it must be realized that a changing supply voltage affects system speed, noise immunity and power consumption. Because noise immunity, and even the correct operation of the circuit, can be affected by noise spikes on the supply lines, therefore, matched decoupling is always necessary in dynamic systems.

Both HC and HCT types have the same power supply regulation and decoupling requirement. The best method of minimizing spiking on the supply lines is by implementing good power supply and ground bussing and having low AC impedances from the $V_{CC}$ and GND pins of each device. Because the minimum value of a decoupling capacitor depends on the voltage spikes that can be allowed, it is a general rule to restrict ground and $V_{CC}$ noise peaks to 400mV. A local voltage regulator on the printed-circuit board can be decoupled using an electrolytic capacitor of 10µF to 50µF.

Localized decoupling of devices can be provided by a 22nF capacitor for every two to five packages, and a 1µF tantalum capacitor for every ten packages. The $V_{CC}$ line of bus driver circuits and level sensitive devices can be effectively decoupled from instantaneous loads by a 22nF ceramic capacitor connected as close to the package as possible.

A practical example of determining the value of a decoupling capacitor is as follows: assume that a buffer output sees a 100Ω dynamic load and that the output low-to-high transition is 5V, then the current demand is 50mA per output. For an octal buffer, the current demand would be 0.4A per package, in approximately 6nS.

The following formula can also be used to determine the value of a decoupling capacitor:

The term $Q = CV$ is differentiated to obtain $\frac{\Delta Q}{\Delta t} = C\frac{\Delta V}{\Delta t}$

Since $\frac{\Delta Q}{\Delta t} = I$, the equation becomes $I = C\frac{\Delta V}{\Delta t}$

Hence: $C = \frac{I\Delta t}{\Delta V}$

For an octal buffer, assuming a change in $V_{CC}$ or GND of 0.4V, then:

$$C = \frac{0.4A \times 6 \times 10^{-9}S}{0.4V} = 6 \times 10^{-9}F = 6nF$$

For further information on power supply regulation and decoupling, refer to Application Note AN7329, "Power-Supply Distribution and Decoupling for QMOS High Speed IC's."

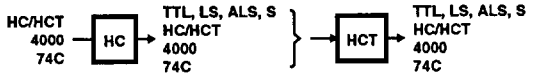
## Interfacing

Because of the characteristics of the CMOS output, the HC/HCT family is very versatile in interfacing between different logic families. This capability including the corresponding fanout is illustrated in Figure 34.

Note that the fanout to CMOS devices is limited only by the input rise and fall times, which are dependent on the capacitive loading, $C_L$. This dependence can be computed by the following relationship:

$$t_R, t_F = 2.2RC_L \qquad \text{(EQ. 5)}$$

Where R is the impedance of the output.




| FANOUT FROM | TO CORRESPONDING LOGIC FAMILIES | | | | | |
|---|---|---|---|---|---|---|
| HC/HCT | TTL | LS | ALS | FAST | S/AS | 4000, 74C |
| Standard Types | 2 | 10 | 20 | 6 | 2 | See Text |
| Bus Drivers | 3 | 15 | 30 | 10 | 3 | |

**FIGURE 34. HC/HCT INTERFACING CAPABILITY AND CORRESPONDING FANOUT TO OTHER LOGIC FAMILIES**

Harris HC types cannot be driven from any of the TTL families because the TTL output voltage high, $V_{OH}$ Min, does not satisfy the HC input voltage high, $V_{IH}$ Min specification. The HCT types can be directly interfaced to the TTL families because the HCT input voltage high, $V_{IH}$ Min is less than the TTL output voltage high, $V_{OH}$ Min. To meet minimum $V_{IH}$ requirements, HC types can use a pull-up resistor as illustrated in Figure 35.

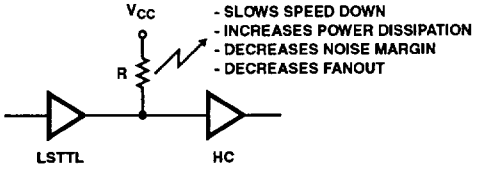



**FIGURE 35. USE OF PULL-UP RESISTOR TO INTERFACE TTL AND HC DEVICES.**

However, the use of a pull-up resistor will not give optimum performance because as noted in Figure 35, the resistor tends to slow down system speed, increase power dissipation, decrease noise margin, and decrease fanout.

For further information on interfacing, refer to Application Note AN7325, "Interfacing HC/HCT QMOS Logic with Other Families and Various Types of Loads." See Section 8, "How to use AnswerFAX", in this selection guide.

### Logic-Level Conversion

The HC/HCT family contains logic-level conversion types necessary to interface high-voltage logic levels (up to 15V common in control and automation systems) to low voltage levels (down to 2V) as shown in Figure 36.

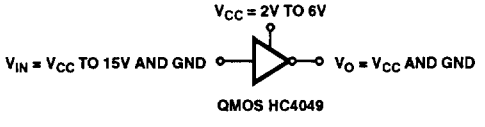



**FIGURE 36A. HEX INVERTING**

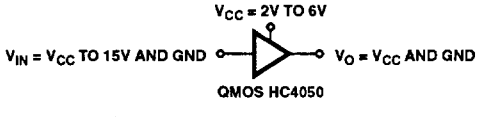



**FIGURE 36B. HEX NON-INVERTING**

**FIGURE. 36. HIGH-TO-LOW LOGIC LEVEL CONVERSION**

The Quad open-drain NAND gate (HC/HCT03) is used to convert from HC (2V to 6V) or HCT (TTL or CMOS) logic levels up to 10V output logic levels as shown in Figure 37. $R_L$ can be a very wide range of values. For design of this output interface, use the output NMOS transistor characteristics of Figure 23. The minimum value of $R_L$ is that necessary to keep the output current below the 25mA HC/HCT family maximum rating. A large value of $R_L$ will prolong the output rise time.

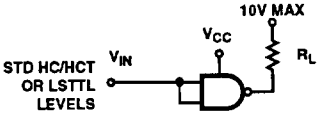



**FIGURE 37. LOW-TO-HIGH LOGIC LEVEL CONVERSION**

### System (Parallel) Clocking

When utilizing the HC/HCT family in synchronously clocked systems the following guidelines should be followed. Because of variations in switching points between devices, a slow clock edge could cause a logic error. If data in one of the synchronously clocked circuits changes before the switching point of the next sequential circuit is reached, a logic error will occur. This situation is illustrated in Figure 38.

$V_{S1}$ = Switching point, Device 1

$V_{S2}$ = Switching point, Device 2

$t_P$ = Propagation Delay

Because of variations in input threshold voltages among Harris HC-version devices, the maximum clock-pulse rise or fall time should adhere to the following relationship:

$$t_R, t_F Max < 2t_P Max \quad \text{(EQ. 6)}$$

In a system where HC, HCT, and TTL-type families are mixed, the maximum clock pulse rise or fall times should adhere to the following relationship:

$$t_R, t_F Max < t_P Max \quad \text{(EQ. 7)}$$

It is recommended that a Schmitt-trigger circuit be utilized if wave shaping is required.

The maximum rise or fall time into any Harris HC or HCT device must be limited to 1000ns, 500ns, and 400ns at 2V, 4.5V, and 6V, respectively. If these limits are exceeded, noise on the input or power supply may cause the outputs to oscillate during transition. This oscillation could cause logic errors and unnecessary power consumption.

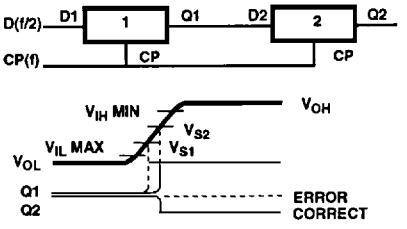



**FIGURE 38. RESULT OF CHANGING DATA IN ONE SYNCHONOUSLY CLOCKED CIRCUIT BEFORE THE SWITCHING POINT OF THE NEXT SEQUENTIAL CIRCUIT IS REACHED**

### Drop-In Replacement

The use of Harris HCT family devices make it unnecessary to sacrifice noise margins, speed, and quiescent power dissipation in constructing interfaces to achieve mixed technology designs. This performance is possible because HCT devices are TTL compatible and can directly replace LSTTL counterparts without the addition of pull-up resistors at the LSTTL outputs.

Fanout capabilities should be taken into account when an HCT device is used to replace a TTL part. TTL fanout is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fanout is determined by the ability of the outputs to sink current (a TTL input usually sources current). The outputs of HCT devices are classified in two categories: standard and bus driver. Table 8 shows the fanout for the different TTL families.

For further information on drop-in replacements, refer to Application Note AN7330, "Replacing LSTTL with QMOS High Speed Logic IC's". See Section 8, "How to Use AnswerFAX", in this selection guide.

The fanout values shown in Table 8 are derived at a voltage drop of maximum 0.4V ($V_{OL}$). In the "74" TTL series, an extended $V_{OL}$ value is often seen, e.g., 8mA at 0.5V voltage drop for LSTTL. If this value is used in determining the fanout of the TTL part, it can result in a higher fanout than is possible with QMOS. This condition can be resolved by replacing as many of the driven TTL parts as possible by HCT devices to reduce the sink current requirement (the HCT input current is negligible). Furthermore, the use of HCT devices results in a substantial reduction in power dissipation.

**TABLE 8. FANOUT OF HCT TO TTL ELEMENTS**

| HCT | TTL | LS | ALS | FAST | S AND AS |
|---|---|---|---|---|---|
| Standard | 2 | 10 | 20 | 6 | 2 |
| Bus-Driver | 3 | 15 | 30 | 10 | 3 |

Devices of the HCT family are power saving, virtually drop-in replacements for LSTTL parts. The total power consumed by a system depends largely on the number of gates switching at any time and on the switching frequency, but in most systems only about 30% of all circuits switch at the maximum system frequency; 70% operate at far lower rates. Thus, even in systems using ALS, AS, S and FAST, the HCT family can be used with consequent power savings and good reliability improvement in mixed technology designs.

### Conversion of LSTTL Test to HCT Test

A simplified technique to convert an LSTTL test program to one that properly tests an HCT type is explained in Application Note AN7323 "Modification of LSTTL Test Programs to Test HCT High Speed CMOS Logic IC's". See Section 8, "How to use AnswerFAX", in this selection guide.

## Bus Systems

Bus systems are commonly used in microcomputer applications. Harris CMOS devices are being increasingly used in these applications.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically noisy environments, battery stand-by requirements and sealed, gas-tight enclosures. QMOS bus systems, e.g., the proposed CMOS STD bus (a non-proprietary CMOS bus proposed standard) provides a low power solution to virtually all of these problems. In comparison with older bipolar digital IC Bus standards, QMOS bus systems offer superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

In order to optimize results with QMOS, particularly in circuits which communicate directly with the bus, the use of only HC devices is recommended, because HC QMOS optimizes input-signal noise immunity with HC QMOS a new low-power bus termination can be introduced (see Figure 39B) which, unlike the conventional high-current TTL bus termination of Figure 39A, draws no heavy DC current and is more suited to QMOS outputs. Both HC and HCT QMOS have the identical rail-to-rail output drive.

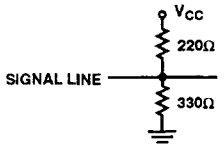



**FIGURE 39A. CONVENTIONAL TERMINATIONS FOR TTL BUSES 0.25W PER LINE OR 2W PER OCTAL DRIVE AND TERMINATION**

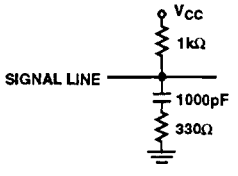



**FIGURE 39B. PROPOSED LOW-POWER TERMINATION FOR CMOS STD BUS EQUIVALENTS**

**FIGURE 39. BUS TERMINATIONS**

The wider supply voltage range of HC type QMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via the card edge-input protection circuit. Such pick-up can exceed the CMOS input current maximum ratings if the input current is not limited by a 10kΩ series resistor in the QMOS logic line. This series resistor will limit transient current to ±20mA for external voltages of up to ±200V. However, for correct functioning, the DC input current should be kept below 2mA. This type of card edge input protection is shown in Figure 40.

In the circuit of Figure 40, if the input diode current exceeds 2mA, a QMOS high-to-low level shifter should be used (e.g., HC4049, or HC4050).

Because QMOS bus-drivers do not have built-in hysteresis, slowly rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the QMOS flip-flop series HC/HCT73, 74,107,109,112, or the dedicated Schmitt-trigger types HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section, "Propagation Delays and Transition Times".

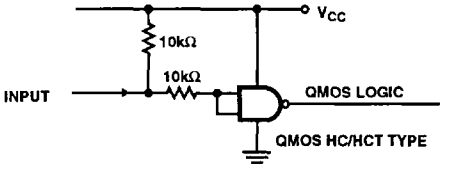



**FIGURE 40. EXAMPLE OF THE CARD EDGE-INPUT-PROTECTION CIRCUIT**

## *Standardized Capacitance Power Dissipation ($C_{PD}$) Test Procedure*

The purpose of the $C_{PD}$ number is to allow the user to estimate the actual power consumption of his system. Therefore, the table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basis, the remaining are measured on a "per device" basis. Each part number's unique setup is listed in the Pin Condition Table. The following paragraphs describe the generic set up for each class of devices.

**All Part Numbers**

Measurements are to be made at $T_A$ = +25°C, $V_{CC}$ = 5V, and three-state outputs both enabled and disabled.

**Gates**

Switch one input. Bias the remaining inputs such that the output switches.

**Latches**

Toggle as in a flip-flop.

**Flipflops**

Switch the clock pin while changing "D" (or biasing "J" and "K") such that the output(s) change each clock cycle. For part numbers with common clocks, exercise the "D", "J", or "K" inputs of only one flip-flop. Set the inputs of the remaining flip-flops so they do not change state.

**Decoders/Demultiplexers**

Switch one address pin, which changes two outputs.

**Data Selectors/Multiplexers**

Switch one address input, with the corresponding data inputs at opposite logic levels, so that the output switches.

**Counters**

Switch the clock pin, with other inputs biased, such that the device counts.

**Shift Registers**

Switch the clock, adjust the data inputs such that the shift register fills with alternate 1's and 0's.

**Transceivers**

Switch one data input. For bi-directional transceivers enable only one direction.

**Parity Generators**

Switch one input.

**Priority Encoders**

Switch the lowest priority input.

**Display Drivers**

Switch one input such that approximately half the outputs change state.

**ALUs/Adders**

Switch one least significant input bit, bias the remaining inputs so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

Since $C_{PD}$ is a measure of device power consumption, and not that of the driven load, each output would ideally be unloaded. However, this is impractical with automatic testers which often have 30pf to 40pF hanging on each pin. Therefore, each output which is switching should be loaded with the standard 50pF. The equivalent load capacitance, based on the number of outputs switching and their frequency, is then subtracted from the measured gross $C_{PD}$ number to obtain the device's actual $C_{PD}$ value.

If a device is tested at a high enough frequency, static supply current will contribute a negligible amount to power consumption and can be ignored. Thus, it is recommended that power consumption be measured at 1MHz and the following formula be used to calculate $C_{PD}$:

$$C_{PD} = \frac{(I_{CC})}{(V_{CC})\,(1E6)} - (\text{Equivalent Load Capacitance})$$

**EXPLANATION OF SYMBOLS**

**Key**

- V = $V_{CC}$ (+5V)
- G = Ground
- H = Logic 1 ($V_{CC}$) - Inputs at $V_{CC}$ for HC Types; 3.5V for HCT Types
- L = Logic 0 (Ground)
- D = Don't Care - Either H or L But Not Switching
- C = a 50pF Load to Ground
- O = An Open Pin; 50pF to Ground is Allowed
- P = Input Pulse (See Illustration)
- Q = Half Frequency Pulse (See Illustration)
- R = 1kΩ Pull-up Resistor to an Additional 5V Supply Other than the $V_{CC}$ Supply
- B = Both R and C

**INPUT PULSES**


**PIN CONDITION TABLE FOR $C_{PD}$ TESTS**

| HC/HCT TYPES | EQUIV-ALENT LOAD (pF) | PIN NUMBER | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 00 | 50 | P | H | C | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 02 | 50 | C | P | L | O | D | D | G | D | D | O | D | D | O | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 03 | 0 | P | H | B | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 04 | 50 | P | C | D | O | D | O | G | O | D | O | D | O | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| U04 | 50 | P | C | D | O | D | O | G | O | D | O | D | O | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 08 | 50 | P | H | C | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 10 | 50 | P | H | D | D | D | O | G | O | D | D | D | C | H | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 11 | 50 | P | H | D | D | D | O | G | O | D | D | D | C | H | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 14 | 50 | P | C | D | O | D | O | G | O | D | O | D | O | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 20 | 50 | P | H | O | H | H | C | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 21 | 50 | P | H | O | H | H | C | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 27 | 50 | P | L | D | D | D | O | G | O | D | D | D | C | L | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 30 | 50 | P | H | H | H | H | H | G | C | O | O | H | H | O | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 32 | 50 | P | L | C | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 42 | 100 | C | C | O | O | O | O | O | G | O | O | O | L | L | L | P | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 73 | 50 | P | H | H | V | D | D | D | O | O | D | G | C | C | H | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

**PIN CONDITION TABLE FOR $C_{PD}$ TESTS (Continued)**

| HC/HCT TYPES | EQUIV-ALENT LOAD (pF) | PIN NUMBER | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 74 | 50 | H | Q | P | H | C | C | G | O | O | D | D | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 75 | 50 | C | Q | D | D | V | D | D | O | O | O | O | G | P | O | O | C | - | - | - | - | - | - | - | - | - | - | - | - |
| 85 | 50 | L | H | P | H | O | C | O | G | L | L | L | L | L | L | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 86 | 50 | P | L | C | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 93 | 47 | Q | L | L | D | V | D | D | C | C | G | C | C | D | P | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 107 | 50 | H | C | C | H | O | O | G | D | D | D | D | P | H | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 109 | 50 | H | H | L | P | H | C | C | G | O | O | D | D | D | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 112 | 50 | P | H | H | H | C | C | O | G | O | D | D | D | D | D | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 123 | 100 | L | H | P | C | O | O | O | G | D | D | D | O | C | O | R | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 125 | 50 | L | P | C | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 126 | 50 | H | P | C | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 132 | 50 | P | H | C | D | D | O | G | O | D | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 137 | 100 | P | L | L | L | L | H | O | G | O | O | O | O | O | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 138 | 100 | P | L | L | L | L | H | O | G | O | O | O | O | O | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 139 | 100 | L | P | L | C | C | O | O | G | O | O | O | O | D | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 147 | 50 | H | H | H | H | H | O | O | G | C | H | P | H | H | O | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 151 | 100 | D | D | L | H | C | C | L | G | L | L | P | D | D | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 153 | 50 | L | L | D | D | L | H | C | G | O | D | D | D | D | P | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 154 | 100 | C | C | O | O | O | O | O | O | O | O | O | G | O | O | O | O | O | L | L | L | L | L | P | V | - | - | - | - |
| 157 | 50 | P | L | H | C | L | L | O | G | O | L | L | O | L | L | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 158 | 50 | P | L | H | C | L | L | O | G | O | L | L | O | L | L | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 160 | 55 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 161 | 50 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 162 | 55 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 163 | 50 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |

PIN CONDITION TABLE FOR $C_{PD}$ TESTS (Continued)

| HC/HCT TYPES | EQUIV-ALENT LOAD (pF) | PIN NUMBER | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 164 | 200 | Q | H | C | C | C | C | G | P | H | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 165 | 50 | H | P | D | D | D | D | C | G | C | Q | D | D | D | D | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 166 | 25 | Q | D | D | D | D | L | P | G | H | D | D | D | C | D | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 173 | 25 | L | L | C | O | O | O | P | G | L | L | D | D | D | Q | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 174 | 25 | H | C | Q | D | O | D | O | G | P | O | D | O | D | D | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 175 | 50 | H | C | C | Q | D | O | O | G | P | O | O | D | D | O | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 181 | 250 | P | H | H | L | L | H | H | L | C | C | C | G | C | B | C | C | C | L | H | L | H | L | H | V | - | - | - | - |
| 190 | 60 | D | C | C | L | L | C | C | G | D | D | H | C | C | P | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 191 | 53 | D | C | C | L | L | C | C | G | D | D | H | C | C | P | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 192 | 60 | D | C | C | H | P | C | C | G | D | D | H | C | C | L | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 193 | 50 | D | C | C | H | P | C | C | G | D | D | H | C | C | L | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 194 | 100 | H | Q | D | D | D | D | D | G | H | L | P | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 195 | 125 | H | H | L | D | D | D | D | G | H | P | C | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 221 | 100 | L | H | P | C | O | O | O | G | D | D | D | O | C | O | R | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 237 | 100 | P | L | L | L | L | H | O | G | O | O | O | O | O | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 238 | 100 | P | L | L | L | L | H | O | G | O | O | O | O | O | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 240 | 50 | L | P | O | D | O | D | O | D | O | G | D | O | D | O | D | O | D | C | D | V | - | - | - | - | - | - | - | - |
| 241 | 50 | L | P | O | D | O | D | O | D | O | G | D | O | D | O | D | O | D | C | H | V | - | - | - | - | - | - | - | - |
| 242 | 50 | L | O | P | D | D | D | G | O | O | O | C | O | L | V | | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 243 | 50 | L | O | P | D | D | D | G | O | O | O | C | O | L | V | | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 244 | 50 | L | P | O | D | O | D | O | D | O | G | D | O | D | O | D | O | D | C | D | V | - | - | - | - | - | - | - | - |
| 245 | 50 | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | - | - | - | - | - | - | - | - |
| 251 | 100 | D | D | L | H | C | C | L | G | L | L | P | D | D | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 253 | 50 | L | L | D | D | L | H | C | G | O | D | D | D | D | P | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 257 | 50 | P | L | H | C | D | D | O | G | O | D | D | O | D | D | L | V | - | - | - | - | - | - | - | - | - | - | - | - |

**PIN CONDITION TABLE FOR $C_{PD}$ TESTS (Continued)**

| HC/HCT TYPES | EQUIV-ALENT LOAD (pF) | PIN NUMBER | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 258 | 50 | P | L | H | C | D | D | O | G | O | D | D | O | D | D | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 259 | 25 | L | L | L | C | O | O | O | G | O | O | O | O | Q | P | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 7266 | 50 | P | L | C | O | D | D | G | D | D | O | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 273 | 25 | H | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | - | - | - | - | - | - | - | - |
| 280 | 100 | L | L | O | L | C | C | G | P | L | L | L | L | L | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 283 | 250 | C | H | L | C | P | H | L | G | C | C | H | L | C | L | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 297 | 12 | H | H | H | P | Q | L | C | G | D | D | O | O | D | H | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 299 | 250 | H | L | L | C | C | C | C | C | H | G | Q | P | C | C | C | C | C | D | L | V | - | - | - | - | - | - | - | - |
| 354 | 100 | D | D | D | D | D | D | L | H | L | G | L | L | L | P | L | L | H | C | C | V | - | - | - | - | - | - | - | - |
| 356 | 50 | D | D | D | D | D | D | D | Q | P | G | L | L | L | L | L | L | H | C | C | V | - | - | - | - | - | - | - | - |
| 365 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 366 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 367 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 368 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 373 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | - | - | - | - | - | - | - | - |
| 374 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | - | - | - | - | - | - | - | - |
| 377 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | - | - | - | - | - | - | - | - |
| 390 | 50 | P | L | C | Q | C | C | C | G | O | O | O | D | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 393 | 47 | P | L | C | C | C | C | G | O | O | O | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 423 | 100 | L | P | H | C | O | O | O | G | D | D | D | O | C | O | R | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 533 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | - | - | - | - | - | - | - | - |
| 534 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | - | - | - | - | - | - | - | - |
| 540 | 50 | L | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | - | - | - | - | - | - | - | - |
| 541 | 50 | L | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | - | - | - | - | - | - | - | - |
| 563 | 25 | L | Q | D | D | D | D | D | D | D | G | P | O | O | O | O | O | O | O | C | V | - | - | - | - | - | - | - | - |

**PIN CONDITION TABLE FOR $C_{PD}$ TESTS (Continued)**

| HC/HCT TYPES | EQUIV-ALENT LOAD (pF) | PIN NUMBER | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 564 | 25 | L | Q | D | D | D | D | D | D | D | G | P | O | O | O | O | O | O | O | C | V | - | - | - | - | - | - | - | - |
| 573 | 25 | L | P | D | D | D | D | D | D | D | G | H | O | O | O | O | O | O | O | C | V | - | - | - | - | - | - | - | - |
| 574 | 25 | L | Q | D | D | D | D | D | D | D | G | P | O | O | O | O | O | O | O | C | V | - | - | - | - | - | - | - | - |
| 583 | 250 | H | H | H | L | L | C | C | G | C | C | C | H | P | L | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 597 | 25 | D | D | D | D | D | D | D | G | C | H | P | D | H | Q | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 640 | 50 | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | - | - | - | - | - | - | - | - |
| 643 | 50 | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | - | - | - | - | - | - | - | - |
| 646 | 50 | D | L | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | D | D | V | - | - | - | - |
| 648 | 50 | D | L | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | D | D | V | - | - | - | - |
| 670 | 100 | Q | Q | Q | L | P | C | C | G | C | C | L | L | L | P | Q | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 688 | 50 | L | P | L | L | L | L | L | L | L | G | L | L | L | L | L | L | L | L | C | V | - | - | - | - | - | - | - | - |
| 4002 | 50 | C | P | L | L | L | O | G | O | D | D | D | D | O | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 4015 | 100 | P | C | O | O | O | D | D | G | D | O | C | C | C | L | Q | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4016 | 0 | O | O | O | O | D | D | G | O | O | O | O | D | P | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 4017 | 55 | C | C | C | C | C | C | C | G | C | C | C | C | L | P | L | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4020 | 48 | C | C | C | C | C | C | C | G | C | P | L | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4024 | 48 | P | L | C | C | C | C | G | O | C | O | C | C | O | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 4040 | 48 | C | C | C | C | C | C | C | G | C | P | L | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4046A | 50 | O | C | L | O | H | O | O | G | O | O | O | O | O | P | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4049 | 50 | V | C | P | O | D | O | D | G | D | O | D | O | O | D | O | O | - | - | - | - | - | - | - | - | - | - | - | - |
| 4050 | 50 | V | C | P | O | D | O | D | G | D | O | D | O | O | D | O | O | - | - | - | - | - | - | - | - | - | - | - | - |
| 4051 | 0 | O | O | O | O | O | L | G | G | L | L | P | O | O | O | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4052 | 0 | O | O | O | O | O | L | G | G | L | P | O | O | O | O | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4053 | 0 | O | O | O | O | O | L | G | G | L | L | P | O | O | O | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4059 | 17 | P | D | H | L | L | L | L | L | L | L | H | G | H | H | L | L | L | L | L | L | L | L | C | V | - | - | - | - |

**PIN CONDITION TABLE FOR $C_{PD}$ TESTS (Continued)**

| HC/HCT TYPES | EQUIV-ALENT LOAD (pF) | PIN NUMBER | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 4060 | 106 | C | C | C | C | C | C | C | G | C | C | P | L | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4066 | 0 | O | O | O | O | D | D | G | O | O | O | O | D | P | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 4067 | 0 | O | O | O | O | O | O | O | O | O | P | L | G | L | L | L | O | O | O | O | O | O | O | O | V | - | - | - | - |
| 4075 | 50 | P | L | D | D | D | O | G | L | C | O | D | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 4094 | 250 | H | Q | P | C | C | C | C | G | C | C | C | C | C | C | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4316 | 0 | O | O | O | O | P | D | L | G | G | O | O | O | O | D | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4351 | 0 | O | O | O | O | O | O | L | H | G | G | H | P | L | O | L | O | O | O | O | V | - | - | - | - | - | - | - | - |
| 4352 | 0 | O | O | O | O | O | O | L | H | G | G | H | P | L | O | O | O | O | O | O | V | - | - | - | - | - | - | - | - |
| 4353 | 0 | O | O | O | O | O | O | L | H | G | G | H | P | L | O | L | O | O | O | O | V | - | - | - | - | - | - | - | - |
| 4510 | 55 | L | C | D | D | L | C | C | G | L | H | C | D | D | C | P | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4511 | 200 | L | L | H | H | L | L | P | G | C | C | O | O | C | O | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4514 | 100 | H | P | L | O | O | O | O | O | C | O | C | G | O | O | O | O | O | O | O | O | L | L | L | V | - | - | - | - |
| 4515 | 100 | H | P | L | O | O | O | O | O | C | O | C | G | O | O | O | O | O | O | O | O | L | L | L | V | - | - | - | - |
| 4516 | 50 | L | C | D | D | L | C | C | G | L | H | C | D | D | C | P | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4518 | 50 | P | H | C | C | C | C | L | G | D | D | O | O | O | O | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4520 | 47 | P | H | C | C | C | C | L | G | D | D | O | O | O | O | D | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4538 | 100 | G | R | H | P | H | C | C | G | O | O | D | D | L | O | G | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 4543 | 50 | H | L | L | H | L | P | L | G | C | C | C | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 7030 | 325 | G | G | C | P | Q | Q | Q | Q | Q | Q | Q | Q | Q | G | L | C | C | C | C | C | C | C | C | C | C | P | H | V |
| 7046A | 50 | O | C | L | O | H | O | O | G | O | O | O | O | O | P | O | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 40102 | 5 | P | H | L | L | L | L | L | G | H | L | L | L | L | C | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 40103 | 3 | P | H | L | L | L | L | L | G | H | L | L | L | L | C | H | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 40104 | 100 | H | Q | D | D | D | D | D | G | H | L | P | C | C | C | C | V | - | - | - | - | - | - | - | - | - | - | - | - |
| 40105 | 200 | L | C | P | Q | Q | Q | Q | G | L | C | C | C | C | C | P | V | - | - | - | - | - | - | - | - | - | - | - | - |