National Semiconductor

MICROCIRCUIT DATA SHEET

MNMM54C02-X REV 1A0

Original Creation Date: 10/16/95
Last Update Date: 05/19/97
Last Major Revision Date: 04/02/97

QUAD 2-INPUT NOR GATE

General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54 devices minimizes design time for those designers already familiar with the standard 54 logic family.

All inputs are protected from damage due to static discharge by diode clamps to Vcc and Gnd.

Industry Part Number

MM54C02

NS Part Numbers

MM54C02J/883
MM54C02W/883

Prime Die

MM54C02

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide supply voltage range	3V to 15V
- Guaranteed noise margin	1V
- High noise immunity	0.45 Vcc (typ.)
- Low power consumption	10nW/package (typ.)
- Low power TTL compatibility	Fan out of 2 driving 74L

(Absolute Maximum Ratings)

Voltage at Any Pin	-0.3V to Vcc +0.3V
Operating Temperature Range	-55 C to +125 C
Storage Temperature Range	-65 C to +150 C
Operating Vcc Range	3.0V to 15V
Maximum Vcc Voltage	18V
Power Dissipation (Pd)	
Dual-In-Line	700mW
Small Outline	500mW
Lead Temperature (Soldering, 10 seconds)	300 C

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Logical "1" Output Voltage	Vcc = 5V, Iout = -10uA			4.5		V	1, 2, 3
		Vcc = 10V, Iout = -10uA			9		V	1, 2, 3
		Vcc = 4.5V, Iout = -360uA (CMOS to LP)			2.4		V	1, 2, 3
		Vcc = 4.5V, Iout = -10uA (LP to CMOS)			4.4		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc = 5V, Iout = 10uA				0.5	V	1, 2, 3
		Vcc = 10V, Iout = 10uA				1	V	1, 2, 3
		Vcc = 4.5V, Iout = 360uA (CMOS to LP)				0.4	V	1, 2, 3
		Vcc = 4.5V, Iout = 10uA (LP to CMOS)				0.4	V	1, 2, 3
Iih	Logical "1" Input Current	Vcc = 15V, Vin = 15V				0.15	uA	1, 3
						1	uA	2
Iil	Logical "0" Input Current	Vcc = 15V, Vin = 0V				-0.15	uA	1, 3
						-1	uA	2
Isource	Output Source Current	Vcc = 5V, Vin = 0V, Vout = 0V			-1.75		mA	1
		Vcc = 10V, Vin = 0V, Vout = 0V			-8		mA	1
Isink	Output Sink Current	Vcc = 5V, Vin = 5V, Vout = Vcc			1.75		mA	1
		Vcc = 10V, Vin = 10V, Vout = Vcc			8		mA	1
Icc	Power Supply Current	Vcc = 15V				0.15	uA	1, 3
						15	uA	2
Vih	Logical "1" Input Voltage	Vcc = 5V	1		3.5		V	1, 2, 3
		Vcc = 10V	1		8		V	1, 2, 3
		Vcc = 4.5V (LP to CMOS)	1		3		V	1, 2, 3
		Vcc = 4.5V (CMOS to LP)	1		4		V	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vil	Logical "0" Input Voltage	Vcc = 5V	1			1.5	V	1, 2, 3
		Vcc = 10V	1			2	V	1, 2, 3
		Vcc = 4.5V (LP to CMOS)	1			0.8	V	1, 2, 3
		Vcc = 4.5V (CMOS to LP)	1			1	V	1, 2, 3

AC PARAMETERS: PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Cl = 50pF

tPHL		Vcc = 5V	3			90	nS	9
			3			125	nS	10
			3			70	nS	11
		Vcc = 10V	2			60	nS	9
			2			85	nS	10
			2			50	nS	11
tPLH		Vcc = 5V	3			90	nS	9
			3			125	nS	10
			3			70	nS	11
		Vcc = 10V	2			60	nS	9
			2			85	nS	10
			2			50	nS	11

Note 1: Parameter tested go-no-go only.
Note 2: Guaranteed parameter not tested.
Note 3: Tested at 25 C; guaranteed but not tested at +125 C and -55 C.