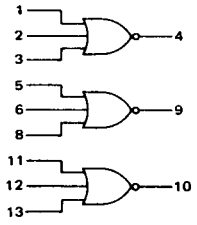
MC1007 thru MC1009
MC1207 thru MC1209

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

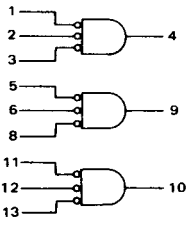
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

POSITIVE LOGIC



$4 = \overline{1 + 2 + 3}$

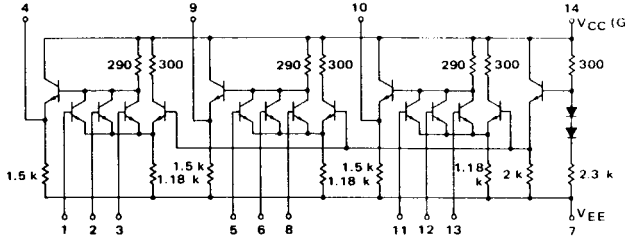
NEGATIVE LOGIC



$4 = \overline{1 \cdot 2 \cdot 3}$

DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = MC1007/MC1207 – 110 mW typical
MC1008/MC1208 – 75 mW typical
MC1009/MC1209 – 60 mW typical

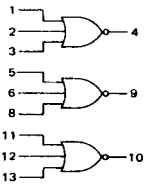
MC1007/MC1207 CIRCUIT SCHEMATIC



MC1008/MC1208
Omit output pulldown resistors to pins 9 and 10.

MC1009/MC1209
Omit all output pulldown resistors.

Resistor values are nominal.



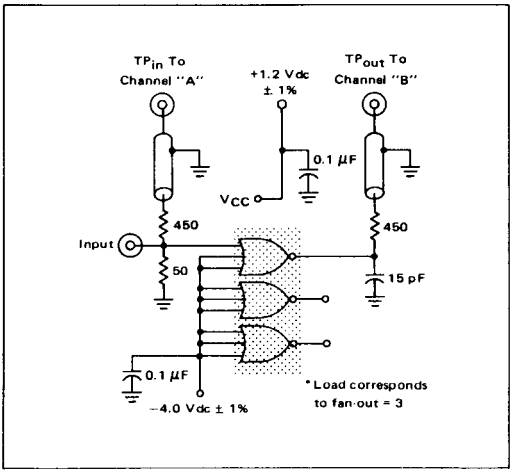
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 k ohm resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1207-1209 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1007-1009 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7														
MC1207 MC1007			-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
MC1208 MC1008			-	-	-	20	-	-		-	-	-	20	-	-	
MC1209 MC1009			-	-	-	16	-	-		-	-	-	16	-	-	
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-		-	-		-	-	-		-	-	
		3	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	4	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	4	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+4-}	4	4.0	7.5	4.0	7.5	6.0	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.5	ns
	t_{1-4+}		4.0	7.0	4.0	7.0	6.0	9.0		4.0	7.0	4.0	7.0	5.0	8.0	
(Fan-Out = 15)	t_{1+4-}		18	-	18	-	22	-		18	-	18	-	20	-	
	t_{1-4+}		5.0	-	5.0	-	9.0	-		5.0	-	5.0	-	7.0	-	
Rise Time (Fan-Out = 3)	t_{4+}		5.0	7.5	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.5	8.0	
Fall Time (Fan-Out = 3)	t_{4-}		6.0	8.5	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.0	9.0	

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

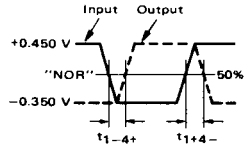
SWITCHING TIME TEST CIRCUIT @ 25°C



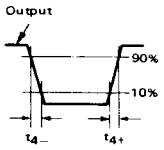
@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	mAdc I_L
MC1207-1209	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1007-1009	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1207/MC1007			-	-	-	1,2,3,5,6,7,8,11,12,13	-	14
MC1208/MC1008			-	-	-		-	
MC1209/MC1009			-	-	-		-	
Input Current	I_{in}	1	-	-	1	2,3,5,6,7,8,11,12,13	-	14
		2	-	-	2	1,3,5,6,7,8,11,12,13	-	
		3	-	-	3	1,2,5,6,7,8,11,12,13	-	
Input Leakage Current	I_R	Inputs*	-	-		1,2,3,5,6,7,8,11,12,13	-	14
"NOR" Logical "1" Output Voltage†	V_{OH}‡	4	1	-	-	2,3,5,6,7,8,11,12,13	4	14
			2	-	-	1,3,5,6,7,8,11,12,13		
			3	-	-	1,2,5,6,7,8,11,12,13		
"NOR" Logical "0" Output Voltage	V_{OL}	4	-	1	-	2,3,5,6,7,8,11,12,13	-	14
			-	2	-	1,3,5,6,7,8,11,12,13	-	
			-	3	-	1,2,5,6,7,8,11,12,13	-	
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Propagation Delay (Fan-Out = 3)	t_{1+4-}	4	1	4	-	2,3,5,6,7,8,11,12,13	-	14
	t_{1-4+}				-		-	
(Fan-Out = 15)	t_{1+4-}				-		-	
	t_{1-4+}				-		-	
Rise Time (Fan-Out = 3)	t_{4+}				-		-	
Fall Time (Fan-Out = 3)	t_{4-}				-		-	

PROPAGATION DELAY



RISE AND FALL TIMES



Switching waveforms shown for pulse in on pin 1 and pulse out on pin 4, however all other input-output combinations will meet the limits specified.

Input Pulse t_r and t_f = 5.0 ± 0.5 ns.

SWITCHING TIME WAVEFORMS

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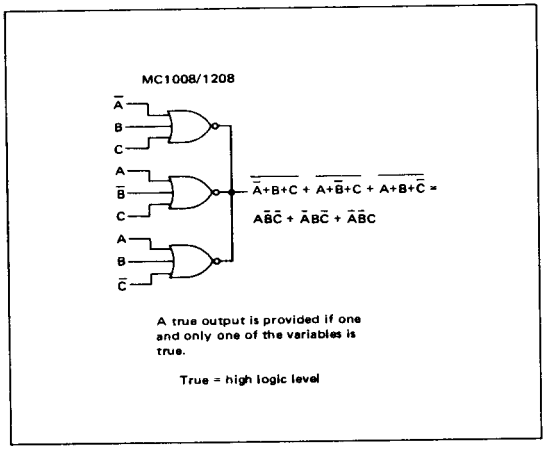
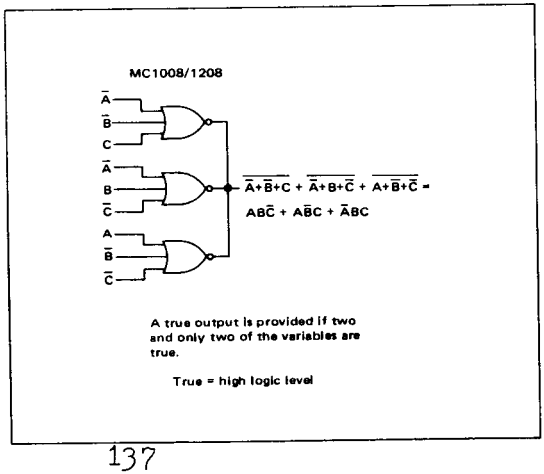
APPLICATIONS INFORMATION

The MC1007-1009/MC1207-1209 triple 3-input gates provide NOR outputs only, due to the pin limitation of the 14-lead package. The three options on the emitter follower pull-down resistors, as on all of the basic gates, provide a significant power savings when the wired-OR feature is utilized. The power dissipation of additional emitter-follower resistors and additional gates to perform the OR function is eliminated. By making liberal use of the wired-OR feature, power dissipation in a logic system may be reduced by one-half. If fast propagation delay time through a logic chain is required, an additional gate propagation delay of 4.0 to 5.0 ns is saved each time the wired-OR option is employed. Shown below are two examples of an MC1008/MC1208 with the outputs wired together.





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