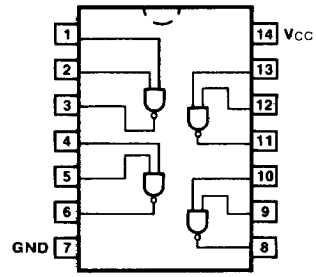
54/7438 01158 6
54LS/74LS38 01158 9

QUAD 2-INPUT NAND BUFFER
(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7438PC, 74LS38PC		9A
Ceramic DIP (D)	A	7438DC, 74LS38DC	5438DM, 54LS38DM	6A
Flatpak (F)	A	7438FC, 74LS38FC	5438FM, 54LS38FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	OC**/30	OC**/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.4			V	V_{IN} = 2.0 V, V_{CC} = Min, I_{OL} = 48 mA	
I_{OH}	Output HIGH Current				250	µA	V_{OH} = 5.5 V, V_{CC} = Min, V_{IN} = V_{IL}	
I_{CCH}	Power Supply Current		8.5		2.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			54		12		V_{IN} = Open	
t_{PLH}	Propagation Delay		22		22	ns	Figs. 3-2, 3-4	
t_{PHL}			18		22			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC—Open Collector