

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4011UB**

### **gates**

### **Quadruple 2-input NAND gate**

Product specification  
File under Integrated Circuits, IC04

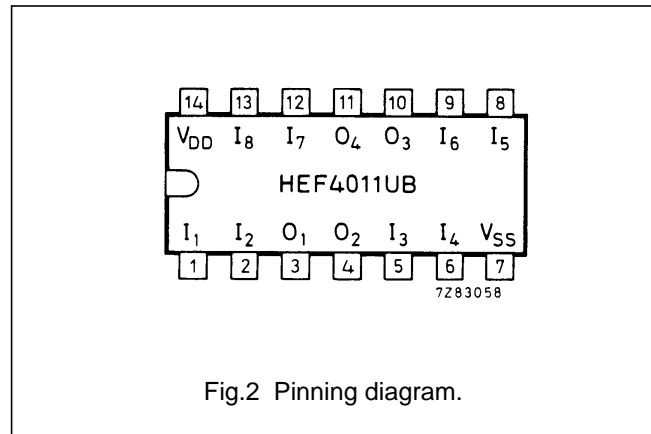
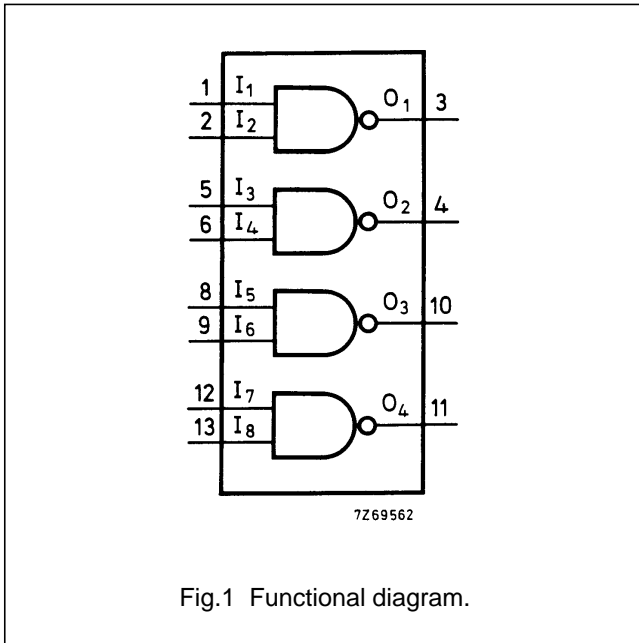
January 1995

# Quadruple 2-input NAND gate

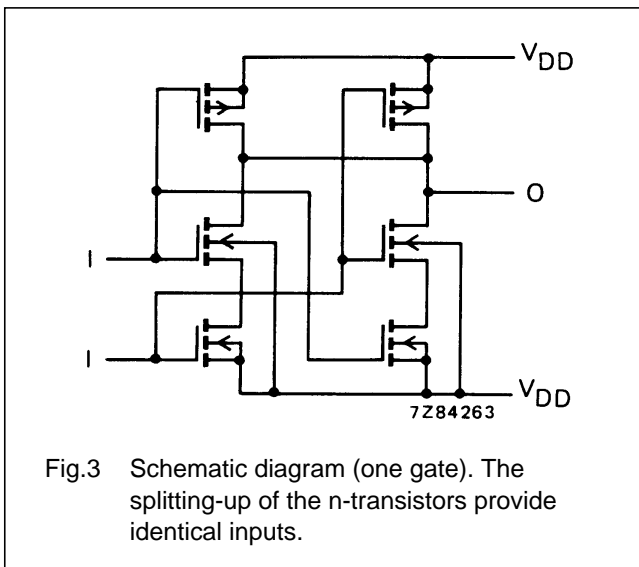
# HEF4011UB gates

### DESCRIPTION

The HEF4011UB is a quadruple 2-input NAND gate. This unbuffered single stage version provides a direct implementation of the NAND function. The output impedance and output transition time depends on the input voltage and input rise and fall times applied.



- HEF4011UBP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4011UBD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4011UBT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America



### FAMILY DATA, I<sub>DD</sub> LIMITS category GATES

See Family Specifications for V<sub>IH</sub>/V<sub>IL</sub> unbuffered stages

# Quadruple 2-input NAND gate

# HEF4011UB gates

## AC CHARACTERISTICS

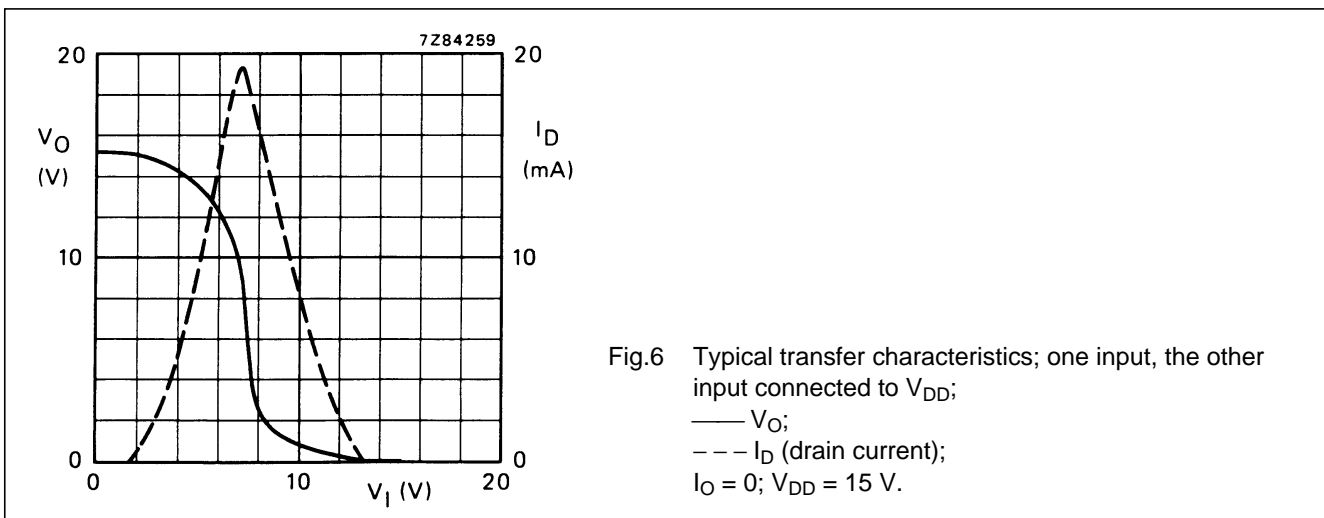
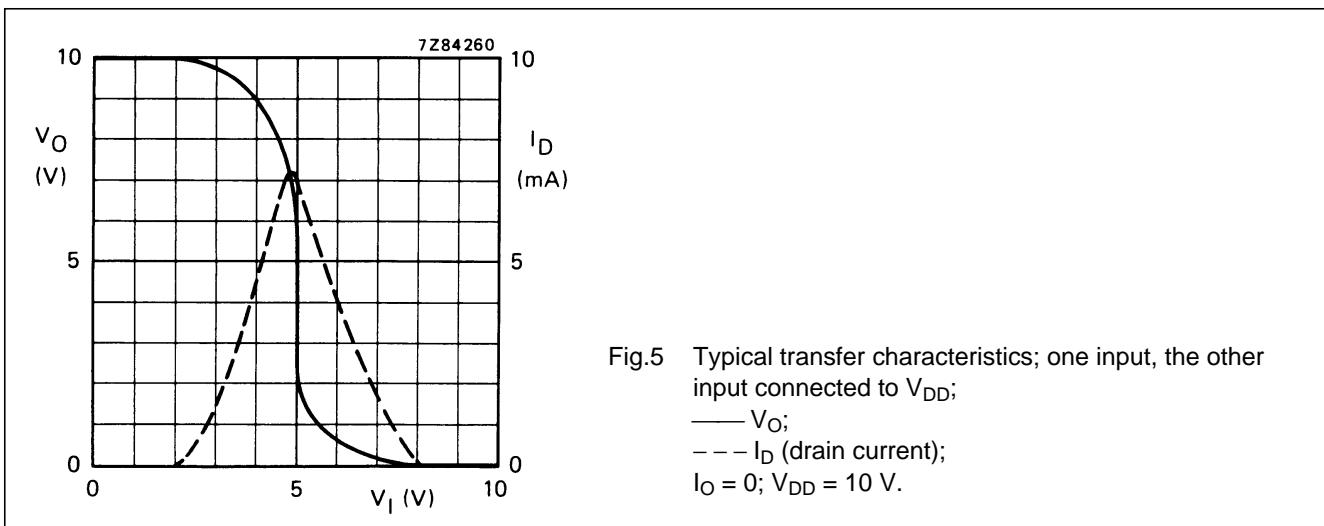
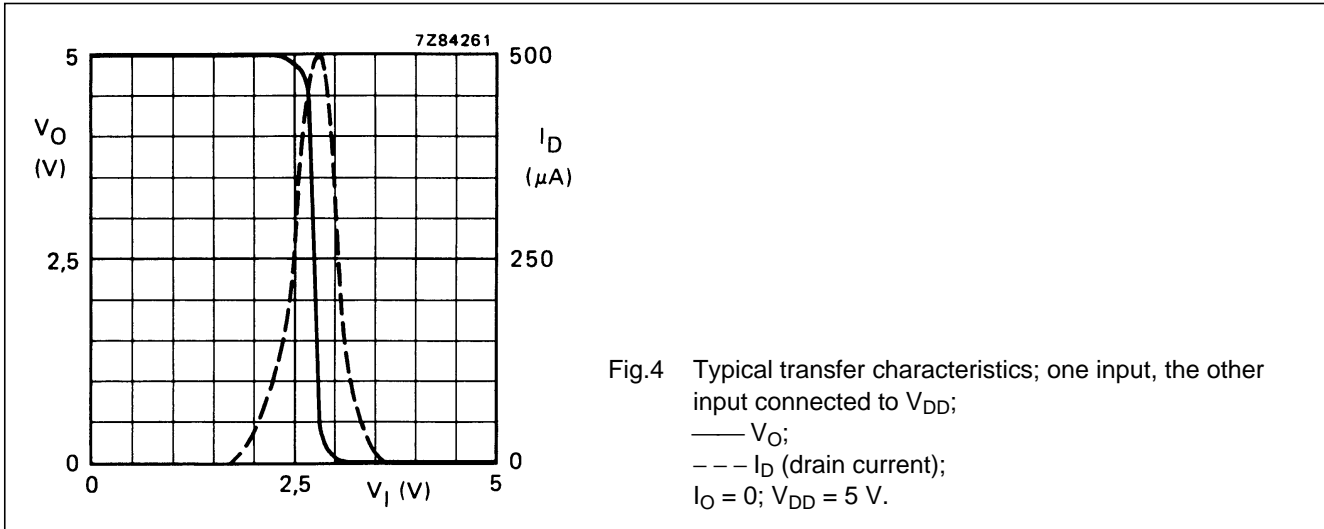
$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	60	120	ns	$25\text{ ns} + (0,70\text{ ns/pF}) C_L$
	10		25	50	ns	$12\text{ ns} + (0,27\text{ ns/pF}) C_L$
	15		20	40	ns	$10\text{ ns} + (0,20\text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{PLH}$	35	70	ns	$8\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		20	40	ns	$9\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		17	35	ns	$9\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	75	150	ns	$15\text{ ns} + (1,20\text{ ns/pF}) C_L$
	10		30	60	ns	$6\text{ ns} + (0,48\text{ ns/pF}) C_L$
	15		20	40	ns	$4\text{ ns} + (0,32\text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{TLH}$	60	110	ns	$10\text{ ns} + (1,00\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
Input capacitance		$C_{IN}$		10	pF	

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$5\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$25\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

Quadruple 2-input NAND gate

HEF4011UB  
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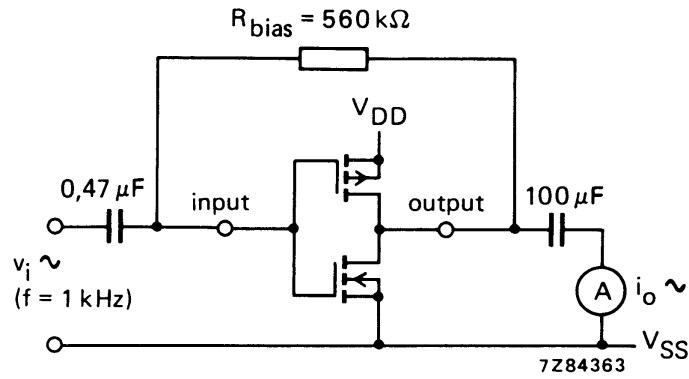
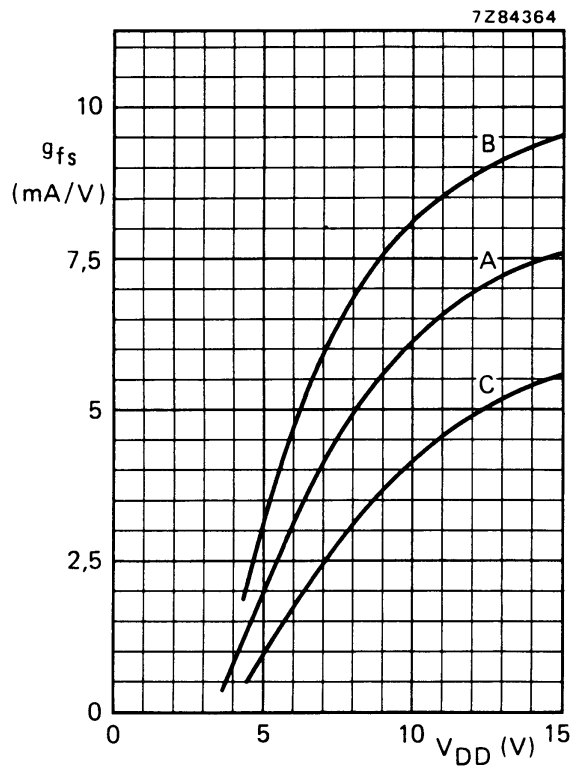


Fig.7 Test set-up for measuring forward transconductance  $g_{fs} = di_o/dv_i$  at  $v_o$  is constant (see also graph Fig.8).



A : average,  
 B : average + 2 s,  
 C : average - 2 s, where 's' is the observed standard deviation.

Fig.8 Typical forward transconductance  $g_{fs}$  as a function of the supply voltage at  $T_{amb} = 25\text{ }^\circ\text{C}$ .

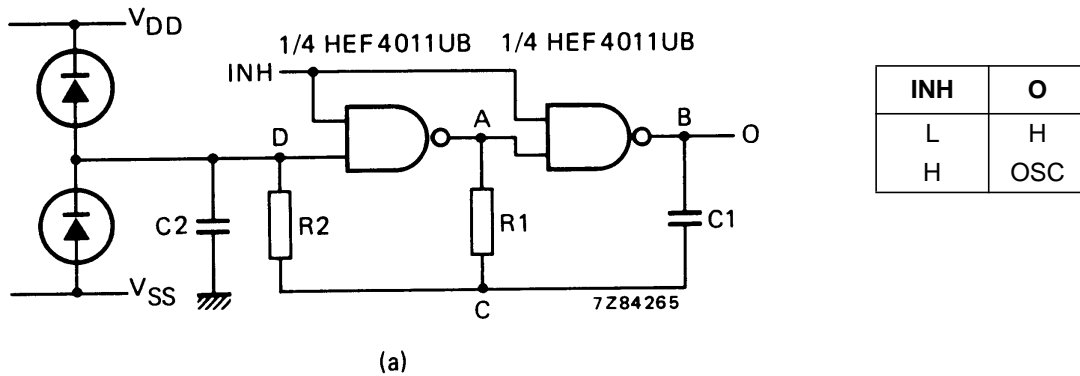
Quadruple 2-input NAND gate

HEF4011UB gates

APPLICATION INFORMATION

Some examples of applications for the HEF4011UB are shown below.

Because of the fact that this circuit is unbuffered, it is suitable for use in (partly) analogue circuits.



In Fig.9 the oscillation frequency is mainly determined by R1C1, provided  $R1 \ll R2$  and  $R2C2 \ll R1C1$ . The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period  $T_p$  is given by  $T_p = T_1 + T_2$ , in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

$V_{ST}$  is the signal threshold level of the gate. The period is fairly independent of  $V_{DD}$ ,  $V_{ST}$  and temperature. The duty factor, however, is influenced by  $V_{ST}$ .

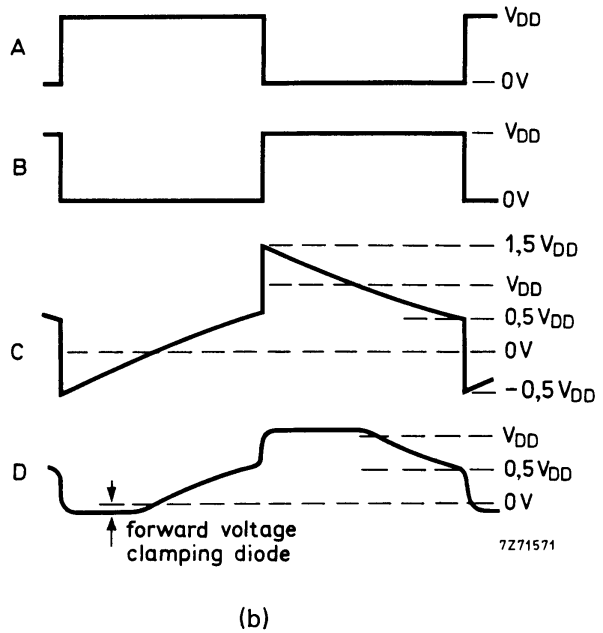
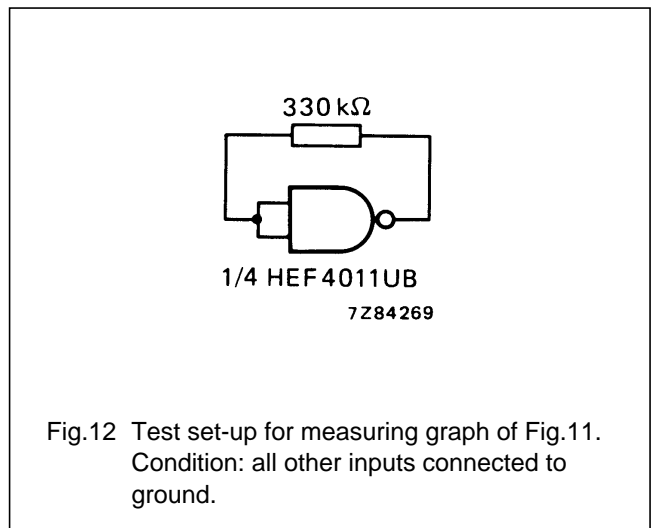
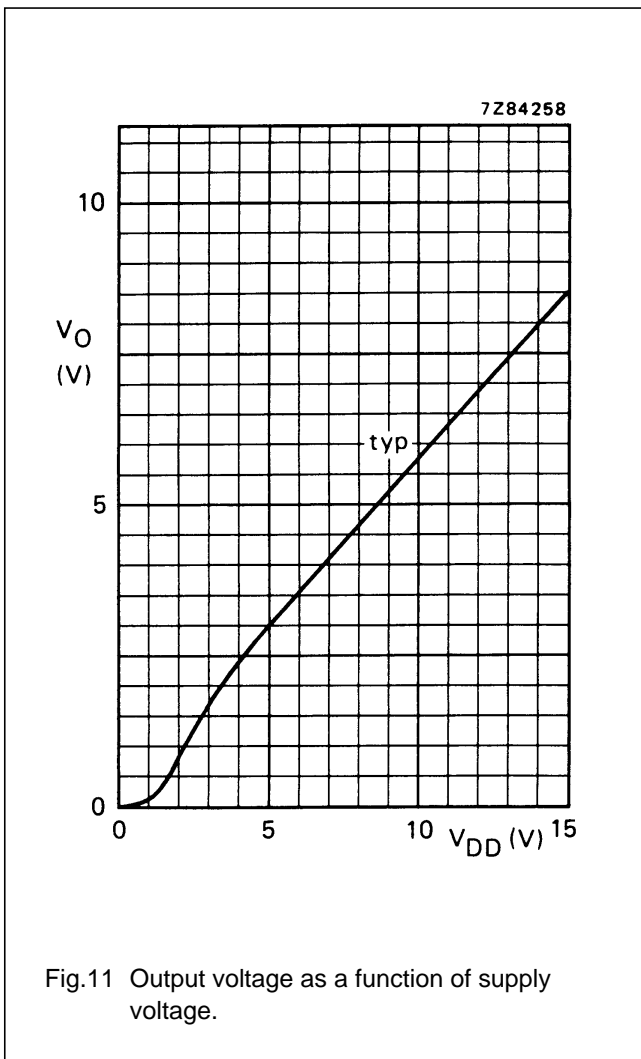
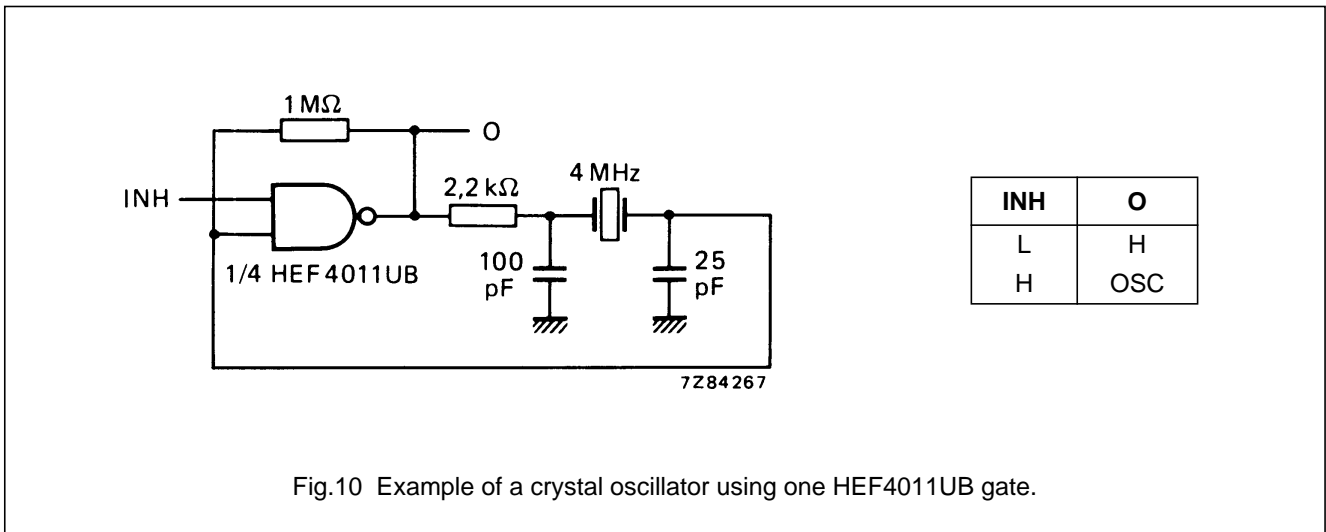


Fig.9 (a) Astable relaxation oscillator using two HEF4011UB gates; the diodes may be BAW62; C2 is a parasitic capacitance.  
 (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

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**NOTES**

If a gate is just used as an amplifying inverter, there are two possibilities:

- Connecting the inputs together gives simpler wiring, but makes the device output not completely symmetrical.
- Connecting one input to  $V_{DD}$  will give the device a symmetrical output.

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