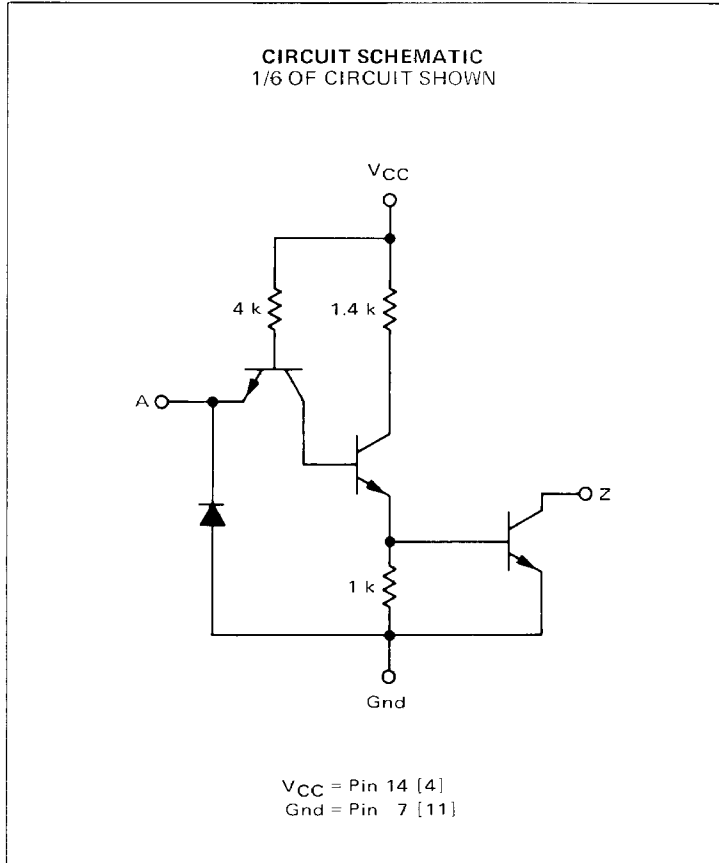


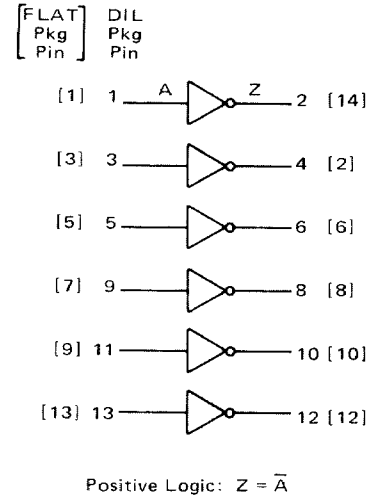


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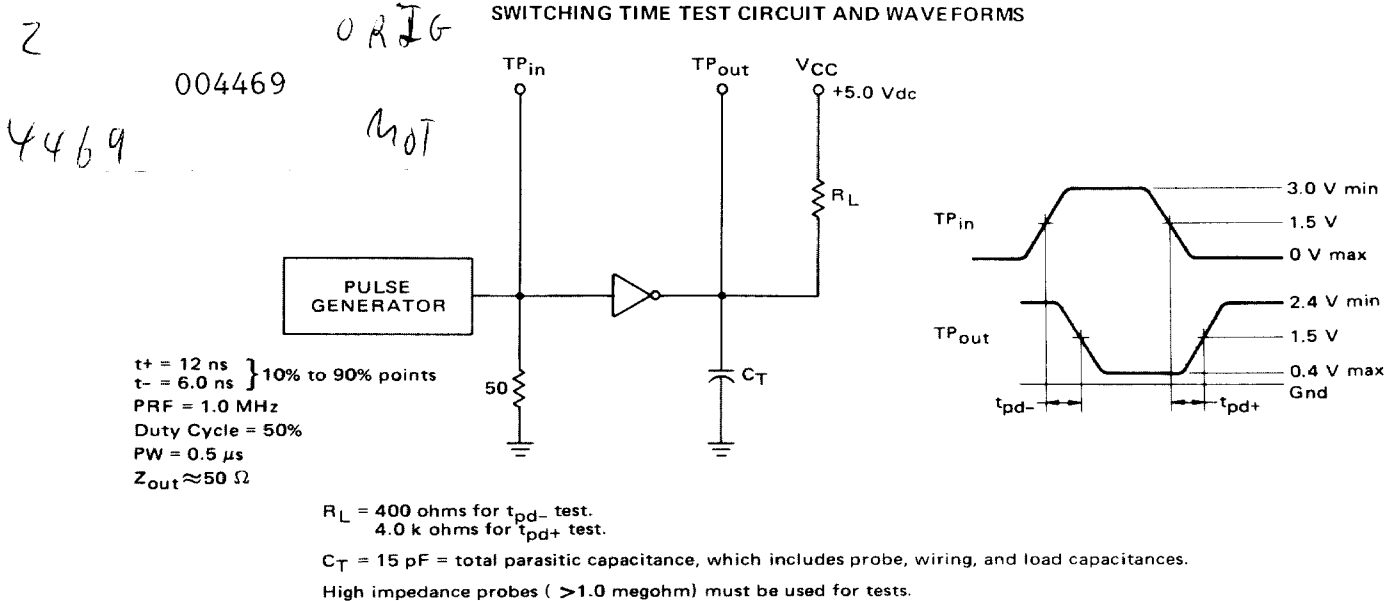
Add Suffix F for TO-86 ceramic package (Case 607).
 Suffix L for TO-116 ceramic package (Case 632).
 Suffix P for TO-116 plastic package (Case 605) MC7405 only.



This device consists of six independent inverting gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.

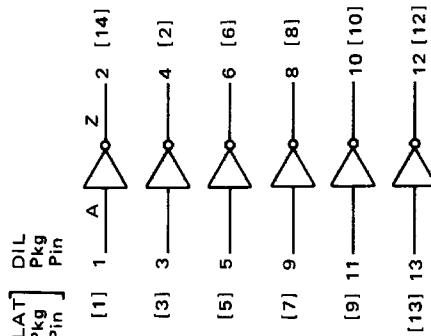


Input Loading Factor = 1
 Output Loading Factor = 10
 Total Power Dissipation = 60 mW typ/pkg
 Propagation Delay Time = 35 ns typ



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



V = V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
mA		Volts											
I _{OL}	V _{CEX}	V _{IL}	V _{IH}	V _{IHH}	V _{R1}	V _{R2}	V _{th1}	V _{th0}	V _{CC}	V _{CCL}	V _{CCH}		
16	5.5	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50		
16	5.5	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25		

Pin 7 [11] is grounded for all tests in addition to the pins listed below:

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Characteristic	Symbol	Pin Under Test	MC5405 Test Limits -55 to +125°C			MC7405 Test Limits 0 to +70°C		
			Min	Max	Unit	Min	Max	Unit
Input Forward Current	I _F	A	-	-1.6	mAdc	-	-1.6	mAdc
Leakage Current	I _{R1}	A	-	40	μAdc	-	40	μAdc
	I _{R2}	A	-	1.0	mAdc	-	1.0	mAdc
Output Voltage	V _{OL}	Z	-	0.4	Vdc	-	0.4	Vdc
Output Leakage Current	I _{CEX}	Z	0.25	-	mAdc	0.25	-	mAdc
Power Requirements (Total Device) Power Supply Drain	I _{PDH}	V	-	33**	mAdc	-	33**	mAdc
	I _{PDL}	V	-	12**	mAdc	-	12**	mAdc
Switching Parameters	Turn-On Delay t _{pd-}	A,Z	-	15**	ns	-	15**	ns
		A,Z	-	55**	ns	-	55**	ns

**Ground inputs to inverters not under test.
**Tested only at 25°C.

