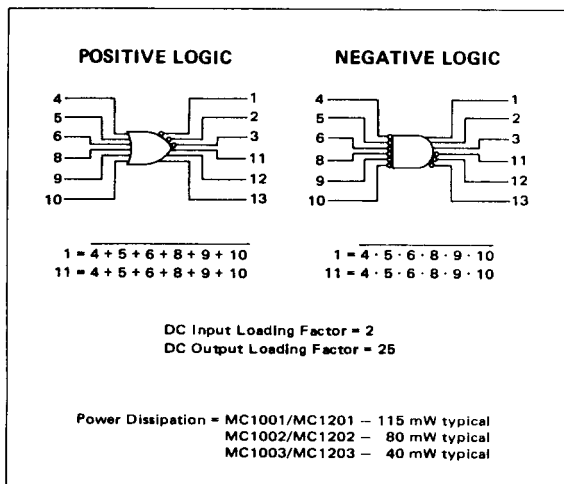


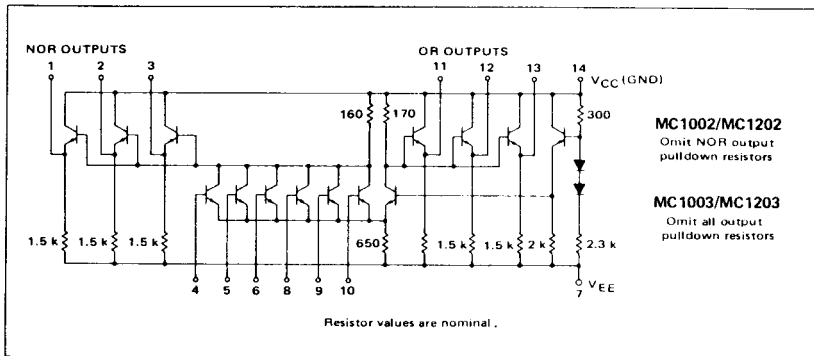
MC1001 thru MC1003 MC1201 thru MC1203

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

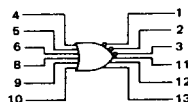
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



MC1001/MC1201 CIRCUIT SCHEMATIC



MC1001 thru MC1003, MC1201 thru MC1203 (continued)



ELECTRICAL CHARACTERISTICS

Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1201-1203 Test Limits						MC1001-1003 Test Limits							
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I _E	7	-	-	-	32	-	-	-	-	-	-	32	-	-	mAdc
			-	-	-	22	-	-	-	-	-	-	22	-	-	
			-	-	-	11	-	-	-	-	-	-	11	-	-	
Input Current	I _{in}	4, 5, 6, 8, 9, 10	-	-	-	200	-	-	-	-	-	-	200	-	-	μAdc
Input Leakage Current	I _R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
'NOR' Logical '1' Output Voltage	V _{OH} ‡	1, 2, 3†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
'NOR' Logical '0' Output Voltage	V _{OL}	1, 2, 3†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
'OR' Logical '1' Output Voltage‡	V _{OH} ‡	11, 12, 13†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
'OR' Logical '0' Output Voltage	V _{OL}	11, 12, 13†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times Propagation Delay (Fan-Out = 3)	t ₄₋₁₋ t ₄₋₁₊ t ₄₋₁₁₊ t ₄₋₁₁₋	1	4.0	7.5	4.0	7.0	6.0	9.0	ns	4.0	7.0	4.0	7.0	5.0	8.0	ns
		11					5.0	9.0								
		11					6.0	9.0								
		(Fan-Out = 15)	1	18	-	18	-	22	-	18	-	18	-	20	-	
		t ₄₋₁₋ t ₄₋₁₊ t ₄₋₁₁₊ t ₄₋₁₁₋	1	6.0	-	6.0	-	8.0	-	6.0	-	6.0	-	7.0	-	
		11	4.0	-	4.0	-	6.0	-	4.0	-	4.0	-	5.0	-		
	Rise Time (Fan-Out = 3)	t ₁₊ t ₁₁₊	1	5.0	8.0	5.0	7.5	6.0	9.0	5.0	7.5	5.0	7.5	5.5	8.0	
			11	4.0	7.0	4.0	6.5	5.0	8.0	4.0	6.5	4.0	6.5	4.5	7.0	
	Fall Time (Fan-Out = 3)	t ₁₋ t ₁₁₋	1	6.0	8.5	6.0	8.0	7.0	10	6.0	8.0	6.0	8.0	6.5	9.0	
			11	6.0	8.0	6.0	8.0	7.0	10	6.0	8.0	6.0	8.0	6.5	9.0	

* Individually test each input using the pin connections shown.

† Individually test each output listed using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.

@Test
Temperature
MC1201-1203
MC1001-1003

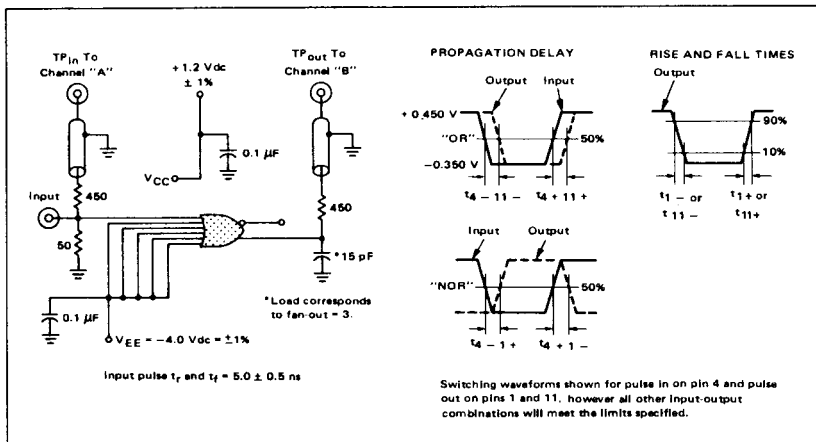
TEST VOLTAGE/CURRENT VALUES					
Vdc ±1.0%					
	V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L mAdc
-55°C	-5.2 to -1.405	-1.165 to -0.625	-	5.2	-2.5
+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	5.2	-2.5
+125°C	-5.2 to -1.205	-0.875 to -0.530	-	5.2	-2.5
0°C	-5.2 to -1.350	-1.070 to -0.740	-	5.2	-2.5
+25°C	-5.2 to -1.325	-1.025 to -0.700	0.700	5.2	-2.5
+75°C	-5.2 to -1.260	-0.950 to -0.615	-	5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					V _{CC} (Gnd)
			V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	
Power Supply Drain Current MC1201/MC1001 MC1202/MC1002 MC1203/MC1003	I _E	7 ↓	-	-	-	4, 5, 6, 7, 8, 9, 10	-	14
Input Current	I _{in}	4 5 6 8 9 10	-	-	4 5 6 8 9 10	5, 6, 7, 8, 9, 10 4, 6, 7, 8, 9, 10 4, 5, 7, 8, 9, 10 4, 5, 6, 7, 9, 10 4, 5, 6, 7, 8, 10 4, 5, 6, 7, 8, 9	-	14
Input Leakage Current	I _R	Inputs*	-	-	-	4, 5, 6, 7, 8, 9, 10	-	14
"NOR" Logical "1" Output Voltage	V _{OH1}	1, 2, 3† ↓	4 5 6 8 9 10	-	-	5, 6, 7, 8, 9, 10 4, 6, 7, 8, 9, 10 4, 5, 7, 8, 9, 10 4, 5, 6, 7, 9, 10 4, 5, 6, 7, 8, 10 4, 5, 6, 7, 8, 9	1	14
"NOR" Logical "0" Output Voltage	V _{OL}	1, 2, 3† ↓	-	4 5 6 8 9 10	-	5, 6, 7, 8, 9, 10 4, 6, 7, 8, 9, 10 4, 5, 7, 8, 9, 10 4, 5, 6, 7, 9, 10 4, 5, 6, 7, 8, 10 4, 5, 6, 7, 8, 9	-	14
"OR" Logical "1" Output Voltage‡	V _{OH‡}	11, 12, 13‡ ↓	-	4 5 6 8 9 10	-	5, 6, 7, 8, 9, 10 4, 6, 7, 8, 9, 10 4, 5, 7, 8, 9, 10 4, 5, 6, 7, 9, 10 4, 5, 6, 7, 8, 10 4, 5, 6, 7, 8, 9	2	14
"OR" Logical "0" Output Voltage	V _{OL}	11, 12, 13‡ ↓	4 5 6 8 9 10	-	-	5, 6, 7, 8, 9, 10 4, 6, 7, 8, 9, 10 4, 5, 7, 8, 9, 10 4, 5, 6, 7, 9, 10 4, 5, 6, 7, 8, 10 4, 5, 6, 7, 8, 9	-	14
Switching Times						V _{EE} = -4.0 Vdc		(+12V)
Propagation Delay (Fan-Out = 3)				Pulse In	Pulse Out			
t ₄₊₁₋	1		4		1		1, 6, 7, 8, 9, 10	14
t ₄₋₁₊	1				1			
t ₄₊₁₁₊	11				1			
t ₄₋₁₁₋	11				1			
(Fan-Out = 15)								
t ₄₋₁₋	1				1			
t ₄₋₁₊	1				1			
t ₄₊₁₁₊	11				11			
t ₄₋₁₁₋	11				11			
Rise Time (Fan-Out = 3)								
t ₁₊	1				1			
t ₁₁₊	11				11			
Fall Time (Fan-Out = 3)								
t ₁₋	1				1			
t ₁₁₋	11				11			

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MC1001 thru MC1003, MC1201 thru MC1203 (continued)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



APPLICATIONS INFORMATION

The MC1001-1003/MC1201-1203 6-input OR/NOR gates are extremely useful in generating multiple wired-OR logic functions since six independent outputs are provided. (An example is shown in Figure 1.) The gate performs well as a clock driver with the multiple outputs which result in three times the normal fan-out for a given clock waveform. If twisted pair lines are being used for clock distribution in a system, the gate will drive three independent twisted pair lines, each with the same clock waveform.

An output impedance of about 2 ohms is obtained if three OR or NOR outputs are tied together. This provides an excellent 50-ohm driving capability. The 50-ohm line or coax should be terminated in its characteristic impedance to a nominal -2.0 V. This prevents excessively high output current that would pull the logic "1" level below nominal (see Figure 2).

FIGURE 1 - MECL II "WIRED OR" FEATURE

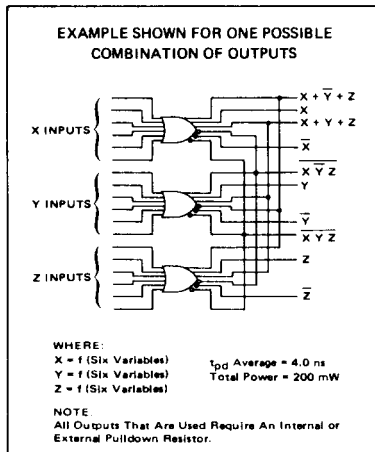


FIGURE 2 - MC1003/MC1203 AS A 50-OHM DRIVER WITH NOMINAL MECL LOGIC LEVELS

