MC14007UB

Dual Complementary Pair Plus Inverter

The MC14007UB multipurpose device consists of three N−Channel and three P−Channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse−shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Antistatic precautions must be taken.
- Pb−Free Packages are Available

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8 second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: − 7.0 mW/°C from 65°C 5o 125°C.

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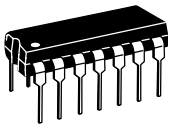
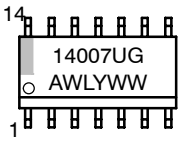
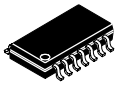
MARKING DIAGRAMS



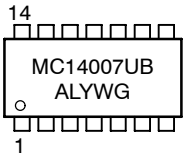
PDIP−14
P SUFFIX
CASE 646

SOIC−14
D SUFFIX
CASE 751A



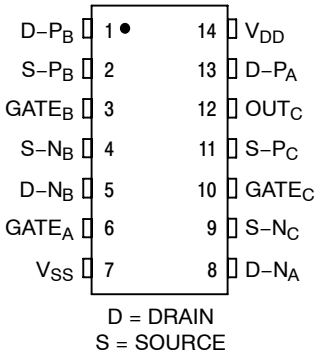


SOEIAJ−14
F SUFFIX
CASE 965



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Indicator

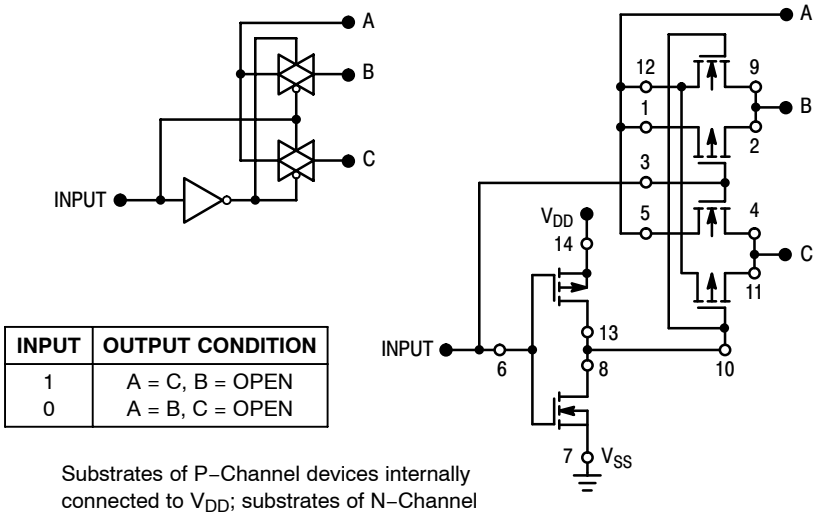
PIN ASSIGNMENT



D = DRAIN
S = SOURCE

ORDERING INFORMATION

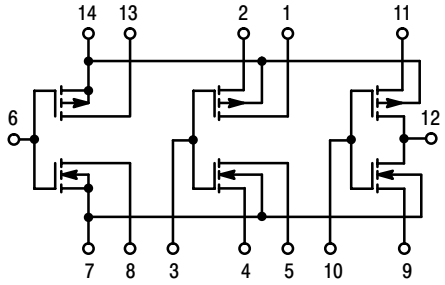
See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.



INPUT	OUTPUT CONDITION
1	A = C, B = OPEN
0	A = B, C = OPEN

Substrates of P−Channel devices internally connected to V_{DD}; substrates of N−Channel devices internally connected to V_{SS}.

Figure 1. Typical Application: 2−Input Analog Multiplexer



V_{DD} = PIN 14
V_{SS} = PIN 7

Figure 2. Schematic

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

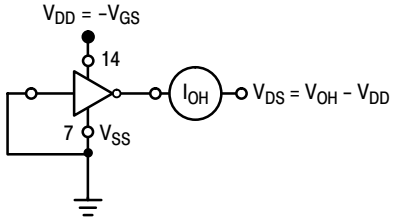
Symbol	Characteristic	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
V_{OL}	Output Voltage "0" Level V_{in} = V_{DD} or 0	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{OH}	V_{in} = 0 or V_{DD} "1" Level	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
V_{IL}	Input Voltage "0" Level (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	 5.0 10 15	 – – –	 1.0 2.0 2.5	 – – –	 2.25 4.50 6.75	 1.0 2.0 2.5	 – – –	 1.0 2.0 2.5	Vdc
V_{IH}	(V_O = 0.5 Vdc) "1" Level (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	5.0 10 15	4.0 8.0 12.5	– – –	4.0 8.0 12.5	2.75 5.50 8.25	– – –	4.0 8.0 12.5	– – –	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	 5.0 5.0 10 15	 –3.0 –0.64 –1.6 –4.2	 – – – –	 –2.4 –0.51 –1.3 –3.4	 –5.0 –1.0 –2.5 –10	 – – – –	 –1.7 –0.36 –0.9 –2.4	 – – – –	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	1.0 2.5 10	– – –	0.36 0.9 2.4	– – –	mAdc
I_{in}	Input Current	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
C_{in}	Input Capacitance (V_{in} = 0)	–	–	–	–	5.0	7.5	–	–	pF
I_{DD}	Quiescent Current (Per Package)	5.0 10 15	– – –	0.25 0.5 1.0	– – –	0.0005 0.0010 0.0015	0.25 0.5 1.0	– – –	7.5 15 30	μAdc
I_T	Total Supply Current (Notes 3 and 4) (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	5.0 10 15	I_T = (0.7 μA/kHz) f + I_{DD}/6 I_T = (1.4 μA/kHz) f + I_{DD}/6 I_T = (2.2 μA/kHz) f + I_{DD}/6							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L - 50)$ Vfk
   where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

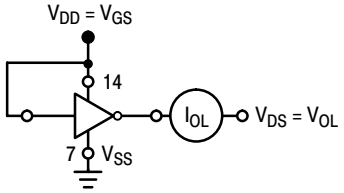
SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
t_{TLH}	Output Rise Time					ns
	t_{TLH} = (1.2 ns/pF) C_L + 30 ns	5.0	–	90	180	
	t_{TLH} = (0.5 ns/pF) C_L + 20 ns	10	–	45	90	
	t_{TLH} = (0.4 ns/pF) C_L + 15 ns	15	–	35	70	
t_{THL}	Output Fall Time					ns
	t_{THL} = (1.2 ns/pF) C_L + 15 ns	5.0	–	75	150	
	t_{THL} = (0.5 ns/pF) C_L + 15 ns	10	–	40	80	
	t_{THL} = (0.4 ns/pF) C_L + 10 ns	15	–	30	60	
t_{PLH}	Turn−Off Delay Time					ns
	t_{PLH} = (1.5 ns/pF) C_L + 35 ns	5.0	–	60	125	
	t_{PLH} = (0.2 ns/pF) C_L + 20 ns	10	–	30	75	
	t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns	15	–	25	55	
t_{PHL}	Turn−On Delay Time					ns
	t_{PHL} = (1.0 ns/pF) C_L + 10 ns	5.0	–	60	125	
	t_{PHL} = (0.3 ns/pF) C_L + 15 ns	10	–	30	75	
	t_{PHL} = (0.2 ns/pF) C_L + 15 ns	15	–	25	55	

5. The formulas given are for the typical characteristics only. Switching specifications are for device connected as an inverter.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



All unused inputs connected to ground.



All unused inputs connected to ground.

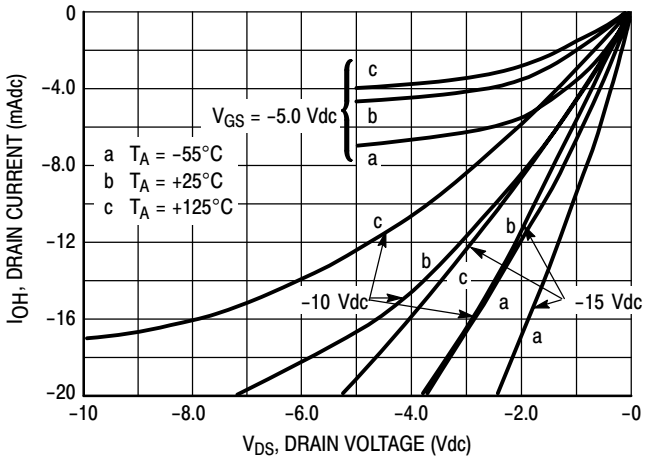


Figure 3. Typical Output Source Characteristics

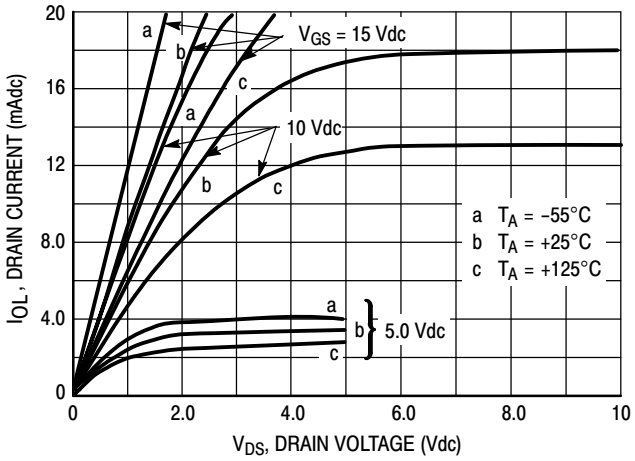


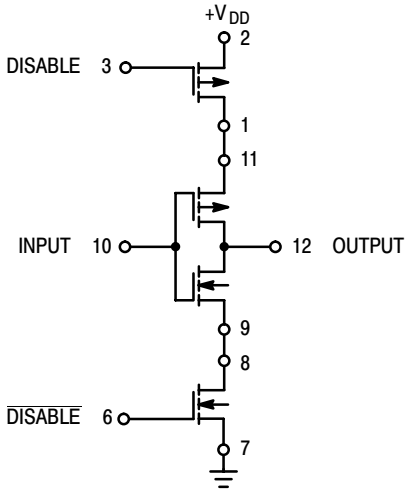
Figure 4. Typical Output Sink Characteristics

These typical curves are not guarantees, but are design aids.
Caution: The maximum current rating is 10 mA per pin.

Figure 5. Switching Time and Power Dissipation Test Circuit and Waveforms

APPLICATIONS

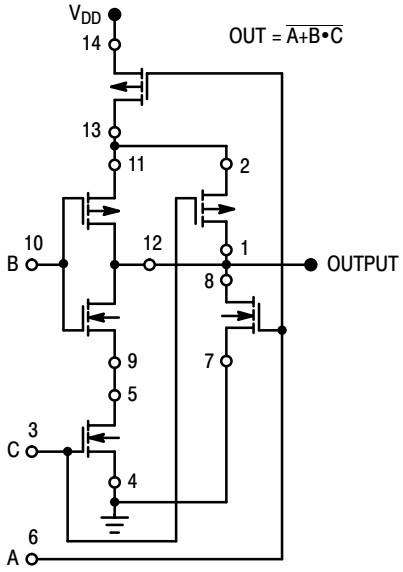
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 6, and 7 are a few examples of the device flexibility.



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	OPEN

X = Don't Care

Figure 6. 3−State Buffer



Substrates of P−Channel devices internally connected to V_{DD};
Substrates of N−Channel devices internally connected to V_{SS}.

Figure 7. AOI Functions Using Tree Logic

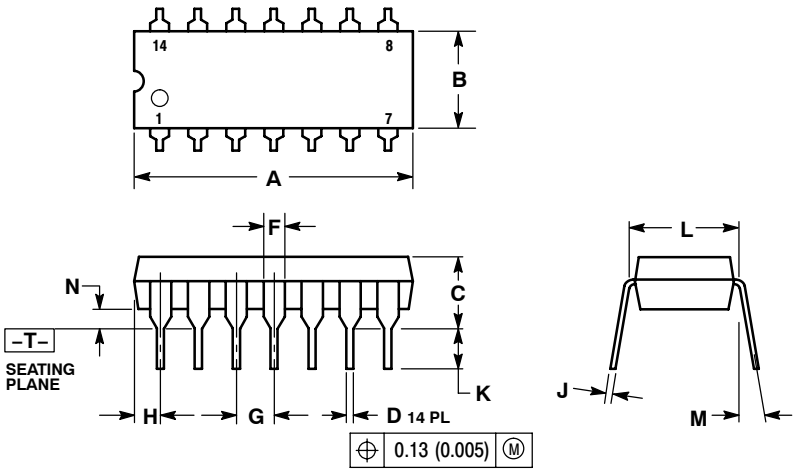
ORDERING INFORMATION

Device	Package	Shipping†
MC14007UBCP	PDIP−14	25 Units / Rail
MC14007UBCPG	PDIP−14 (Pb−Free)	
MC14007UBD	SOIC−14	55 Units / Rail
MC14007UBDG	SOIC−14 (Pb−Free)	
MC14007UBDR2	SOIC−14	2500 / Tape & Reel
MC14007UBDR2G	SOIC−14 (Pb−Free)	
MC14007UBFEL	SOEIAJ−14	2000 / Tape & Reel
MC14007UBFELG	SOEIAJ−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P

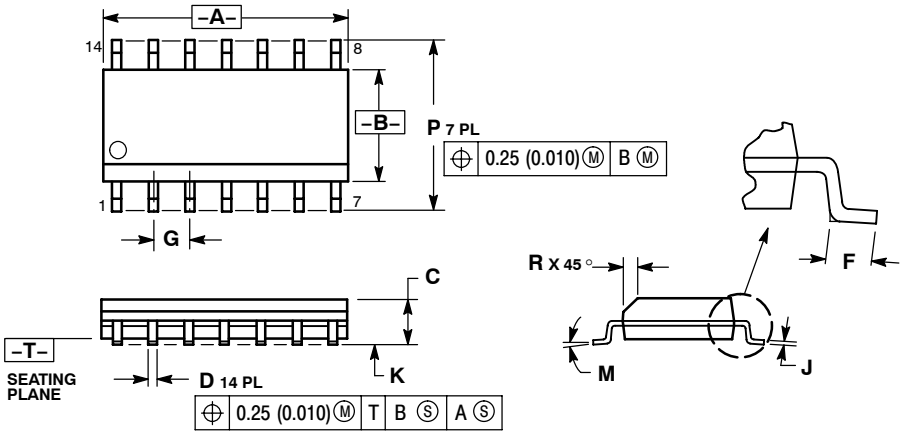


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01

PACKAGE DIMENSIONS

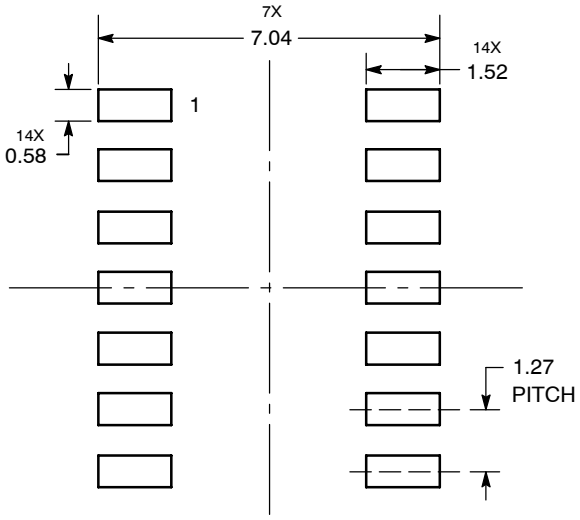
SOIC−14
CASE 751A−03
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

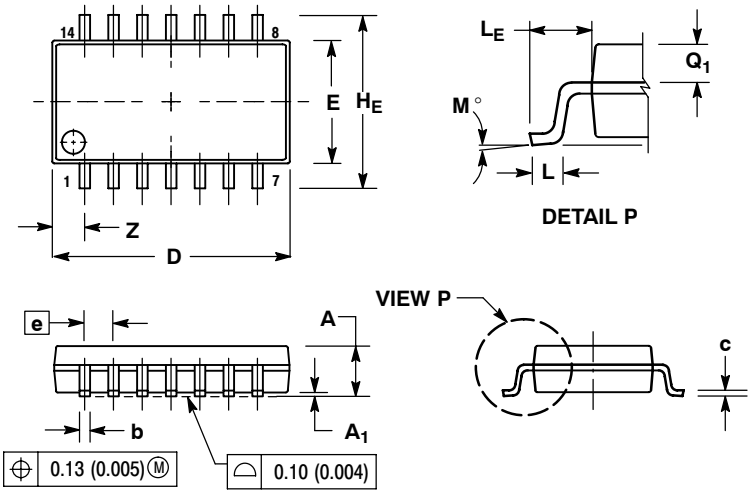


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOEIAJ−14
CASE 965−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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P.O. Box 5163, Denver, Colorado 80217 USA
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MC14007UB/D