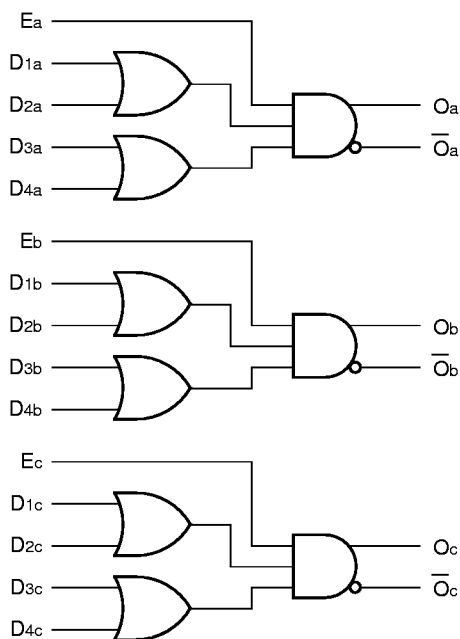


FEATURES

- Max. propagation delay of 900ps
- IEE min. of -48mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- Approximately 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPAC and 28-pin PLCC package

BLOCK DIAGRAM



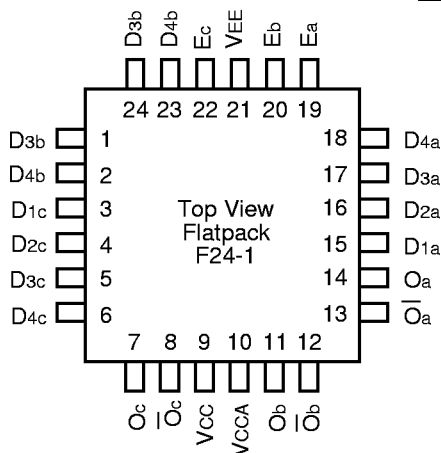
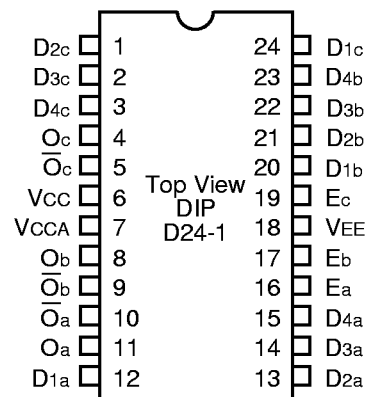
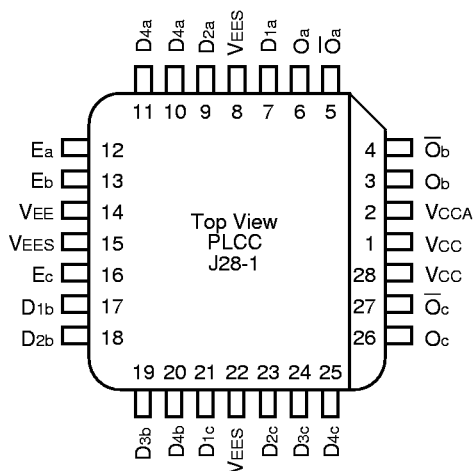
PIN NAMES

Pin	Function
D _{na} – D _{nc}	Data Inputs (n = 1...4)
E _a – E _c	Enable Inputs
O _a – O _c	Data Outputs
\bar{O}_a – \bar{O}_c	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

DESCRIPTION

The SY100S317 is a set of ultra-fast, triple 2-wide OR/AND gates designed for use in high-performance ECL systems. This device offers both true and complement outputs. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	$V_{IN} = V_{IH} (Max.)$
I _{EE}	Power Supply Current	-48	-32	-22	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	300	1100	300	1100	300	1100	ps	
t _{PLH} t _{PHL}	Propagation Delay Enable to Output	300	900	300	900	300	900	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

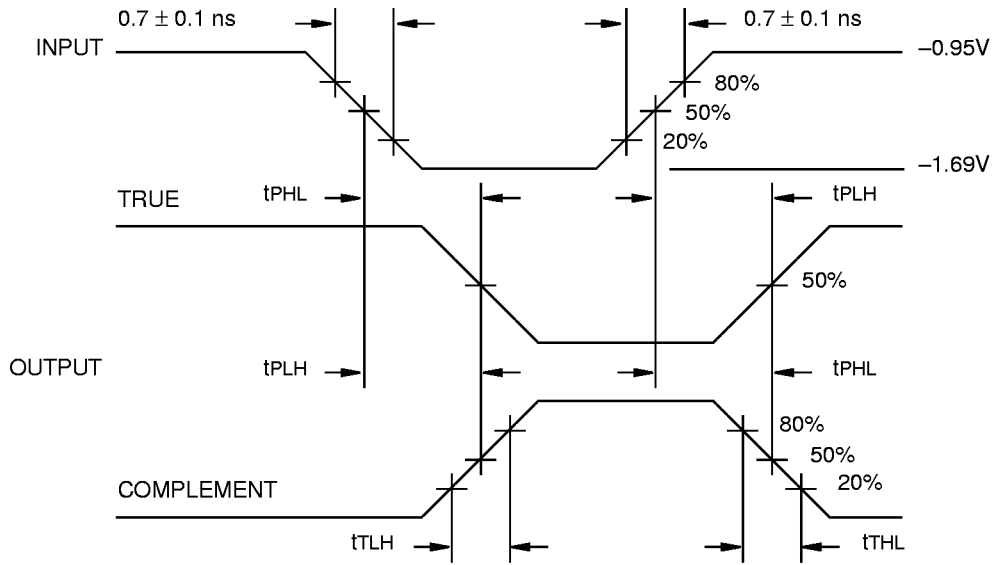
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	300	1000	300	1000	300	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay Enable to Output	300	800	300	800	300	800	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps	
t _{PLH} t _{PHL}	Propagation Delay Enable to Output	300	700	300	700	300	700	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S317DC	D24-1	Commercial
SY100S317FC	F24-1	Commercial
SY100S317JC	J28-1	Commercial
SY100S317JCTR	J28-1	Commercial

24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERTED DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

NOTES:
 1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

SYNERGY SEMICONDUCTOR
 3250 SCOTT BOULEVARD
 SANTA CLARA, CA, 95054
 TEL: 408-960-9191
 FAX: 408-587-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO		
RELEASE DATE:				

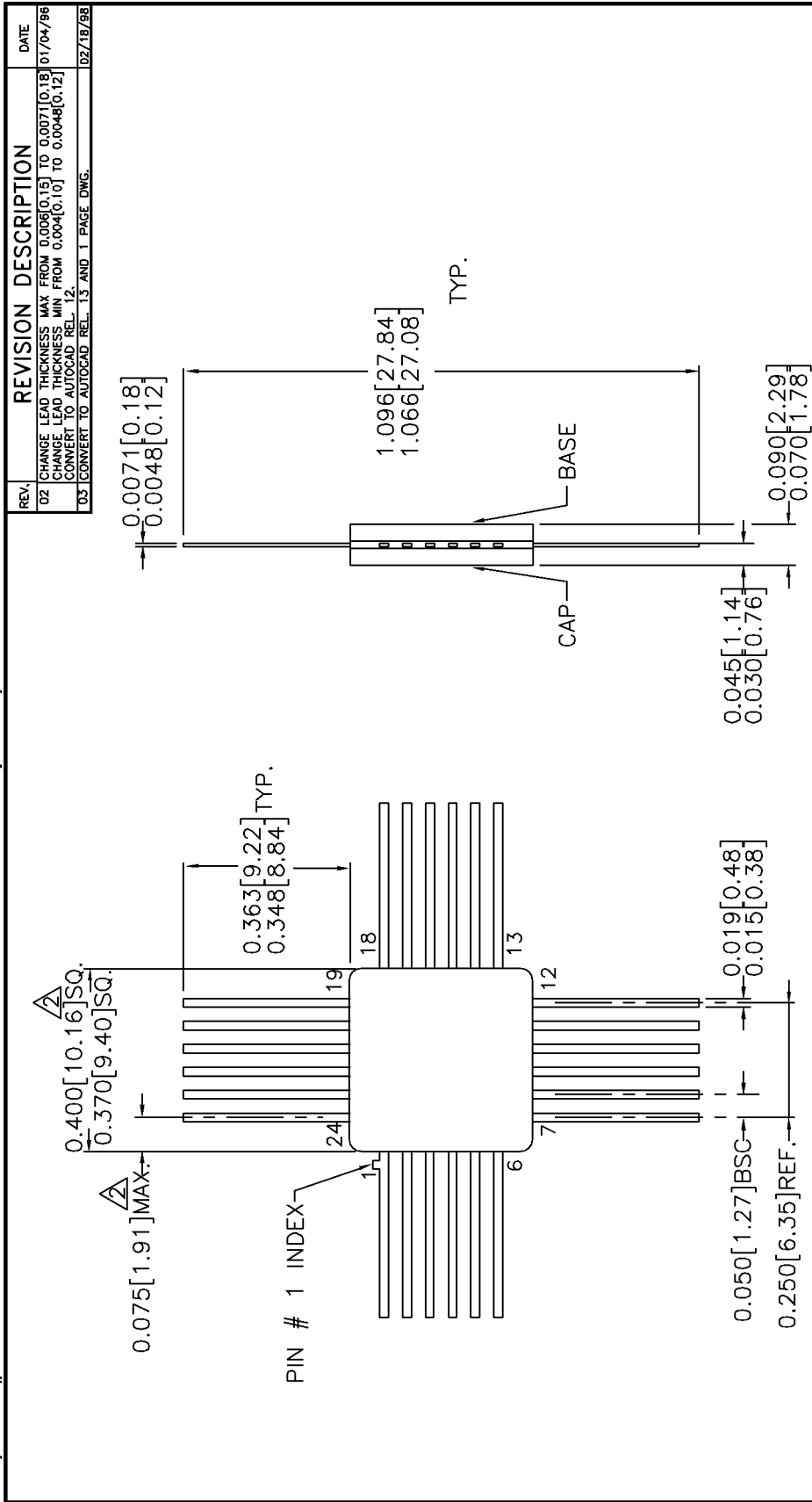
THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE TO BE BASED ON THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.

24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-960-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	N/A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					REVISION 03

24 LEAD CERPACK
PACKAGE OUTLINE

THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR, ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

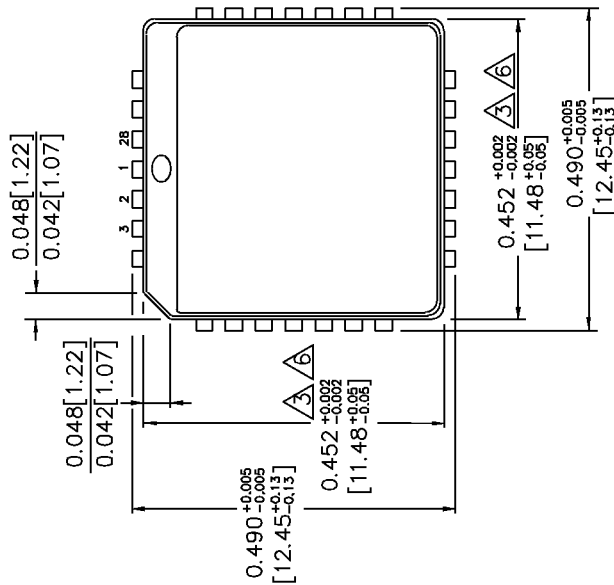
FILE/REV #: PD0008A03

PD/0008/ASCORP

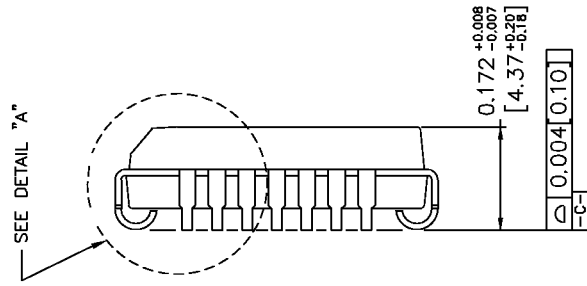
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

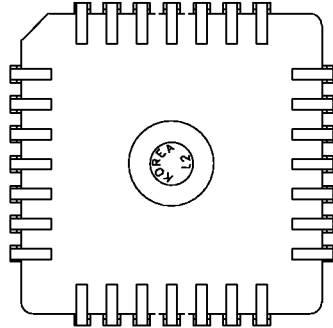
TOP VIEW



SIDE VIEW



BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



3250 SCOTT BOULEVARD
SANTA CLARA, CA. 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: TERMIN G. LIRRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	28 LEAD PLCC PACKAGE OUTLINE
CHK'D: RON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR. ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.
RELEASE DATE:					N/A REVISION 03

DETAIL "A"