LPTTL/SSI 9L04
LOW POWER HEX INVERTER

DESCRIPTION – The low power TTL/SSI 9L04 consists of six TTL gates, each performing a single inversion function. Designed for low power, medium speed operation, the 9L04 is very useful where a number of complement signals are desired simultaneously.

- **TYPICAL PROPAGATION DELAY OF 20 ns**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

INPUTS (Pins 1, 3, 5, 9, 11, 13)
OUTPUTS (Pins 2, 4, 6, 8, 10, 12)

LOADING

HIGH	LOW
0.5 U.L.	0.25 U.L.
10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

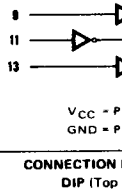
SCHEMATIC DIAGRAM

* Input Clamp Diode

TYPICAL RESISTOR VALUES

R_1 = 16 kΩ R_3 = 6 kΩ R_5 = 16 kΩ
R_2 = 5 kΩ R_4 = 600 Ω R_6 = 320 Ω

LOGIC SY



V_{CC} = P
GND = P

CONNECTION
DIP (Top

FLATPAK

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65 C to +150
Temperature (Ambient) Under Bias	-55 C to +125
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0
*Input Voltage (dc)	-0.5 V to +5.5
*Input Current (dc)	-30 mA to +5.0
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} va
Output Current (dc) (Output LOW)	+30

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATU
	MIN.	TYP	MAX.	
9L04XM	4.5 V	5.0 V	5.5 V	-55 C to 125
9L04XC	4.75 V	5.0 V	5.25 V	0 C to 75

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this prod

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE NOTED) (See Notes 1 &

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. Note 3	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = -0.4 mA, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH}
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all in
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input logical LOW voltage for all inp
I_{IL}	Input LOW Current		-0.25	-0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 4)	Output Short Circuit Current	-10	-22	-40	mA	V_{CC} = MAX., V_{OUT} = 0.00 V, Inputs grounded
I_{CC}	Power Supply Current per Gate		0.9	1.56	mA	V_{CC} = MAX., Input HIGH
			0.28	0.45	mA	V_{CC} = MAX., Input LOW

NOTES: 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur a temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the able system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25 C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		15		ns	V_{CC} = 5.0V See F
t_{PHL}	Turn On Delay Input to Output		25		ns	C_L = 15 pF

SWITCHING TIME WAVEFORM

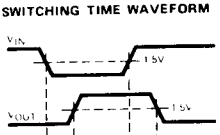


Fig. 1