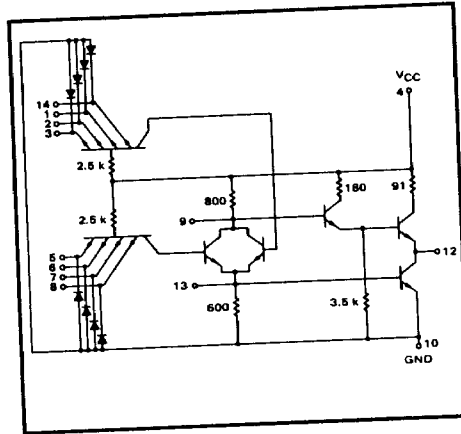


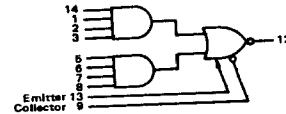
EXPANDABLE  
2-WIDE 4-INPUT  
"AND-OR-INVERT" GATE

MTTL II MC2100/2000 series

MC2100 • MC2150  
MC2000 • MC2050



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds. This gate is usable for construction of half adders and other applications where the exclusive OR function is required.



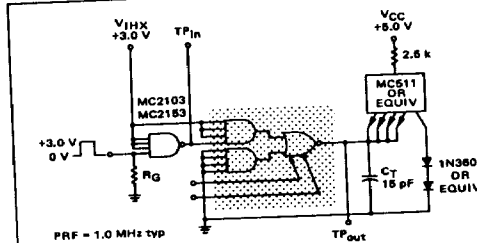
Positive Logic:  
 $12 = (1 + 2 + 3 + 14) + (5 + 6 + 7 + 8) + (\text{Expanders})$

Negative Logic:  
 $12 = (1 + 2 + 3 + 14) + (5 + 6 + 7 + 8) + (\text{Expanders})$

Total Power Dissipation = 27 mW typ/Pkgs  
Propagation Delay Time = 7.0 ns typ

SERIES	INPUT LOADING FACTOR (I <sub>F</sub> )	OUTPUT DRIVE (I <sub>OL</sub> )	TEMPERATURE RANGE	
MC2100 MC2150	1	11 MC2100 series Gates 6 MC2100 series Gates	22 mA 12 mA	-55°C to +125°C
MC2000 MC2050	1	9 MC2000 series Gates 5 MC2000 series Gates	22.5 mA 12.5 mA	

SWITCHING TIME TEST CIRCUIT

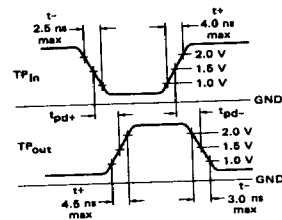


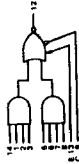
PRF = 1.0 MHz typ  
PW = 200 ns  
t<sub>r</sub> = 5.0 ns max  
t<sub>f</sub> = 5.0 ns max

NOTES:

- R<sub>G</sub> = 50 ohms
- C<sub>T</sub> = the total parasitic capacitance which includes probe, wiring, and load capacitances.
- Scope rise time < 1.0 ns
- Probe capacitance < 5.0 pF
- Expander pins should be left open when measuring switching times.

VOLTAGE WAVEFORMS AND DEFINITIONS





**ELECTRICAL CHARACTERISTICS**  
 Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.

Characteristic	Pin Under Test	MC2100, MC2150 Test Limits						MC2000, MC2050 Test Limits						TEST CONDITIONS																			
		-55°C		+25°C		+125°C		-25°C		0°C		+75°C		mA				Volts															
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	I <sub>CC</sub>	I <sub>SD</sub>	I <sub>PR</sub>	I <sub>OLK</sub>	I <sub>IN</sub>	V <sub>IN</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>OL</sub>	V <sub>OH</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>			
Input Forward Current	I <sub>F</sub>	1	-2.0	-2.0	-2.0	-2.0	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	2.3.14	-	-	-	-	-	-	-	-	-	-	-	-	-	1.5, 8.7, 8.10
Leakage Current	I <sub>R</sub>	1	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-	-	-	-	-	-	-	-	-	-	-	-	-	2.3, 5.6, 7, 8.10, 14	
Inverse Beta Current	I <sub>IB</sub>	1	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-	-	-	-	-	-	-	-	-	-	-	-	-	5.6, 7, 8, 10	
Breakdown Voltage	BV <sub>IN(1)</sub> BV <sub>IN(12)</sub>	1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	5.6, 7, 8, 10	
Output Voltage	V <sub>OUT(1)</sub> V <sub>OUT(12)</sub>	12	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	-	-	-	-	-	-	-	-	-	-	-	-	-	-	5.6, 7, 8, 10	
Leakage Current	I <sub>OLK</sub>	12	2.5	2.4	2.5	2.5	2.5	2.4	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	12	-	-	-	-	-	-	-	-	-	-	-	-	-	5.6, 7, 8, 10	
Short-Circuit Current	I <sub>SC</sub>	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-	-	-	-	-	-	-	-	-	-	-	-	-	7.8, 10, 14	
Output Voltage	V <sub>OL</sub> V <sub>OH</sub>	12	0.40	0.40	0.40	0.45	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	12	-	-	-	-	-	-	-	-	-	-	-	-	-	5.6, 7, 8, 10	
Power Requirements (Total Device)	I <sub>max</sub>	4	-	-	10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1.2, 3.5, 6, 7.8, 10, 14	
Maximum Power Supply Current	I <sub>PDH</sub> I <sub>PDL</sub>	4	9.0	9.0	9.0	9.0	12	12	12	12	12	12	12	12	12	12	12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1.2, 3.5, 6, 7.8, 10, 14
Power Supply Drain	I <sub>DD</sub>	4	9.0	9.0	9.0	9.0	12	12	12	12	12	12	12	12	12	12	12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1.2, 3.5, 6, 7.8, 10, 14
Switching Parameters	t <sub>pd</sub>	1, 12	-	-	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.3, 14, 5.6, 7, 8, 10	
Turn-On Delay	t <sub>pd</sub>	1, 12	-	-	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.3, 14, 5.6, 7, 8, 10	
Turn-Off Delay	t <sub>pd</sub>	1, 12	-	-	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.3, 14, 5.6, 7, 8, 10	
Rate Time	t <sub>r</sub>	1, 12	-	-	4.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.3, 14, 5.6, 7, 8, 10	
Fall Time	t <sub>f</sub>	1, 12	-	-	3.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2.3, 14, 5.6, 7, 8, 10	

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Pin-out and Package Information

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
WT	45	L13	nc	103	
X/Y	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Power Supply	Circuit Supplied
63	L8	VCCN	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			