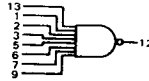
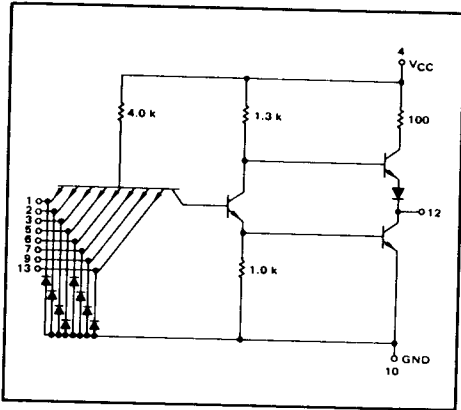


8-INPUT "NAND" GATE

MTTL I MC500/400 series

MC502 · MC552
MC402 · MC452

This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.



Positive Logic:
 $12 = \overline{1 + 2 + 3 + 5 + 6 + 7 + 9 + 13}$
 Negative Logic:
 $12 = \overline{1 + 2 + 3 + 5 + 6 + 7 + 9 + 13}$

Total Power Dissipation = 15 mW typ/pkg
 Propagation Delay Time = 12 ns typ

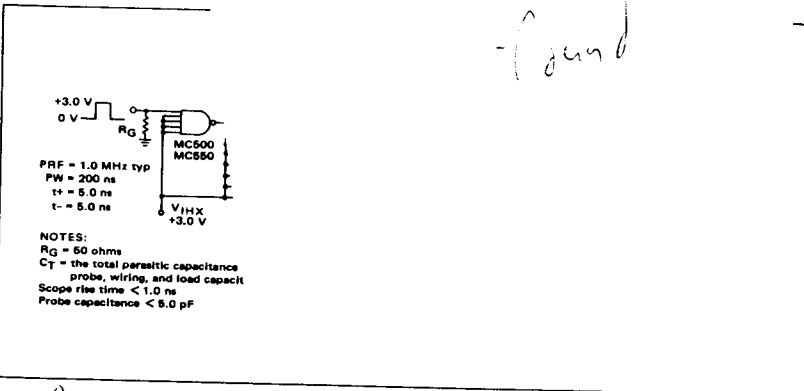
TYPE NO.	INPUT LO
MC502	
MC552	
MC402	
MC452	

MC402

RANGE
°C

MC
(ground)

SWITCHING

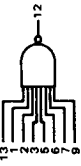


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MC502, MC552/MC402, MC452 (continued)

ELECTRICAL CHARACTERISTICS		TEST CONDITIONS																			
		mA						Volts													
		I_{Ox}	I_{OH}	I_{LH}	I_{LH}^{std}	I_{in}	I_{in}	V_{IH}	V_{IL}	V_{OL}	V_{OH}	$V_{IH(1)}$	$V_{IH(0)}$	$V_{OH(1)}$	$V_{OH(0)}$						
		Pr ¹	Std	Pr ¹	Std	Pr ¹	Std	Pr ¹	Std	Pr ¹	Std	Pr ¹	Std	Pr ¹	Std						
		TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																			
Characteristic	Symbol	Pin Under Test	MC502		MC552		Test Limits		MC402		MC452		Test Limits		Unit						
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max									
Input	Forward Current	I_F	1	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mADC						
			12	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0							
Leakage Current	I_L	1	1	100	-	100	-	100	-	100	-	100	-	100	μ Adc						
			12	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0						
Breakdown Voltage	$BV_{in}^{(+)}$	1	-	5.5	-	5.5	-	Vdc	-	5.5	-	Vdc	-	Vdc							
			12	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0							
Output	Output Voltage	$V_{out}^{(+)}$	12	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc						
			12	2.5	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc							
Leakage Current	I_{OLK}	12	250	-	250	-	250	-	250	-	250	-	250	μ Adc							
			12	10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mADC							
Short-Circuit Current	I_{SC}	12	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	Vdc							
			12	2.8	3.2	3.0	3.1	3.15	3.15	Vdc	12	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5
Power Requirements (Total Device)	Maximum Power Supply Current	I_{max}	-	-	10	-	-	-	10	-	-	-	-	mADC							
			4	6.0	6.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	mADC							
Switching Parameters	Turn-On Delay	$t_{pd}^{(1)}$	1, 12	-	24	-	-	-	24	-	-	-	ns								
			1, 12	-	20	-	-	-	20	-	-	-	ns								
Fail Time	t_r	1, 12	-	8.0	-	8.0	-	8.0	-	8.0	-	8.0	ns								
			1, 12	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	ns							
Pulse Parameters	Pulse In	Pulse Out																			
			1, 12																		
Power Requirements (Total Device)	Maximum Power Supply Current	I_{max}	4	-	-	-	-	10	-	-	-	-	4								
			4	6.0	6.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0								
Switching Parameters	Turn-On Delay	$t_{pd}^{(1)}$	1, 12	-	24	-	-	-	24	-	-	-	ns								
			1, 12	-	20	-	-	-	20	-	-	-	ns								
Fail Time	t_r	1, 12	-	8.0	-	8.0	-	8.0	-	8.0	-	8.0	ns								
			1, 12	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0								



Test procedures are shown for only one input of the gate. To complete testing, sequence through remaining inputs in the same manner.

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