MC14069UB

Hex Inverter

The MC14069UB hex inverter is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin–for–Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	− 0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	− 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	− 55 to +125	°C
T_{stg}	Storage Temperature Range	− 65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq$ (V_{in} or V_{out}) $\leq V_{DD}$.
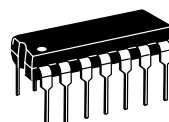
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
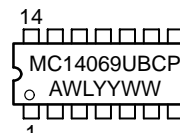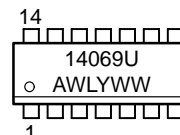
ON Semiconductor™

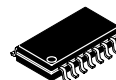**http://onsemi.com**

MARKING DIAGRAMS

PDIP–14
P SUFFIX
CASE 646

14
MC14069UBCP
AWLYYWW
1

SOIC–14
D SUFFIX
CASE 751A

14
14069U
AWLYWW
1

TSSOP–14
DT SUFFIX
CASE 948G

14
14
069U
ALYW
1

EIAJ SO–14
F SUFFIX
CASE 965

14
MC14069UB
ALYW
1
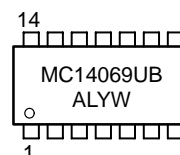
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14069UBCP	PDIP–14	2000/Box
MC14069UBD	SOIC–14	2750/Box
MC14069UBDR2	SOIC–14	2500/Tape & Reel
MC14069UBDT	TSSOP–14	96/Rail
MC14069UBDTEL	TSSOP–14	2000/Tape & Reel
MC14069UBDTR2	TSSOP–14	2500/Tape & Reel
MC14069UBF	EIAJ SO–14	See Note 1.
MC14069UBFEL	EIAJ SO–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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Figure 1. Pin Assignment
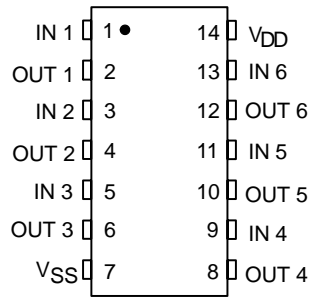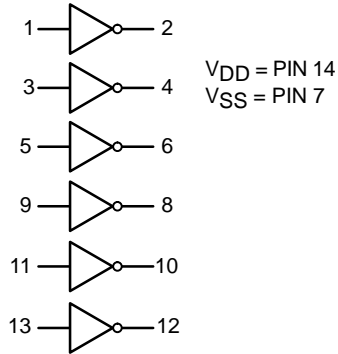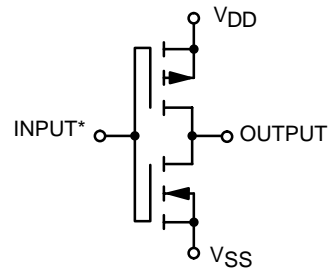

V_{DD} = PIN 14
V_{SS} = PIN 7

Figure 3. Logic Diagram

*Double diode protection on all inputs not shown

Figure 2. Circuit Schematic
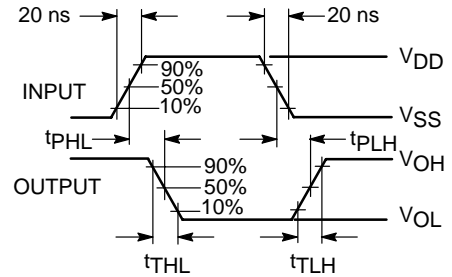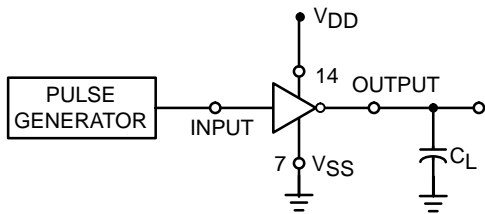
(1/6 of circuit shown)

Figure 4. Switching Time Test Circuit and Waveforms

MC14069UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
$V_{in} = 0$ "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.0 2.0 2.5	— — —	2.25 4.50 6.75	1.0 2.0 2.5	— — —	1.0 2.0 2.5	Vdc
"1" Level (V_O = 0.5 Vdc) (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	V_{IH}	5.0 10 15	4.0 8.0 12.5	— — —	4.0 8.0 12.5	2.75 5.50 8.25	— — —	4.0 8.0 12.5	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0 10 15	I_T = (0.3 µA/kHz) f + I_{DD}/6 I_T = (0.6 µA/kHz) f + I_{DD}/6 I_T = (0.9 µA/kHz) f + I_{DD}/6							µAdc
Output Rise and Fall Times (5.) (C_L = 50 pF) t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	— — —	100 50 40	200 100 80	— — —	— — —	ns
Propagation Delay Times (5.) (C_L = 50 pF) t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 22 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 17 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	— — —	— — —	65 40 30	125 75 55	— — —	— — —	ns

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.