

IVCR2401 25V 4A Sink and Source Dual-Channel Driver

1. Features

- Industry standard SOIC-8 pinout
- Two independent gate drive channels
- 4A sink and source peak drive current
- Wide VDD range up to 25V
- Separated enable inputs
- Two channels in parallel for high current driving
- Enhanced parallel accuracy with floating one enable pin
- VDD UVLO protection
- TTL and CMOS compatible input
- Low propagation delays (45ns typical) with build-in de-glitch filter
- 1ns typical delay matching between two channels
- Outputs held low when floating inputs
- SOIC-8 with exposed pad for high frequency and power applications
- Operating temperature range -40°C to 125°C

2. Applications

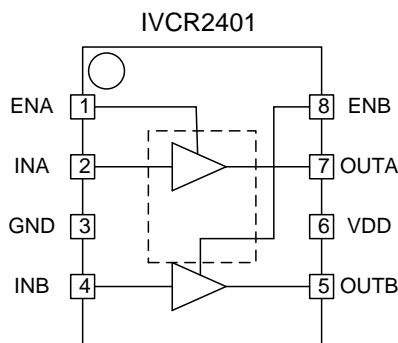
- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- EV/HEV inverters and DC/DC converters
- PV boosters and inverters
- UPS

The IVCR2401 is a 4A dual-channel, high-speed, low-side gate driver, capable of effectively and safely driving MOSFETs and IGBTs. Low propagation delay and mismatch with an optional exposed pad SOIC-8 package enables MOSFETs to switch at hundreds of kHz. It is very suitable for server and telecom power supply's synchronous rectification driving, where synchronous MOSFET's dead time accuracy directly impacts converter's efficiency. The driver is capable to parallel two channels to increase output driving current. When only one enable pin is tied to logic high, both channel's output stages are driven by the same logic signal. This unique feature reduces two channels' mismatch significantly and makes the driver very suitable for paralleled switches driving. The input thresholds are based on TTL with voltage tolerance up to 20V.

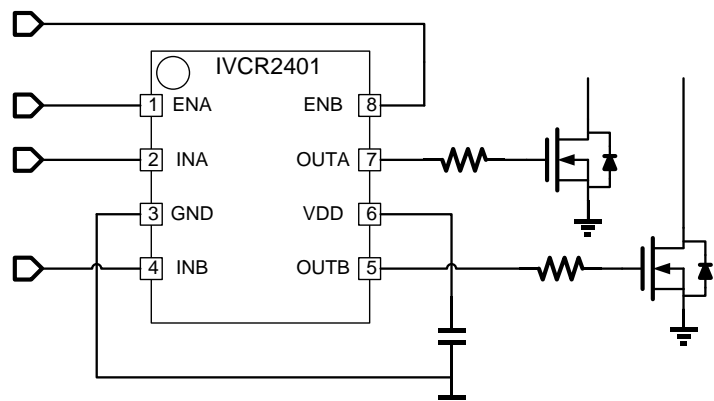
Device Information

PART NUMBER	PACKAGE	PACKING
IVCR2401DR	SOIC-8	Tape and Reel
IVCR2401D	SOIC-8	Tube
IVCR2401DPR	SOIC-8 (EP)	Tape and Reel
IVCR2401DP	SOIC-8 (EP)	Tube

3. Description



Pinout SOIC-8



Typical Application Diagram

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4. Pin Configuration and Functions

PIN	NAME	I/O	DESCRIPTION
1	ENA	I	Channel A enable input
2	INA	I	Channel A input
3	GND	G	Driver ground
4	INB	I	Channel B input
5	OUTB	O	Channel B driver output
6	VDD	P	Positive bias supply
7	OUTA	O	Channel A driver output
8	ENB	I	Channel B enable input
	Exposed pad		Bottom exposed pad is often tied to GND on layout. SOIC-8 (EP) only

5. Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Total supply voltage (reference to GND)	-0.3	25	V
OUTA, B	Gate driver output voltage	-0.3	V _{DD} +0.3	V
I _{OUTH}	Gate driver output source current (at max pulse width 10us and 0.2% duty cycle)		6.6	A
I _{OUTL}	Gate driver output sink current (at max pulse width 10us and 0.2% duty cycle)		6.6	A
INA, INB,	Signal input voltage	-5.0	20	V
ENA, ENB,	Enable input voltage	-0.3	20	V
T _J	Junction temperature	-40	150	°C
T _{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

		Value	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V _{DD}	Total supply voltage	8	20	V
V _{INx, ENx}	Signal input voltage	0	18	V
T _A	Operating ambient temperature range	-40	125	°C

5.4 Thermal Information

		IVCR2401D	IVCR2401DP	UNIT
R _{θJA}	Junction-to-Ambient	112	39	°C/W
R _{θJB}	Junction-to-PCB	53	11	°C/W
R _{θJP}	Junction-to-exposed pad		5.1	°C/W

5.5 Electrical Specifications

Unless otherwise noted, $V_{DD} = 15\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C

Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
I_{DDq}	Quiescent current	$I_N=0\text{V}$		0.75	1.5	mA
UVLO						
V_{ON}	Under voltage thresholds	Rising threshold	6.2	6.7	7.2	V
V_{OFF}		Falling threshold	5.7	6.2	6.7	
INPUT (INA, INB)						
V_{INH}	Input rising threshold		1.6	1.86	2.1	V
V_{INL}	Input falling threshold		1.1	1.4	1.7	V
V_{INHYS}	Input hysteresis			0.4		V
V_{INNS}	Input negative voltage capability		-5			V
ENABLE INPUT (ENA, ENB)						
V_{ENH}	Enable input rising threshold		1.6	1.86	2.1	V
V_{ENL}	Enable input signal threshold		1.1	1.4	1.7	V
V_{INHYS}	Enable input hysteresis			0.4		V
OUTPUTS (OUTA, OUTB)						
$I_o^{(1)}$	Peak source and sink currents	$C_{LOAD} = 0.22\mu\text{F}$, with external current limiting resistors, 1kHz switching frequency		4.0		A
V_{OH}	Output high voltage	$I_{OUTH} = -100\text{mA}$	$V_{DD}-0.3$	$V_{DD}-0.13$		V
V_{OL}	Output low voltage	$I_{OUTL} = 100\text{mA}$		0.08	0.2	V
R_{OH}	Output pull-up resistance			1.3	3	Ω
R_{OL}	Output pull-down resistance			0.8	2	Ω
Timing						
T_{Dff}	Falling delay	Load = 1.8nF	30	45	80	ns
T_{Drr}	Rising delay		30	45	80	
T_f	Fall time	Load = 1.8nF	6	13	20	ns
T_r	Rise time		6	13	20	
$T_{dm}^{(1)}$	Delay mismatch	$I_N=I_{NB}$, $EN_A=5\text{V}$, EN_B floating		1		ns

(1) Ensured by design and characterization, not 100% tested in production.

6. Typical Characteristics

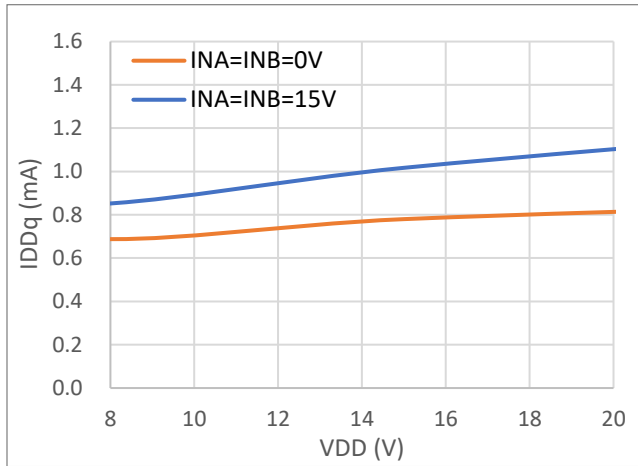


Figure 1. Quiescent Current $IDDq$ vs VDD

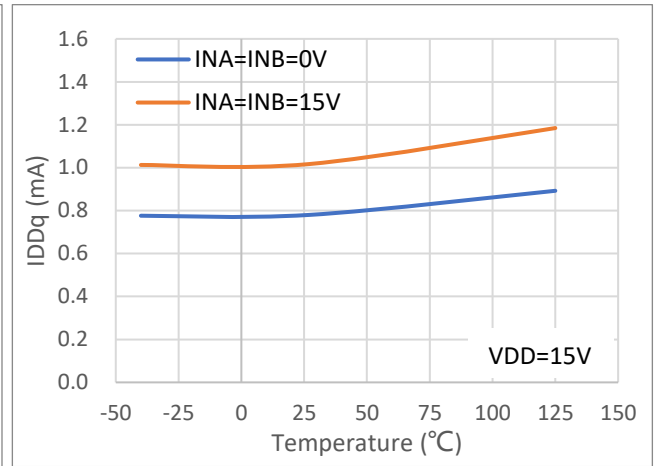


Figure 2. Quiescent Current $IDDq$ vs Temperature

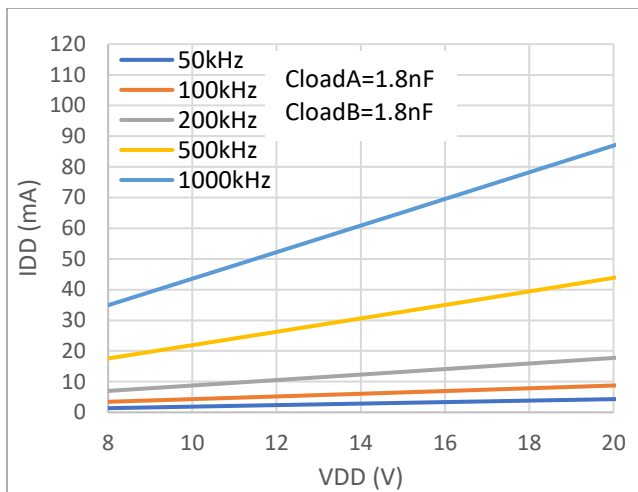


Figure 3. Operating Current IDD vs VDD

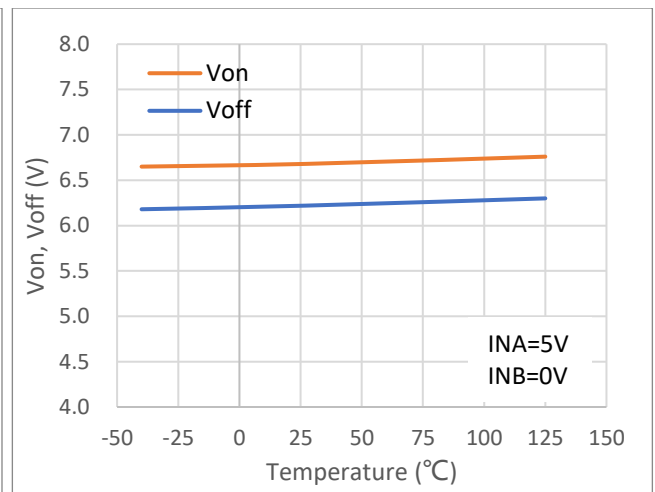


Figure 4. UVLO vs Temperature

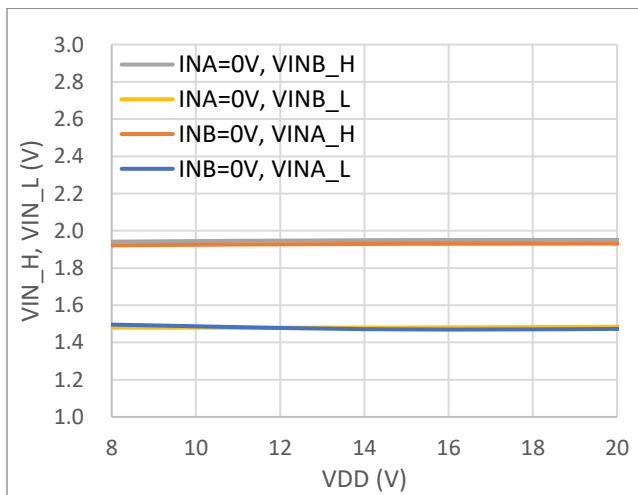


Figure 5. Input Threshold Voltage vs VDD

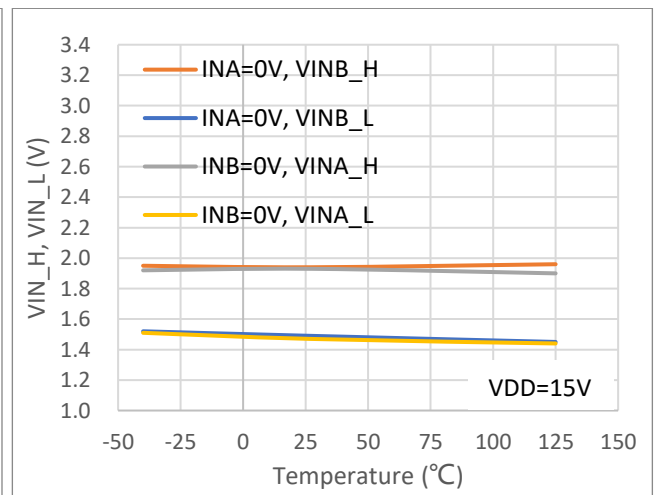


Figure 6. Input Threshold Voltage vs Temperature

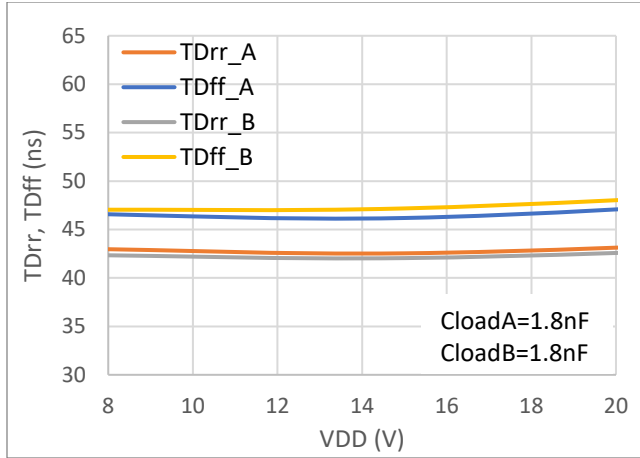


Figure 7. Propagation Delay vs VDD

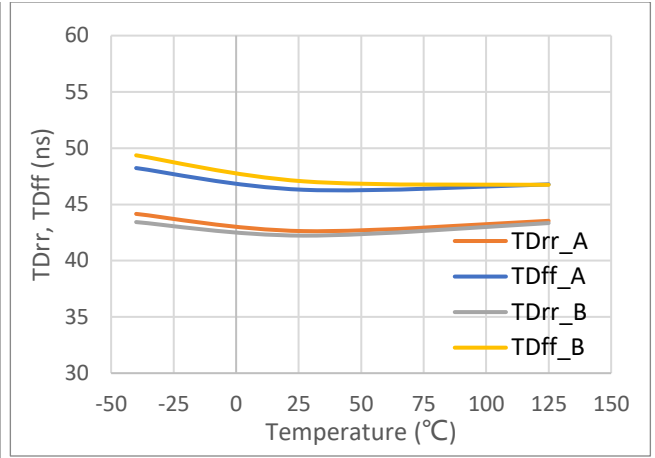


Figure 8. Propagation Delay vs Temperature

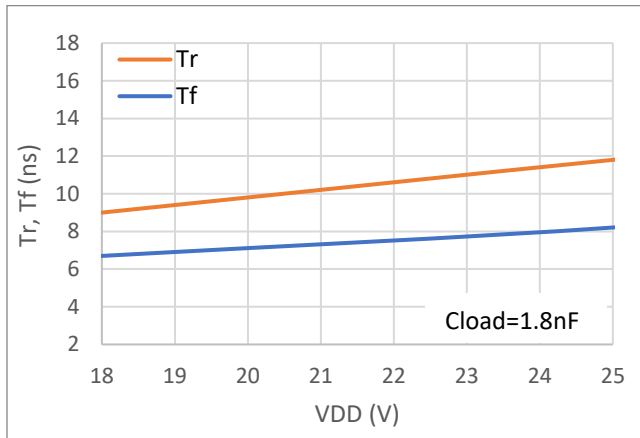


Figure 9. Rise Time and Fall time vs VDD

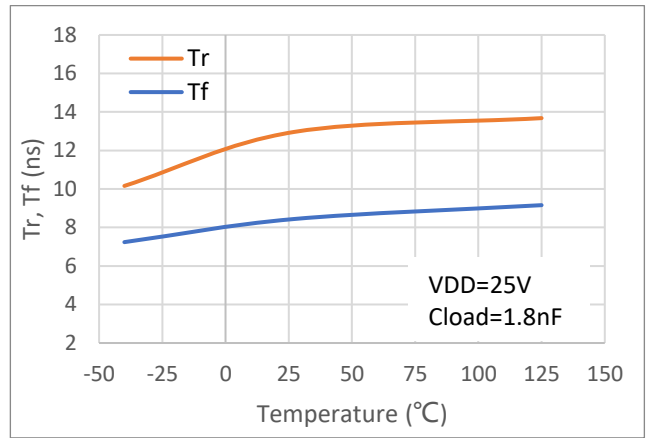


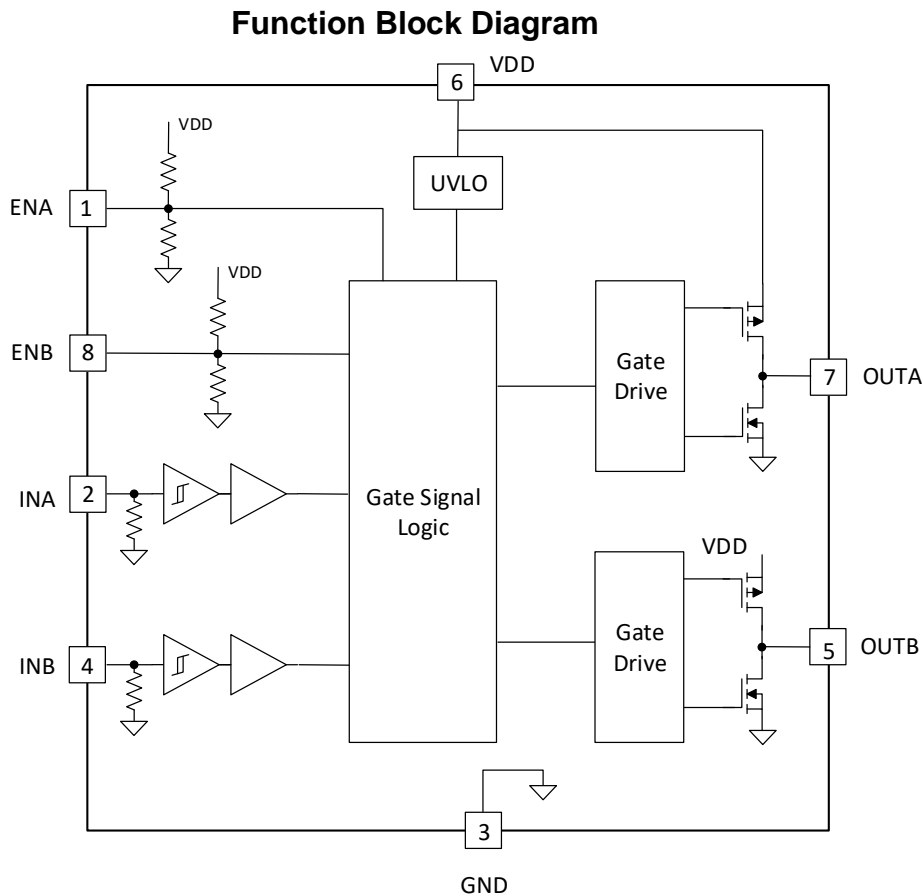
Figure 10. Rise Time and Fall time vs Temperature

7. Detail Descriptions

IVCR2401 driver provides dual-channel high-speed low-side gate drive. It features three-level enable signal inputs for tight mismatching outputs when two channels are paralleled to drive large or paralleled power switches.

7.1 Input Signal

INA and INB are non-inverting logic gate driver inputs. The pins have a weak pulldown. When left floating, outputs are pulled to GND. The input is a TTL and CMOS logic level with maximum 20V input tolerance.



7.2 ENA and ENB

ENA and ENB are three-level inputs. When grounded, their corresponding channels are disabled. When they are logic HIGH, or floating, both channels are enabled. When one of them is floating while the other is logic HIGH, its output stage will be driven by the other channel's input signal. This unique feature ensures the two channels have very tight delay mismatch.

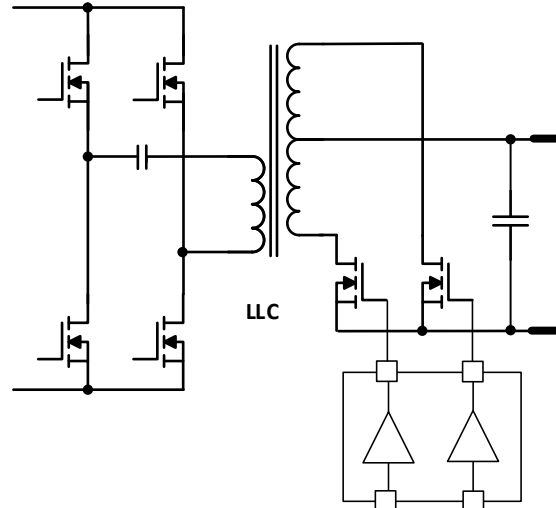
7.3 OUTA and OUTB

OUTA and OUTB are totem-pole outputs, which consist of a P-channel MOSFET for pullup and an N-channel MOSFET for pulldown. Each output stage in IVCR2401 can supply 4A peak source and 4A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation. The presence of the MOSFET body diodes also offers voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

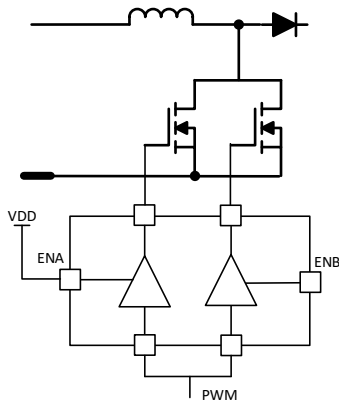
7.4 VDD and Under Voltage Protection

IVCR2401 maximum voltage rating is 25V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The driver has internal under voltage lockout (UVLO) protection feature. When VDD level is below UVLO threshold, this circuit holds the output LOW, regardless of the status of the inputs.

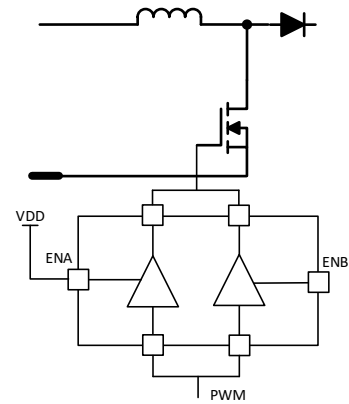
8. Application Implementation



Two channels driven separately

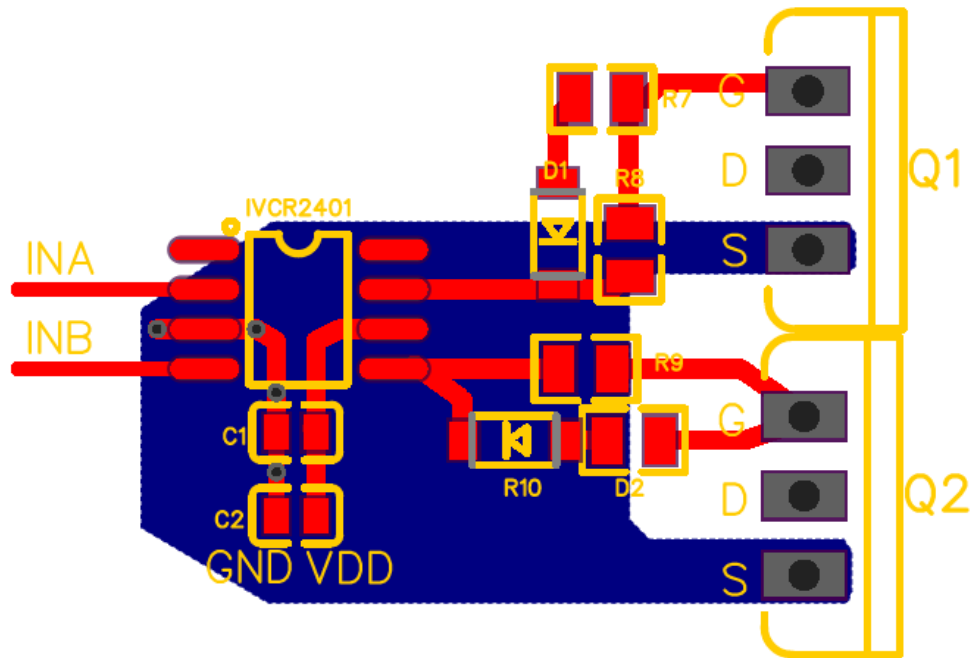


Two paralleled switches driven by two outputs with minimized mismatch



A large switch driven by two paralleled outputs with minimized mismatch

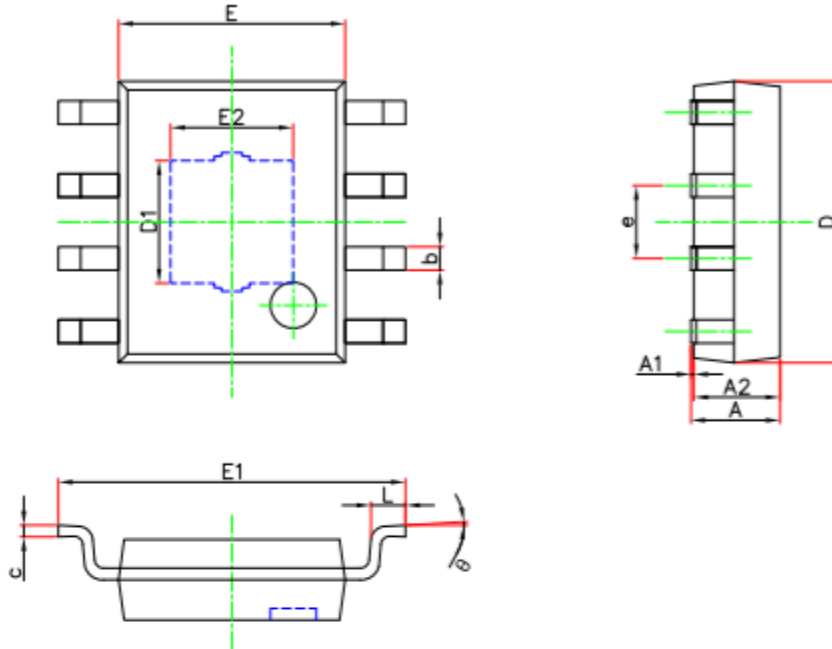
9. Layout



Layout Example for IVCR2401

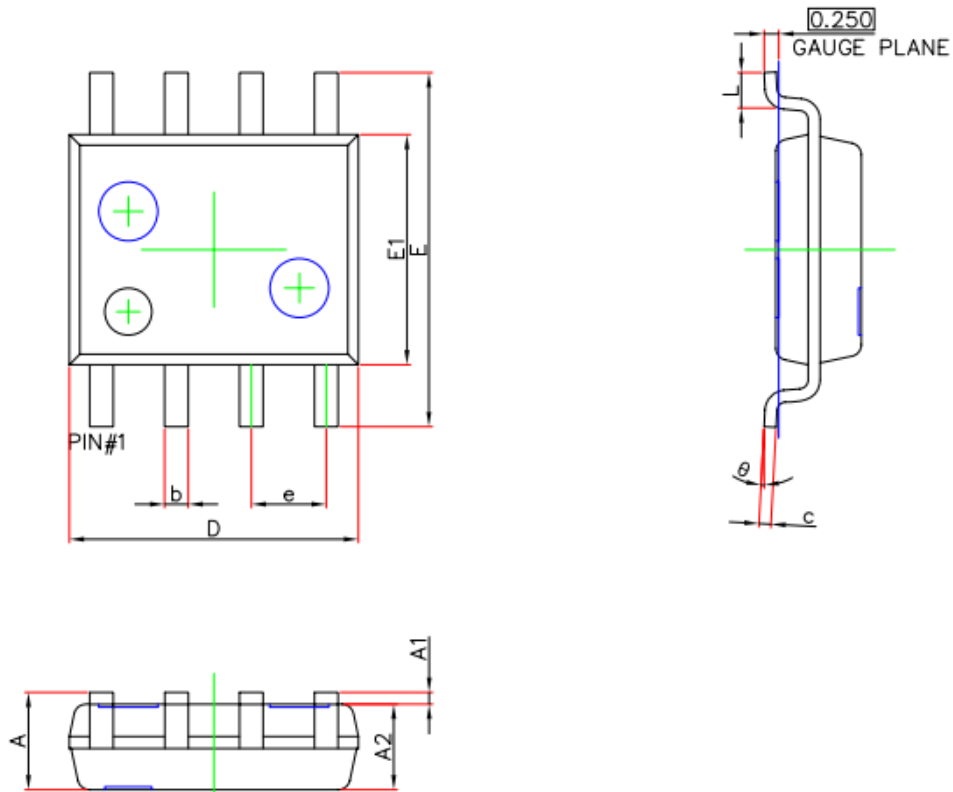
10. Package Information

SOIC-8 (EP) Package Dimensions

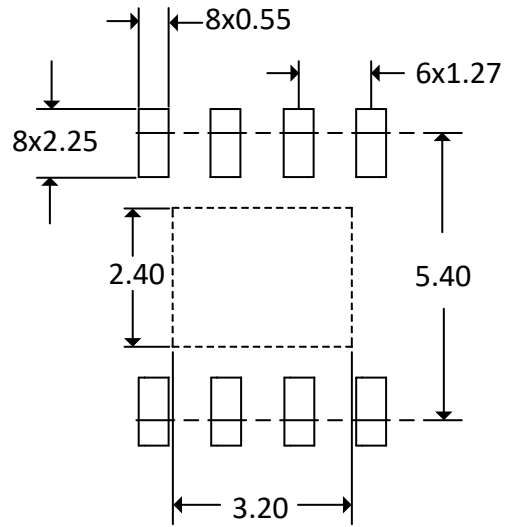


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	2.034	2.234	0.080	0.088
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.034	2.234	0.080	0.088
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

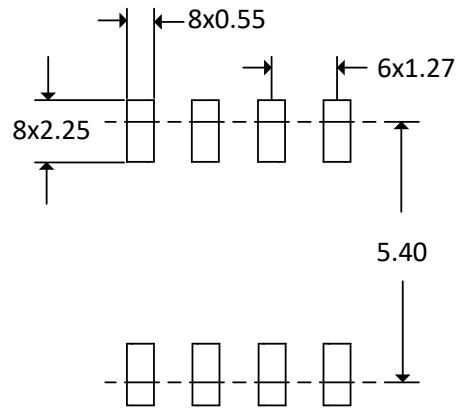
SOIC-8 Package Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



IVCR1401DP Recommended Soldering Dimensions



IVCR1401D Recommended Soldering Dimensions