Data Sheet | July 25, 2005 | FN9087.2

High Voltage Bootstrap High Side Driver

The ISL6801 is a single monolithic, inverting bootstrap driver. Its floating Level Shifter Section is optimized for the control of N-Channel Power MOSFETs in high side configurations with Bus Voltages up to 120VDC from a 5V Controller Output. It features two output stages pinned out separately to allow independent control of rise and fall times. To ensure static DC operation an integrated recharge path charges the bootstrap cap while the driver is switched off. A pull-up resistor forces the input low when no control signal is applied. The supply voltage is monitored to guarantee faultless operation at start-up.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL6801AB	-40 to 125	8 Ld SOIC	M8.15
ISL6801AB-T	-40 to 125	8 Ld SOIC Tape and Reel	M8.15

Features

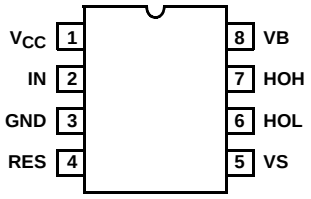
- Single Bootstrap High Side Driver
- Bootstrap Supply Max Voltage. 120VDC
- Peak Output Drive Current. 200mA
- Switching Frequency 100kHz
- Active Low Input
- Separate Reset Input
- Recharge Path for Static Operation
- Separate High and Low Gate Drive Outputs Allow Independent Turn ON/OFF Time Control
- Supply Undervoltage Protection
- Space Saving SO-8 Package
- Wide Operating Temperature Range

Applications

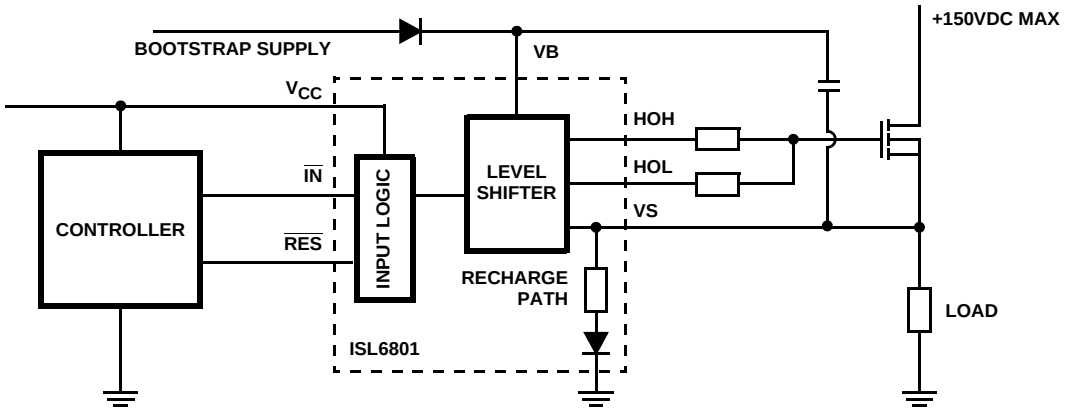
- Driver for N-Channel MOSFETs in High Side Configurations that Control Ground Referenced Loads
- Drives Solenoids, Motors, Relays and Lamps in Automotive Applications

Pinout

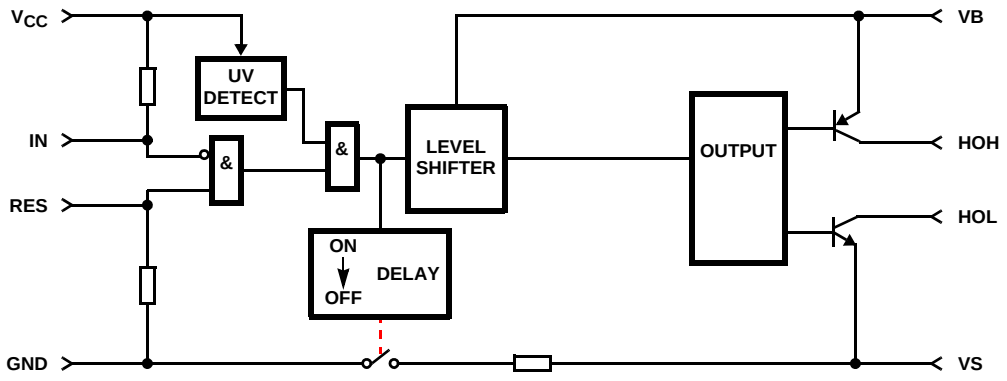
SL6801AB (SOIC)
TOP VIEW



Typical Application Block Diagram



Functional Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{CC}	Driver Supply, Typical 5.0V
2	IN	Driver Control Signal Input
3	GND	Ground
4	RES	Driver Enable Signal Input (‘RESET’)
5	VS	MOSFET Source Connection
6	HOL	MOSFET Gate Low Connection
7	HOH	MOSFET Gate High Connection
8	VB	Driver Output Stage Supply

NOTE:
The HOL and HOH are the low respective high gate drive output pins. The turn on and turn off time of the external MOSFET could be controlled by using different resistance values for high and low signal.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 16V
Driver Output Stage Voltage, V_B (Referred to GND) 130V
Source Reference Voltage, V_S
(-5V for 0.5ms, MOSFET Off) . . . . . (Min) -1.5V
. . . . . (Max) 120V
ESD Rating, V_{ESD}
Human Body Model . . . . . (Min) 820V
(Per MIL-STD-883 Method 3015.7)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
SOIC Package	90

Maximum Junction Temperature (Plastic Package) . . . . . .150^{o}C
Maximum Storage Temperature Range . . . . . -55^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . .245^{o}C
(SOIC Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^{o}C to 125^{o}C
Supply Voltage Range (Max) . . . . . 4.5V to 6.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

All values are over full temperature range.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Temperature Range	T_A		-40	-	125	^{o}C
Source Reference Voltage	VS	-1.8V Continuous, VB/V_{OH} must stay low, IN = 0V, RES = 5V, V_{CC} = 4.5V and 6.5V, VB = 5V and 12V, (Load R = 50Ω, C = 6.8nF) T_A = -40 to 125^{o}C	-1.5	-	120	V
Supply Voltage (Note 2)	V_{CC}		4.5	-	6.5	V
Driver Output Supply	$V_{VB - VS}$	Ident. to V_{GS} of MOSFET Device Functional	4.0	8.5	16.0	V
	$V_{VB - GND}$		2.0	-	-	V
Switching Frequency	f	Guaranteed by Design	100	-	-	kHz
Voltage Transconductance (Note 3)	dVs/dt		-	-	500	V/µs
Peak Gate Drive Current	I_{HOpeak}	Sink/Source Current VB = 5V and 16V, 100ns	-	200	-	mA
Continuous Gate Drive Current (Note 3)	I_{HOcont}	Sink/Source Current Continuous	6.5	8	-	mA
Gate Drive Level LOW	$V_{HOL, VS}$	IN at H, I_{HO} = 1mA, VB-VS = 5V and 16V	-	-	0.3	V
Gate Drive Level LOW	$V_{HOL, VS}$	IN at H, I_{HO} = 100mA	-	-	2.2	V
Gate Drive Level HIGH	$V_{VB, HOH}$	IN at L, I_{HO} = 1mA, VB-VS = 5V and 16V	-	-	0.5	V
Gate Drive Level HIGH	$V_{VB, HOH}$	IN at L, I_{HO} = 100mA	-	-	2.2	V
Total IN to Output Delay (Figure 1)	$td_{IN-HOH, L}$	at V_{CC} = 5.0V, RES = 5V, Output Trigger Level: 3.5V ON at VB = 5V, 1.0V OFF at VB = 16V, Input 2.5V (Load R = 50Ω, C = 6.8nF)	-	1.0	3.0	µs
Total RES to Output Delay (Figure 2)	$td_{RES - HOH, L}$	VB-VS = 5V and 16V, (Load R = 50Ω, C = 6.8nF)	-	1.0	3.0	µs
Output Rise/Fall Times	$t_{HOH, L}$ Fall/Rise	VB-VS = 5V (Load R = 50Ω, C = 6.8nF)	-	100	500	ns
		VB-VS = 16V	-	200	500	ns
VB Drop Voltage (Figure 4, Note 4)	VB_{DROP}	VB-VS = 9.0V, C_{100} = 1µF, (Load R = 50Ω, C = 6.8nF)	-	100	210 (Note 5)	mV

Electrical Specifications All values are over full temperature range. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VB Input Current (Note 6)	I_{VB}	Static Current, VB-VS = 8.5V, V_{CC} = 5V, IN = 0V, RES = 5V, (Load R = 50Ω, C = 6.8nF)	300	750	875	µA
VB Input Current	I_{VB}	Static Current, VB-VS = 8.5V, V_{CC} = 5V, IN = 0V, RES = 0V, (Load R = 50Ω, C = 6.8nF)	100	550	700	µA
Driver Supply Current	I_{VCC}	at V_{CC} = 4.5V and 6.5V (Load R = 50Ω, C = 6.8nF)	-	1.2	2.5	mA
Input Threshold LOW (Note 7)	IN_{LOW}	V_{CC} = 4.5V and 6.5V	1.4	-	-	V
Input Threshold HIGH (Note 7)	IN_{HIGH}	V_{CC} = 4.5V and 6.5V	-	-	3.0	V
Enable Threshold LOW (Note 7)	RES_{LOW}	V_{CC} = 4.5V and 6.5V	1.4	-	-	V
Enable Threshold HIGH (Note 7)	RES_{HIGH}	V_{CC} = 4.5V and 6.5V	-	-	3.0	V
Input Impedance at IN	R_{IN}	at V_{CC} = 5.0V, RES = 5V, IN = 0V, VB = 12V	60	100	170	kΩ
Input Impedance at RES	R_{RES}	at V_{CC} = 5.0V, RES = 5V, IN = 0V, VB = 12V	60	100	170	kΩ
Logic Input Current at RES (Note 8)	I_{RES}	at Logic LOW Response HIGH	-0.1	-	1.0	mA
Undervoltage Shutdown Threshold	V_{UV}	V_{CC} to GND, Incl. Hyst.	-	3.5	-	V
Recharge Resistance (Note 9)	$R_{recharge}$	VB = VS = HOH = HOL = 7V, RES = 5V, IN = 5V, V_{CC} = 4.5V and 6V	70	170	350	Ω
Recharge Turn On Delay (Note 9)	$t_{RechargeON}$		7	10	15	µs
Recharge Turn Off Delay	$t_{RechargeOFF}$		-	-	1.5	µs
Recharge Path Voltage Drop	Vdrop Recharge	at a Constant Current of 1.0mA	-	-	0.8	V
		at a Constant Current of 10mA	-	-	3.5	V

NOTES:

2. Shutdown between 3.5V and 4.5V.
3. Parametric limits are guaranteed by design, but not tested in production.
4. The drop voltage is caused by VB to VS current flow during switching. See Figure 3.
5. Assuming 3µs switching overlap, time delay use at testing 100µs.
6. External MOSFET ON or OFF.
7. Input and Enable thresholds tested at V_{CC} = 4.5V and 6.5V, VB = 12V, VS = 0V, IN at 0V, Response RES at 5.0V.
8. The defined values are to be considered as a maximum allowed value. The input stage does not need to have sink or source capability.
9. The recharge path has to withstand transients in the 120V range for approximately 1µs while injector turn off, causing high power dissipation in the resistor.

Timing Diagrams

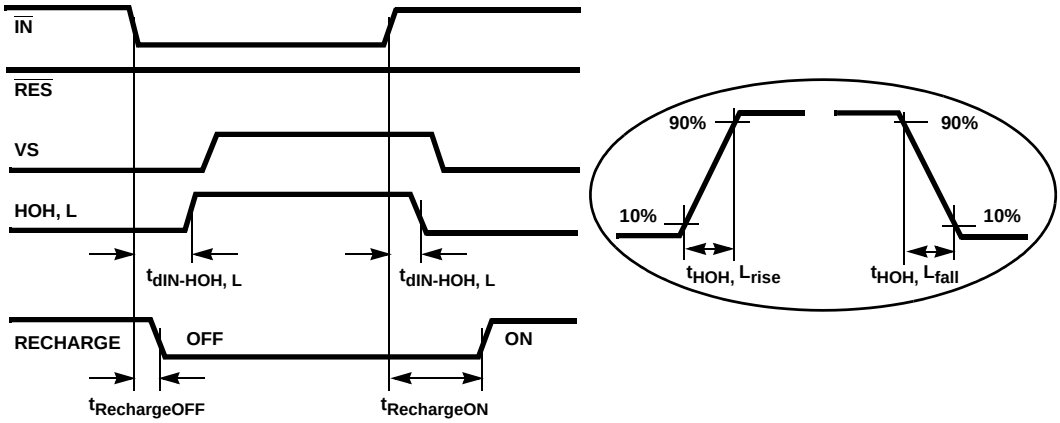


FIGURE 1. INPUT/OUTPUT TIMING DIAGRAM

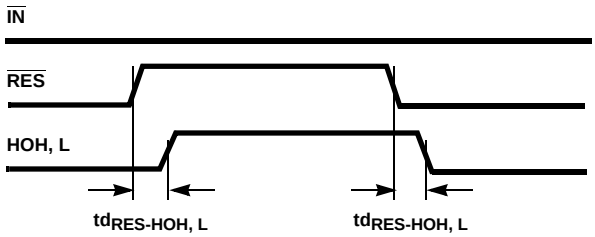


FIGURE 2. RESET TIMING DIAGRAM

VB Drop Voltage Test

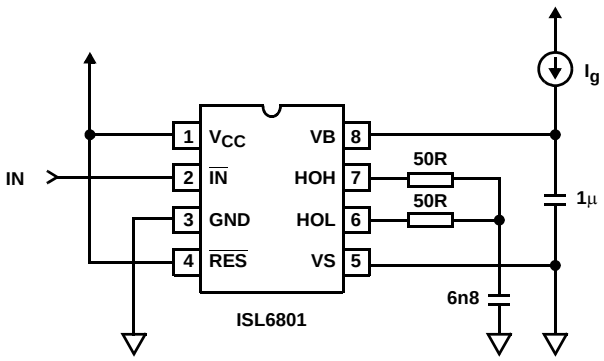


FIGURE 3. VB DROP VOLTAGE TEST CIRCUIT

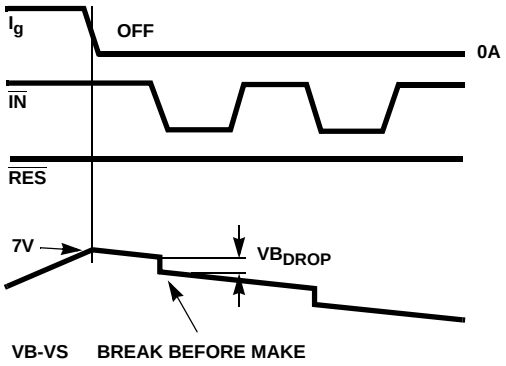
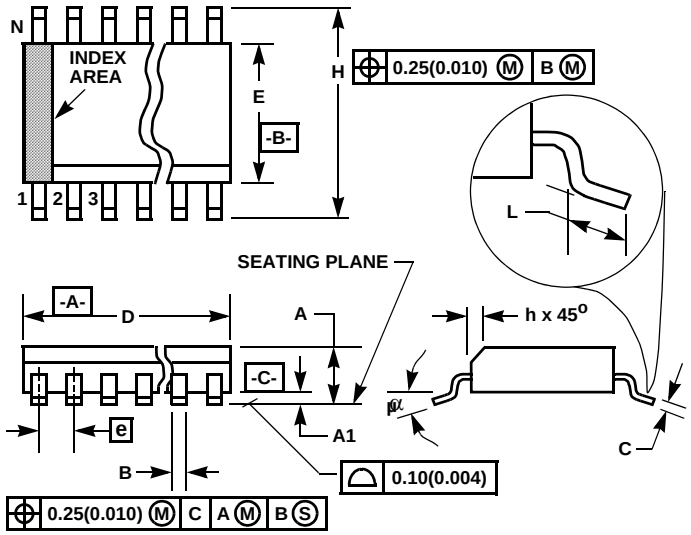


FIGURE 4. VB DROP VOLTAGE DIAGRAM

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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