# High-Frequency, High Side and Low Side Gate Driver

# NCV51511


**SOIC8−EP**
**CASE 751AC**

The NCV51511 is high side and low side gate−drive IC designed for high−voltage, high−speed, driving MOSFETs operating up to 80 V.

The NCV51511 integrates a driver IC and a bootstrap diode. The driver IC features low delay time and matched PWM input propagation delays, which further enhance the performance of the part.

The high speed dual gate drivers are designed to drive both the high−side and low−side of N−Channel MOSFETs in a half bridge or synchronous buck configuration. The floating high−side driver is capable of operating with supply voltages of up to 80 V. In the dual gate driver, the high side and low side each have independent inputs to allow maximum flexibility of input control signals in the application. The PWM input signal (high level) can be 3.3 V, 5 V or up to $V_{DD}$ logic input to cover all possible applications. The bootstrap diode for the high−side driver bias supply is integrated in the chip. The high−side driver is referenced to the switch node (HS) which is typically the source pin of the high−side MOSFET and drain pin of the low−side MOSFET. The low−side driver is referenced to $V_{SS}$ which is typically ground. The functions contained are the input stages, UVLO protection, level shift, bootstrap diode, and output driver stages.

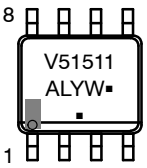
### Features

- Drives two N−Channel MOSFETs in High & Low Side
- Integrated Bootstrap Diode for High Side Gate Drive
- Bootstrap Supply Voltage Range up to 100 V
- 3 A Source, 6 A Sink Output Current Capability
- Drives 1nF Load with Typical Rise/Fall Times of 6 ns/4 ns
- TTL Compatible Input Thresholds
- Wide Supply Voltage Range 8 V to 16 V (Absolute Maximum 18 V)
- Fast Propagation Delay Times (Typ. 30 ns)
- 2 ns Delay Matching (Typical)
- Under−Voltage Lockout (UVLO) Protection for Drive Voltage
- Industry−Standard Pinouts, SOIC 8 with Exposed PAD
- Automotive Qualified to AEC−Q100:
  - Operating temperature range from −40°C to 150°C
  - Reliability at 150°C for 2,016 hrs
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- 48 V Converters for HEV/EV
- Half−Bridge and Full−Bridge Converters
- Synchronous−Buck Converters

### MARKING DIAGRAM




| | |
|---|---|
| V51511 | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Device |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

## TYPICAL APPLICATIONS

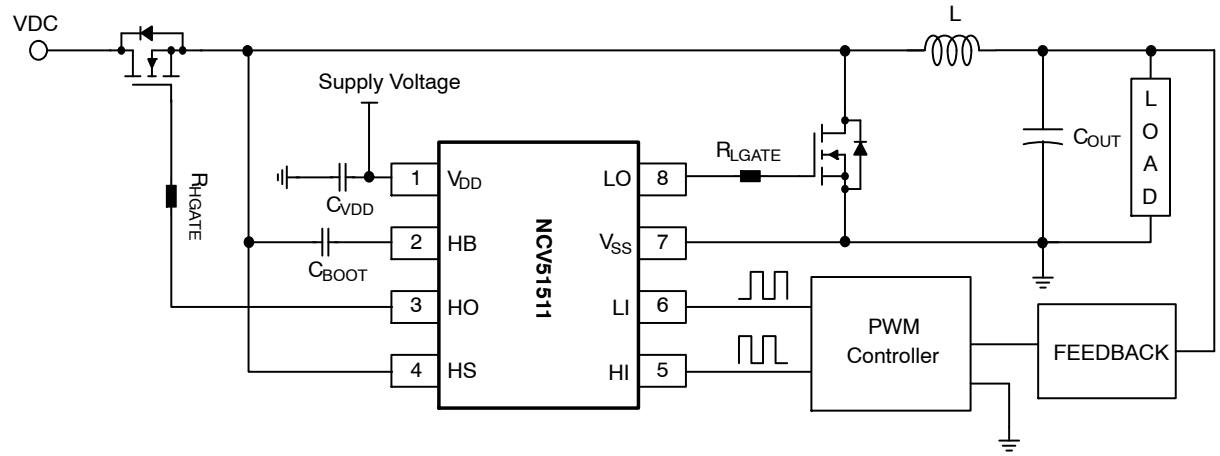



**Figure 1. Application Schematic – Synchronous Buck Converter**

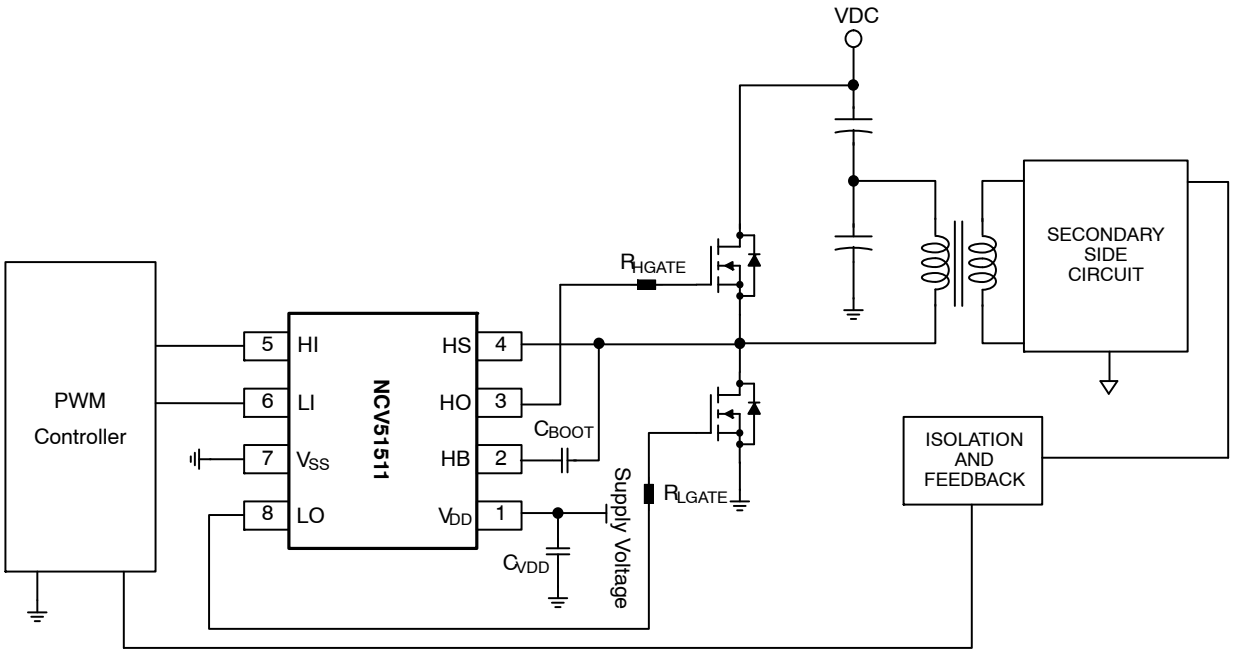



**Figure 2. Application Schematic – Half Bridge Converter**

## BLOCK DIAGRAM

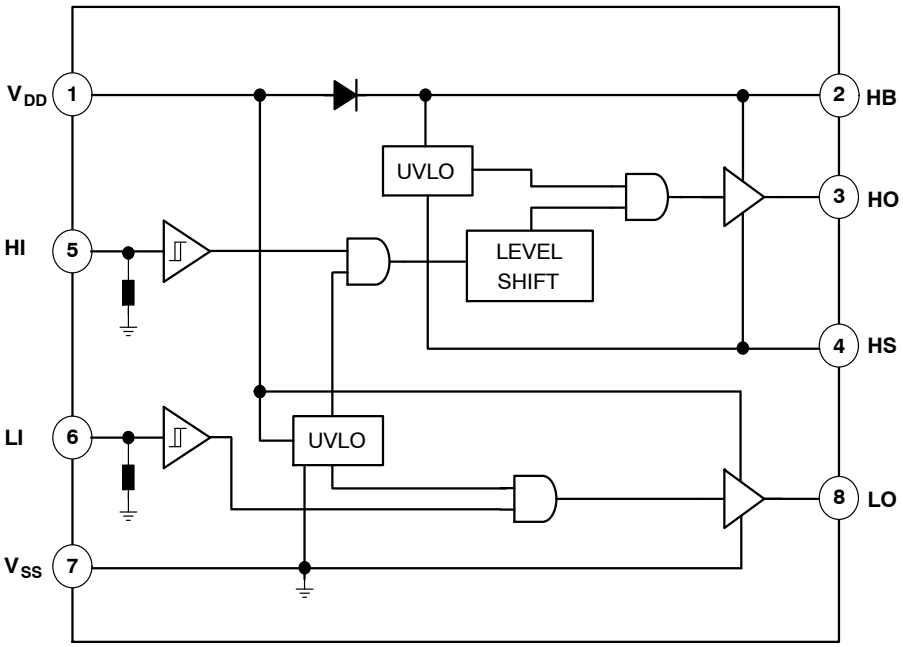



**Figure 3. Simplified Block Diagram**

## PIN CONNECTIONS

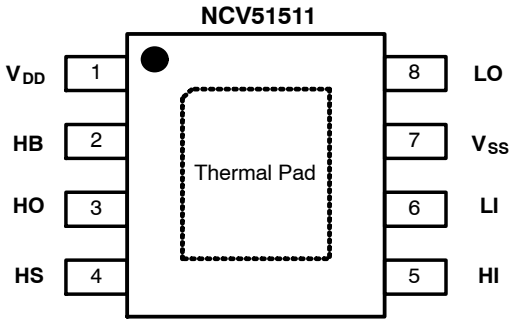



**Figure 4. Pin Assignments – SOIC8–EP** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $V_{DD}$ | Logic and low–side gate driver power supply voltage |
| 2 | HB | High–side floating supply |
| 3 | HO | High–side driver output |
| 4 | HS | High–voltage floating supply return |
| 5 | HI | Logic input for High–side gate driver output |
| 6 | LI | Logic input for Low–side gate driver output |
| 7 | $V_{SS}$ | Logic Ground |
| 8 | LO | Low–side driver output |
| – | Exposed PAD | Can either be left open or connected to $V_{SS}$. We recommend EPAD to be connected to $V_{SS}$ plane for improved thermal performance. |

**Table 2. MAXIMUM RATINGS**

All voltage parameters are referenced to $V_{SS}$, unless otherwise noted.

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{DD}$ | Low−Side and Logic Fixed Supply Voltage | −0.3 | 18 | V |
| $V_{HS}$ | High−Side Floating Supply Offset Voltage(Note 1) | −1 | 100 | V |
| | Repetitive Pulse (< 100 ns)(Note 2) | −(24 − $V_{DD}$) | 100 | V |
| $V_{LO}$ | Low−Side Output Voltage, LO Pin | −0.3 | $V_{DD}$ + 0.3 | V |
| | Repetitive Pulse (< 100 ns)(Note 2) | −2 | $V_{DD}$ + 0.3 | V |
| $V_{HO}$ | High−Side Floating Output Voltage, HO Pin | $V_{HS}$ − 0.3 | $V_{HB}$ + 0.3 | V |
| | Repetitive Pulse (< 100 ns)(Note 2) | $V_{HS}$ − 2 | $V_{HB}$ + 0.3 | V |
| $V_{LI}$, $V_{HI}$ | Logic Input Voltage | −0.3 | $V_{DD}$ + 0.3 | V |
| $V_{HB}$ | High−Side Floating Supply Voltage | −0.3 | 100 | V |
| $V_{HB}$ − $V_{HS}$ | $V_{HS}$ to $V_{HB}$ Supply Voltage | −0.3 | 18 | V |
| $P_D$ | Power Dissipation (Note 3) | | 2.5 | W |
| $T_J$, | Operating Junction Temperature | −55 | 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The $V_{HS}$ negative voltage capability can be calculated using ($V_{HB}$ −$V_{HS}$)−18 V base on $V_{HB}$, due to its dependence on $V_{DD}$ voltage level.
2. Verified at bench characterization.
3. JEDEC standard: JESD51−2, JESD51−3. Mounted on 76.2 x 114.3 x1.6 mm PCB (FR−4 glass epoxy material).

**Table 3. ESD AND MSL**

| Symbol | Parameters | | Value | Unit.s |
|---|---|---|---|---|
| $ESD_{HBM}$ | Electrostatic Discharge Capability | Human Body Model,per AEC Q100−002 | 2000 | V |
| $ESD_{CDM}$ | | Charged Device Model, AEC Q100−011 | 1000 | |
| MSL | Moisture Sensitivity Level | | 2 | Level |

**Table 4. THERMAL INFORMATION** (Note 4)

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance Junction−Air (Note 4) | 39 | °C/W |
| $\psi_{JL}$ | Thermal characterization parameter Junction−Lead | 15 | °C/W |
| $\psi_{JT}$ | Thermal characterization parameter Junction−Case (TOP) | 6 | °C/W |

4. As mounted on a 76.2 x 114.3 x 1.6 mm FR4 substrate with a Multi−layer of 1 oz copper traces and heat spreading area. As specified for a JEDEC 51−7 conductivity test PCB. Test conditions were under natural convection or zero air flow

**Table 5. RECOMMENDED OPERATING RANGES**

All voltage parameters are referenced to $V_{SS}$

| Symbol | Parameters | Test Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | DC | 8 | 16 | V |
| $V_{HS}$ | High Side Floating Return | DC | −1 | 80 | V |
| | | Repetitive Pulse (< 100 ns) | −(24 − $V_{DD}$) | 100 | V |
| $V_{HB}$ | Voltage on HB | DC | $V_{HS}$ + 8 | $V_{HS}$ + 16 | V |
| $dV_{SW}/dt$ | Voltage Slew Rate on SW | | | 50 | V/ns |
| $T_J$ | Operating Temperature | | −40 | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 6. ELECTRICAL CHARACTERISTICS**

$V_{DD}$ = $V_{HB}$ = 12 V, $V_{HS}$ = $V_{SS}$ = 0 V, $T_A$ = $T_J$ = −40°C to 150°C, no load on HO or LO, unless otherwise noted.

| Symbol | Parameters | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Power Supply Section** | | | | | | |
| $I_{DD}$ | $V_{DD}$ Quiescent Current | $V_{HI}$ = 0 V; $V_{LI}$ = 0 V | | 0.17 | 0.3 | mA |
| $I_{DDO}$ | $V_{DD}$ Operating Current | $f_{SW}$ = 500 kHz | | 1.5 | 3.0 | mA |
| $I_{HB}$ | HB Quiescent Current | $V_{HI}$ = 0 V; $V_{LI}$ = 0 V | | 0.1 | 0.2 | mA |
| $I_{HBO}$ | HB Operating Current | $f_{SW}$ = 500 kHz | | 1.9 | 3.0 | mA |
| $I_{HBS}$ | HB to $V_{SS}$ Quiescent Current | $V_{HS}$ = $V_{HB}$ = 80 V | | 0 | 10 | μA |
| $I_{HBSO}$ | HB to $V_{SS}$ Operating Current | $f_{SW}$ = 500 kHz | | 0.3 | 1.0 | mA |
| $V_{DDR}$ | $V_{DD}$ UVLO Threshold | $V_{DD}$ Rising | 6.2 | 6.8 | 7.4 | V |
| $V_{DDH}$ | $V_{DD}$ UVLO Hysteresis | | | 0.6 | | V |
| $V_{HBR}$ | HB UVLO Threshold | HB Rising | 5.5 | 6.3 | 7.2 | V |
| $V_{HBH}$ | HB UVLO Hysteresis | | | 0.4 | | V |
| **Input Logic Section** | | | | | | |
| $V_{IH}$ | High Level Input Voltage Threshold | | 1.80 | 2.2 | 2.50 | V |
| $V_{IL}$ | Low Level Input Voltage Threshold | | 1.3 | 1.7 | 2.0 | V |
| $V_{IHYS}$ | Input Logic Voltage Hysteresis | | | 0.5 | | V |
| $R_{IN}$ | Input Pull−down Resistance | | | 100 | | kΩ |
| **Bootstrap Diode** | | | | | | |
| $V_{FL}$ | Forward Voltage @ Low Current | $I_{VDD-HB}$ = 100 μA | | 0.55 | 0.8 | V |
| $V_{FH}$ | Forward Voltage @ High Current | $I_{VDD-HB}$ = 100 mA | | 0.8 | 1.0 | V |
| $R_D$ | Dynamic Resistance | $I_{VDD-HB}$ = 100 mA | | 0.7 | 1.5 | Ω |
| $t_{BS}$ (Note 5) | Diode Turn−off Time | $I_F$ = 20 mA, $I_{REV}$ = 0.5 A | | 20 | | ns |
| **Low Side Driver** | | | | | | |
| $V_{OLL}$ | Low Level Output Voltage | $I_{LO}$ = 100 mA | | 0.06 | 0.15 | V |
| $V_{OHL}$ | High Level Output Voltage | $I_{LO}$ = −100 mA, $V_{OHL}$ = $V_{DD}$ − $V_{LO}$ | | 0.16 | 0.28 | V |
| $I_{OHL}$ (Note 5) | Peak Pull−up Current | $V_{LO}$ = 0 V | | 3 | | A |
| $I_{OLL}$ (Note 5) | Peak Pull−down Current | $V_{LO}$ = 12 V | | 6 | | A |
| $t_{R\_LO}$ | LO Rise Time | 10% to 90%, $C_{LOAD}$ = 1 nF | | 6 | | ns |
| $t_{F\_LO}$ | LO Fall Time | 90% to 10%, $C_{LOAD}$ = 1 nF | | 4 | | ns |
| $t_{R\_LO1}$ | LO Rise Time | 3 V to 9 V, $C_{LOAD}$ = 100 nF | | 300 | 500 | ns |
| $t_{F\_LO1}$ | LO Fall Time | 9 V to 3 V, $C_{LOAD}$ = 100 nF | | 140 | 300 | ns |
| $t_{LPHL}$ | LI = Low Propagation Delay | $V_{LI}$ Falling to $V_{LO}$ Falling, $C_{LOAD}$ = 0 | | 28 | 45 | ns |
| $t_{LPLH}$ | LI = High Propagation Delay | $V_{LI}$ Rising to $V_{LO}$ Rising, $C_{LOAD}$ = 0 | | 30 | 47 | ns |
| **High Side Driver** | | | | | | |
| $V_{OLH}$ | Low Level Output Voltage | $I_{HO}$ = 100 mA | | 0.06 | 0.15 | V |
| $V_{OHH}$ | High Level Output Voltage | $I_{HO}$ = −100 mA, $V_{OHH}$ = $V_{HB}$ − $V_{HO}$ | | 0.16 | 0.28 | V |
| $I_{OHH}$ (Note 5) | Peak Pull−up Current | $V_{HO}$ = 0 V | | 3 | | A |
| $I_{OLH}$ (Note 5) | Peak Pull−down Current | $V_{HO}$ = 12 V | | 6 | | A |
| $t_{R\_HO}$ | HO Rise Time | 10% to 90%, $C_{LOAD}$ = 1 nF | | 6 | | ns |
| $t_{F\_HO}$ | HO Fall Time | 90% to 10%, $C_{LOAD}$ = 1 nF | | 4 | | ns |
| $t_{R\_HO1}$ | HO Rise Time | 3 V to 9 V, $C_{LOAD}$ = 100 nF | | 300 | 500 | ns |
| $t_{F\_HO1}$ | HO Fall Time | 9 V to 3 V, $C_{LOAD}$ = 100 nF | | 140 | 300 | ns |
| $t_{HPHL}$ | HI = Low Propagation Delay | $V_{HI}$ Falling to $V_{HO}$ Falling, $C_{LOAD}$ = 0 | | 28 | 45 | ns |
| $t_{HPLH}$ | HI = High Propagation Delay | $V_{HI}$ Rising to $V_{HO}$ Rising, $C_{LOAD}$ = 0 | | 30 | 47 | ns |

**Table 6. ELECTRICAL CHARACTERISTICS**

$V_{DD}$ = $V_{HB}$ = 12 V, $V_{HS}$ = $V_{SS}$ = 0 V, $T_A$ = $T_J$ = −40°C to 150°C, no load on HO or LO, unless otherwise noted.

| Symbol | Parameters | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Delay Matching** | | | | | | |
| $t_{MON}$ | HO Turn−OFF to LO Turn−ON | | | 2 | 10 | ns |
| $t_{MOFF}$ | LO Turn−OFF to HO Turn−ON | | | 2 | 10 | ns |
| **Minimum Pulse Width** | | | | | | |
| $t_{PW}$ | Minimum Pulse Width for HI and LI (Note 5) | | | | 50 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These parameters are guaranteed by design.

## TYPICAL CHARACTERISTICS

Typical characteristics are provided at 25°C and $V_{DD}$, $V_{HB}$ = 12 V unless otherwise noted.

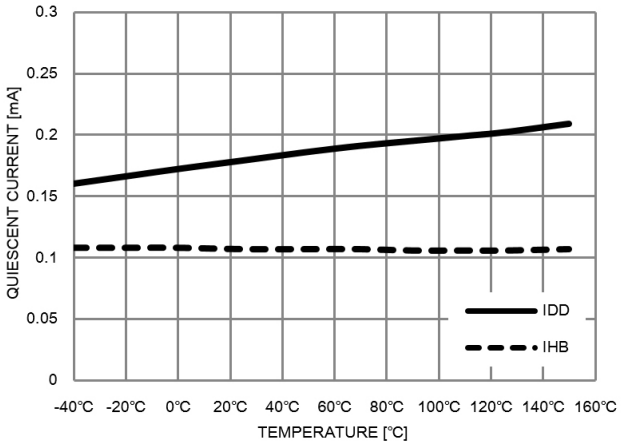



**Figure 5. Quiescent Current vs. Temperature**

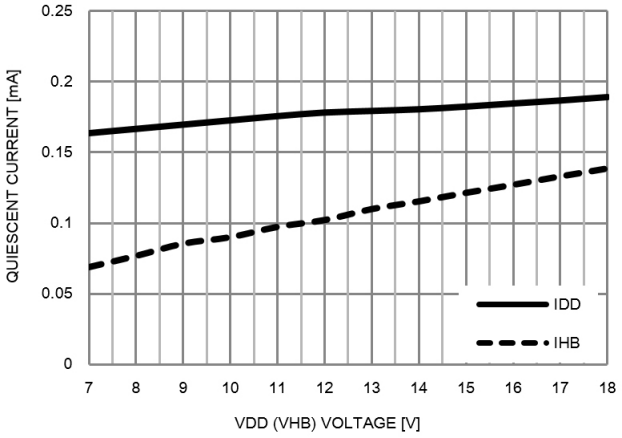



**Figure 6. Quiescent Current vs. $V_{DD}$ ($V_{HB}$)**

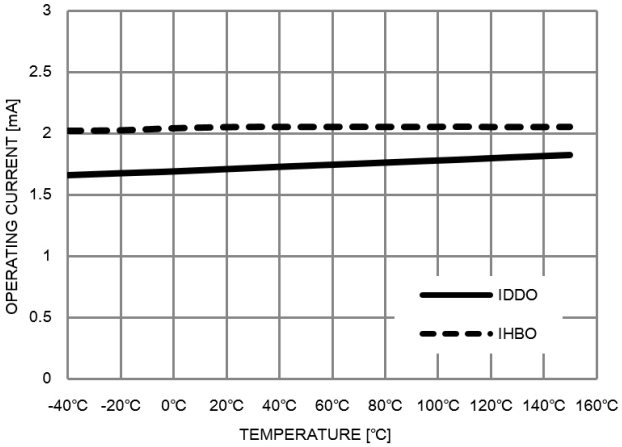



**Figure 7. Operating Current vs. Temperature**

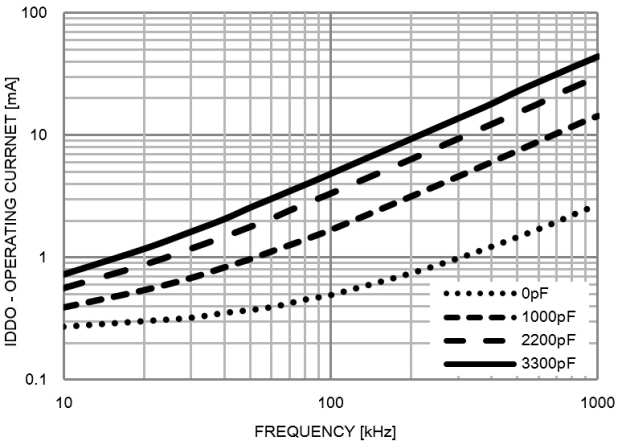



**Figure 8. $I_{DD}$ Operating Current vs. Frequency**

## TYPICAL CHARACTERISTICS

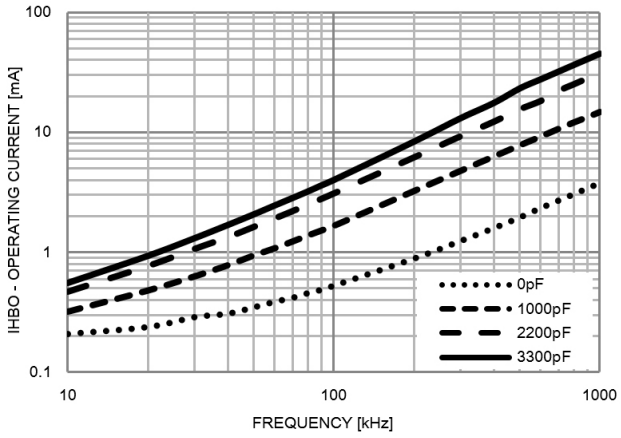



Figure 9. $I_{HB}$ Operating Current vs. Frequency

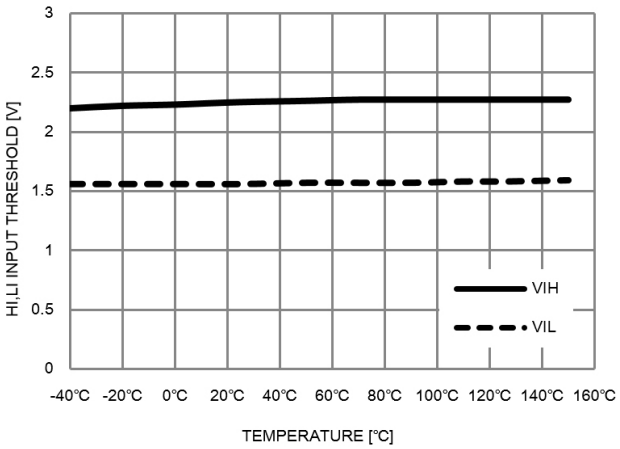



Figure 10. Input Threshold vs. Temperature

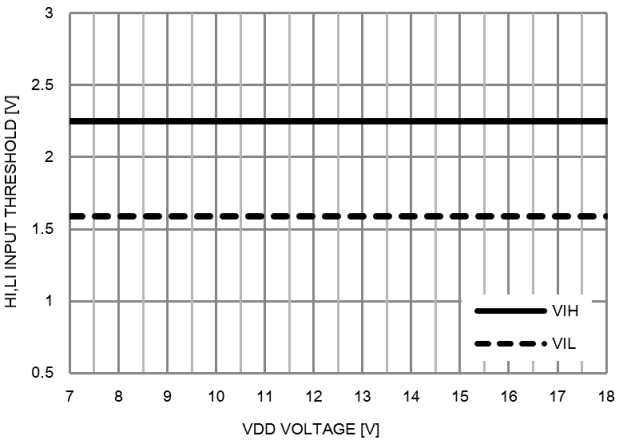



Figure 11. Input Threshold vs. $V_{DD}$

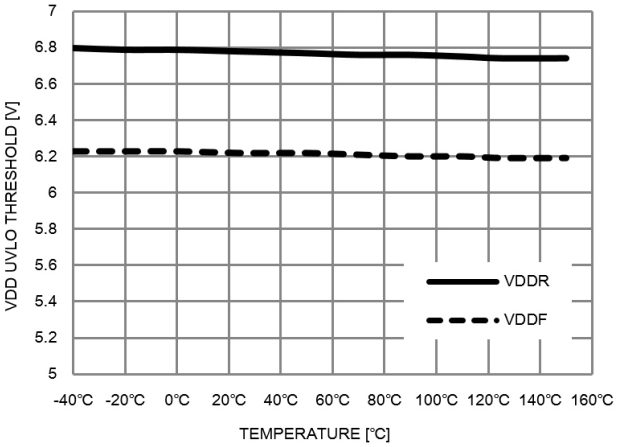



Figure 12. $V_{DD}$ UVLO Threshold vs. Temperature

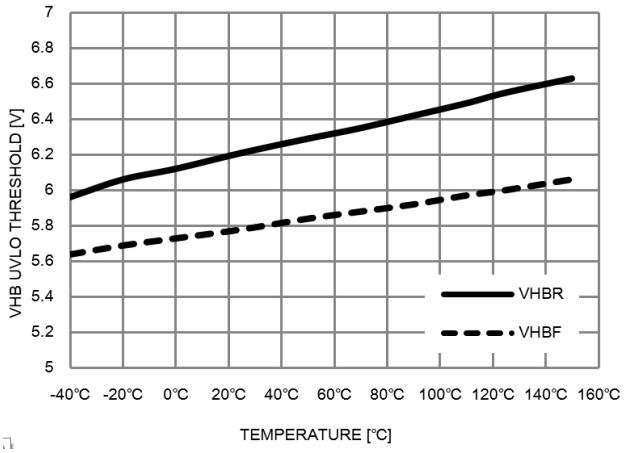



Figure 13. $V_{HB}$ UVLO Threshold vs. Temperature

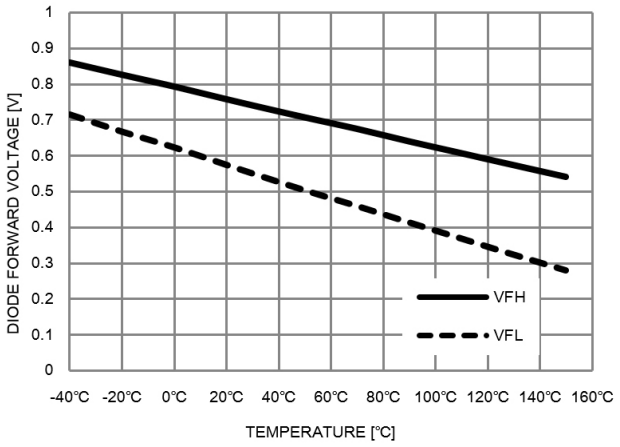



Figure 14. Bootstrap Diode $V_F$ vs. Temperature

## TYPICAL CHARACTERISTICS

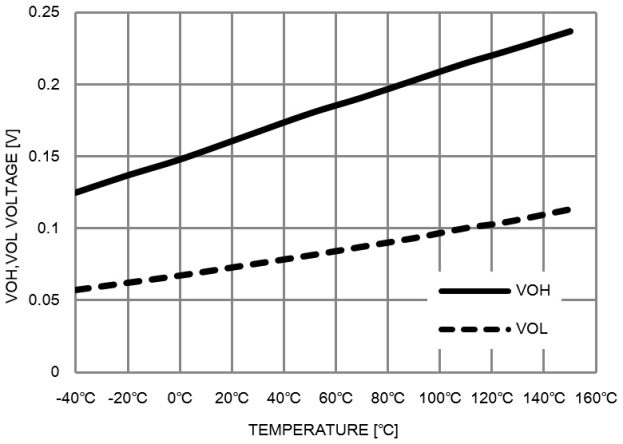



**Figure 15. $V_{OH}$, $V_{OL}$ Voltage vs. Temperature**

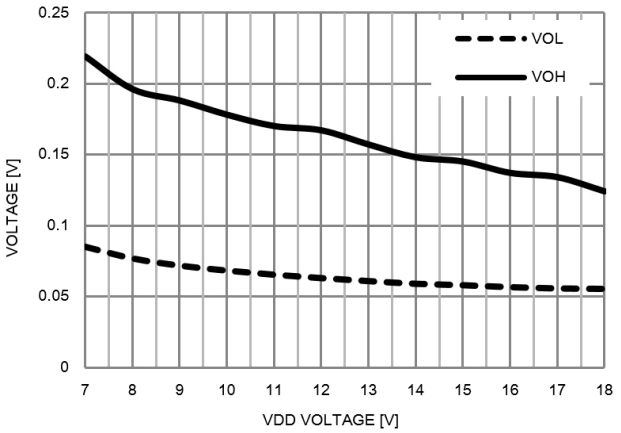



**Figure 16. $V_{OH}$, $V_{OL}$ Voltage vs. $V_{DD}$ ($V_{HB}$)**

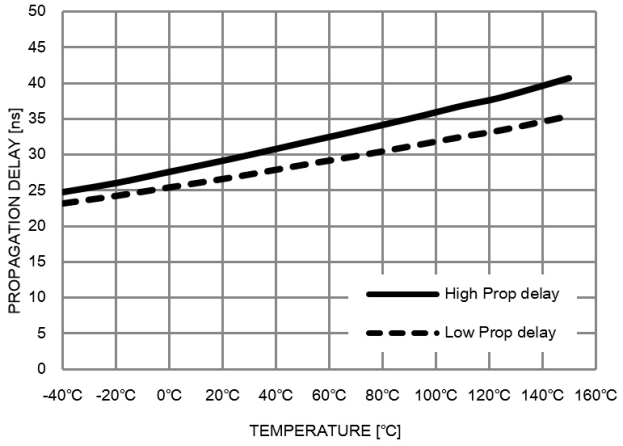



**Figure 17. Low Side Propagation Delay vs. Temperature**

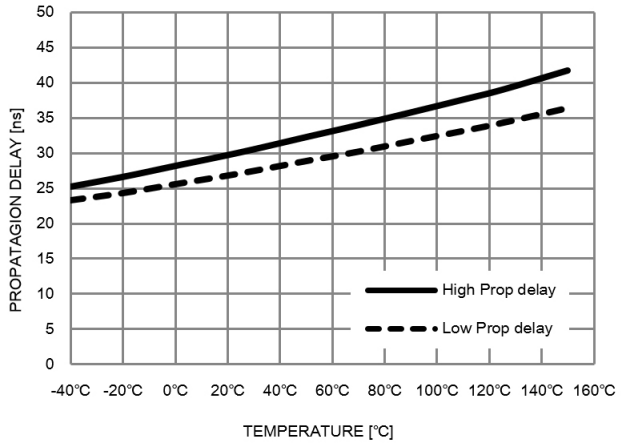



**Figure 18. High Side Propagation Delay vs. Temperature**

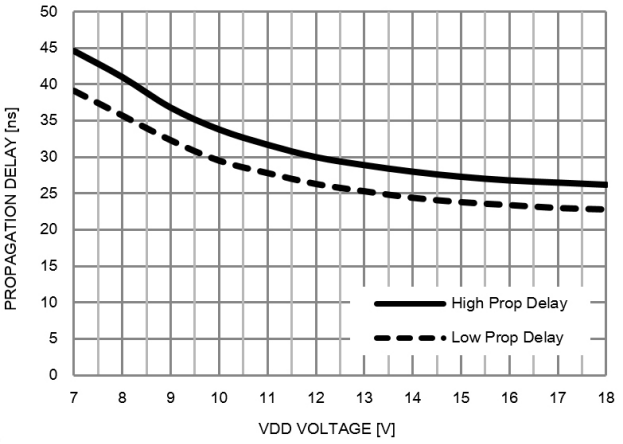



**Figure 19. Low Side Propagation Delay vs. $V_{DD}$**

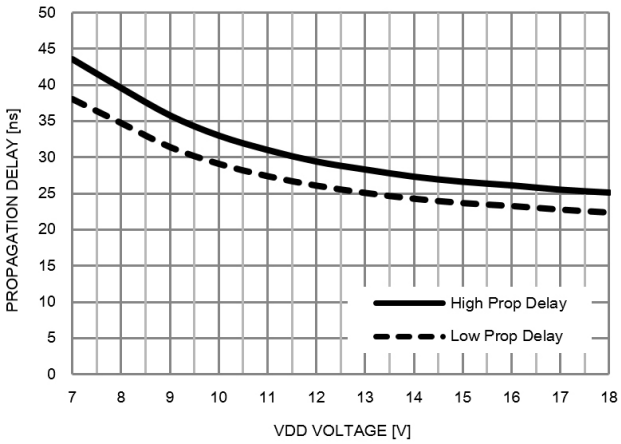



**Figure 20. High Side Propagation Delay vs. $V_{HB}$**

## TYPICAL CHARACTERISTICS

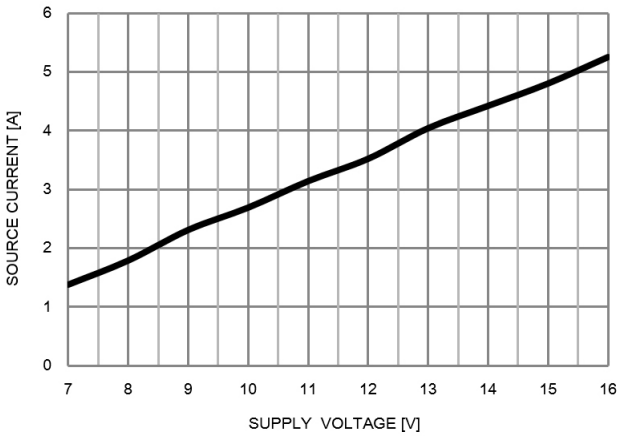



**Figure 21. HO, LO Peak Source Current vs. Supply Voltage**

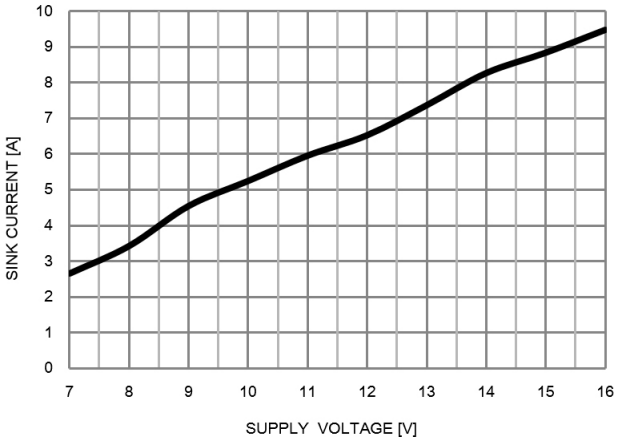



**Figure 22. HO, LO Peak Sink Current vs. Supply Voltage**

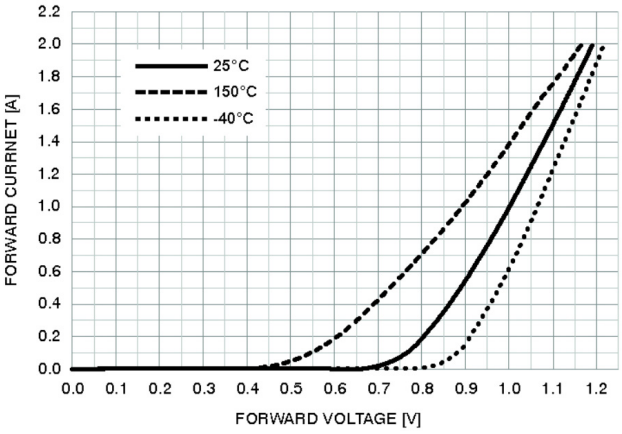



**Figure 23. Bootstrap Diode Forward Voltage vs. Temperature**

### Switching Time Definitions

Figure 24 shows the switching time waveforms definitions of the turn on and off propagation delay times.

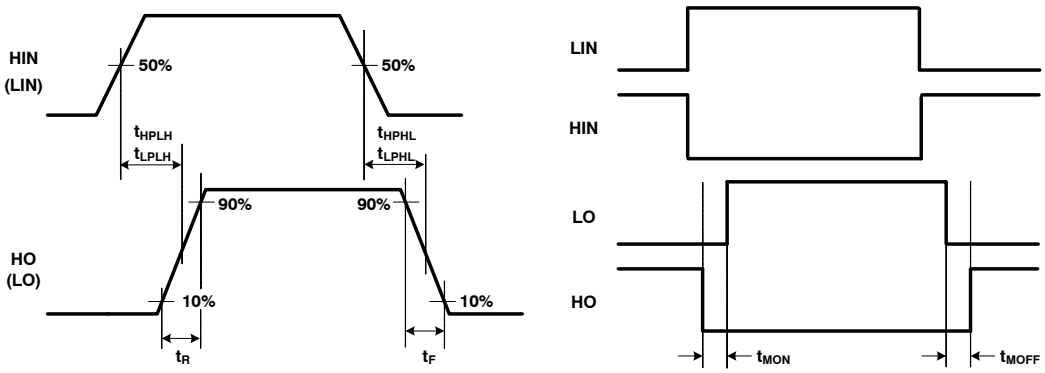



**Figure 24. Timing Diagrams**

### Input to Output Definitions

Figure 25 shows an input to output timing diagram for overall operation.

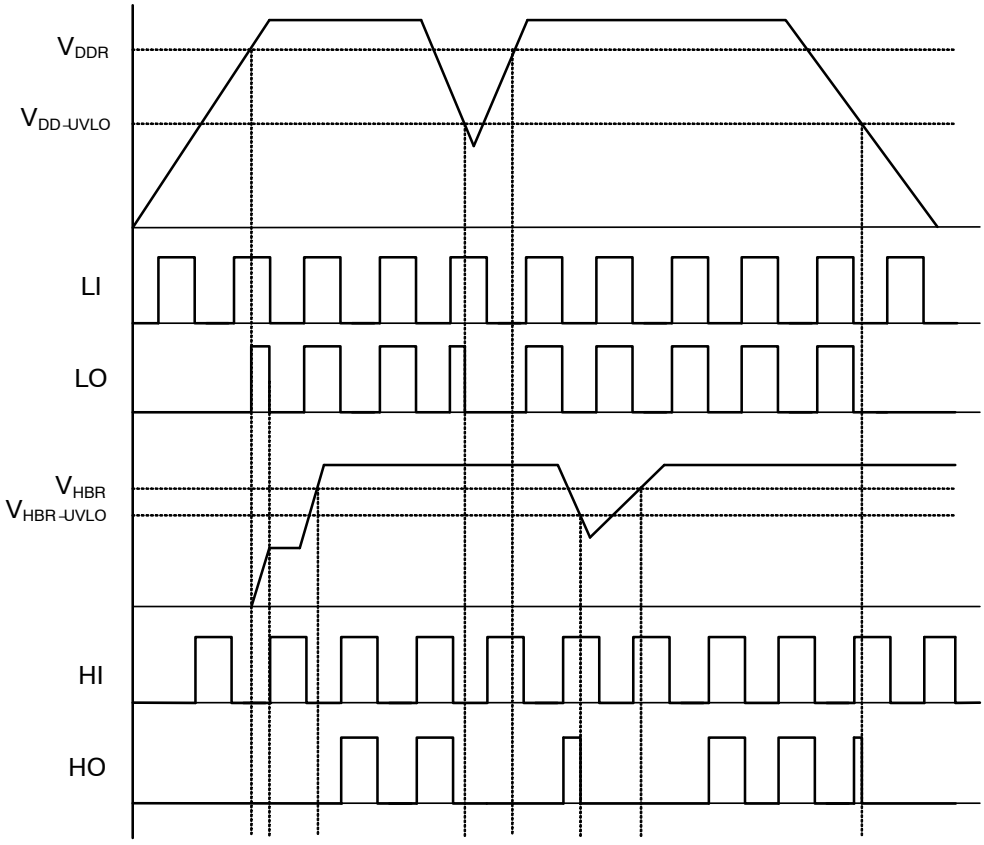



**Figure 25. Overall Operation Timing Diagram**

## APPLICATIONS INFORMATION

The NCV51511 is a gate driver to drive both the high side and the low side N−channel power MOSFETs in a half bridge or synchronous buck converters and have the capabilities to operate with maximum HS voltage up to 80 V. This device has an integrated bootstrap diode with 100 V rating to charge the bootstrap capacitor for high side driver bias. High side and low side outputs are independently controlled by each of input control signals of TTL and CMOS logic which it can simply interface with analog or digital controller. Output stages have driving capabilities of 3 A peak source current and 6 A peak sink current to drive easily high power MOSFETs. The NCV51511 provides Under−Voltage Lockout (UVLO) protection which the power supply is to ensure both the high side and the low side driver to bias correctly.

### Input Stage

NCV51511 driver has two input pins HI, LI which are compatible with TTL and CMOS logic level. The amplitude for PWM input signal can be driven from 3.3 V to VDD level to be interfaced simply with analog and digital controllers. The input pins in this device are designed with Schmitt triggers to prohibit logic error by unexpected noises sources. In addition, there are pull down resistors in all input pins to ensure that the output stays low when input pin is floating. Input logic threshold voltage for high and low state is 2.2 V and 1.7 V respectively.

### Level Shift

The level shifter used in this device is the bridge circuit to deliver the PWM signal from the high side input to the high side output stage which is referenced to the switch node (HS). Therefore, HO output can be controlled through the level shifter and input signal. NCV51511 had been designed to minimize the propagation delay time generated by level shifter itself, hence this device provides excellent delay matching characteristic less than10 ns between high and low side driver. The extreme low delay matching time allows the systems to be designed with high frequency and high efficiency.

### Bootstrap Diode

The NCV51511 integrates a bootstrap diode to supply the high side bias from $V_{DD}$ when HS pin potential is transited to ground by turned−on low side power MOSFET. The device has a boot diode with forward voltage drop at 0.8 V and dynamic resistance of 0.7 Ω to charge safely a bootstrap capacitor that is connected externally between HB and HO pins. Diode recovery time is specified as 50 ns at $I_F$ = 20 mA, $I_{REV}$ = 0.5 A. Bootstrap diode's dynamic impedance can limit peak forward current and prevent possible damage from high repetitive peak current occurred in many of systems. If integrated diode rating is not enough to drive very high frequency in applications with large sized bootstrap capacitance, the external Schottky diode might be preferable. In addition, the peak current rating of bootstrap diode can be exceeded by high VDD supply voltage and large sized bootstrap capacitance in initial charing process so, it might be required to add the external current limiting resistor, $R_{BOOT}$, in series with the bootstrap capacitor to prevent over demanding of internal diode as shown in Figure 26. However, it's important to also realize having an effect on switching performance of high side MOSFET when the bootstrap series resistor is installed with bootstrap capacitor because the bootstrap resistor limits the current available to charge the gate of the high side MOSFET. The bootstrap resistor is recommended to select value less than 5 Ω.

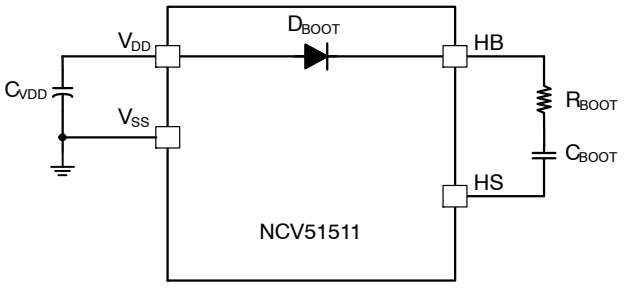



**Figure 26. External Current Limiting Resistor**

### Under−Voltage Lockout (UVLO)

Both high side and low side drivers have independent UVLO protections which monitor the VDD supply voltage and HB bootstrap voltage. The function of the UVLO circuits is to ensure that there are enough supply voltages (VDD and HB) to correctly bias high side and low side circuits. This also ensures that the gate of external MOSFETs is driven at an optimum voltage. If the VDD is below the VDD UVLO level, both low side and high side driver output keep low. If HB voltage is lower than HB UVLO but VDD is above VDD−on level, the high side driver output remains low and low side driver output can be controlled according to LI signal. Both VDD and VHB UVLO circuits have hysteresis features to avoid errors caused by ground noise in the power supply as well as to ensure continuous operation in case of slight drop when device starts switching and operation current is increased. Timing diagram of UVLO function is depicted in the Figure 25 and it is to illustrate the typical operating conditions – there are input filters in UVLO block that one needs to take into account when dimensioning all surrounding components and during the validation of the complete design under all worst case operating conditions.

### Output Stage

The NCV51511 output stage is able to Sink / Source 3.0 A / 6.0 A typical which can effectively charge and discharge a 1 nF load in few ns. High−speed switching, low resistance and high current capability of both high side and low side drivers allow for efficient switching operation. The

low side driver is referenced from VDD to VSS and the high side is referenced from HB to HS. The device logic status shows as below.

**Table 7. DEVICE LOGIC STATUS**

| | HI | LI | HO | LO |
|---|---|---|---|---|
| Status | L | L | L | L |
| | L | H | L | H |
| | H | L | H | L |
| | H | H | H | H |
| | X | X | L | L |

### Select Bootstrap and VDD Capacitor

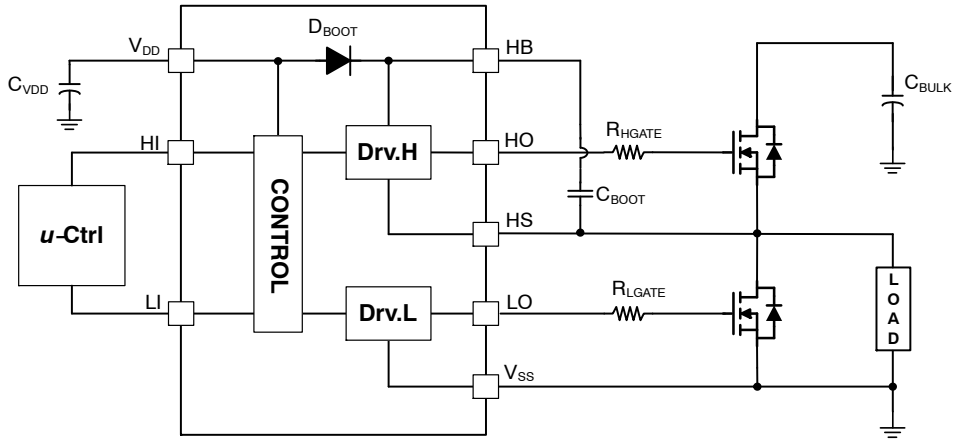



**Figure 27. Application Circuit**

**Table 8. DESIGN REQUIREMENTS**

| Parameter | Value |
|---|---|
| DC Input Voltage range, $V_{IN}$ | 38 V ~ 60V |
| Regulated DC Output Voltage, $V_{OUT}$ | 28 V |
| Maximum ouput current, $I_{OUT}$ | 11 A |
| Operating Frequency, $F_{SW}$ | 200 kHz |
| MOSFET | FDMS86101, $Q_G$ = 39 nC (typ), $R_G$ = 1.0 Ω |
| Supply Voltage, $V_{DD}$ | 10 V |

The NCV51511 has two independent drivers for half bridge application as shown Figure 27. The low side driver is powered from VDD while the high side driver is supplied by the bootstrap capacitor CBOOT charged through the integrated bootstrap diode from VDD when HS pin is connected to VSS by fully discharged inductor or turned−on low side power MOSFET. Therefore, the bootstrap capacitor should be designed for VHB−HS to even higher than UVLO threshold for safe operation and the maximum ripple votlage, $\Delta V_{HB,}$ produced in the process charged from VDD capacitor needs to take into consideration. Let's determine the acceptable ripple voltage to 2% of normal value and it can be obtained with Eq. 1.

$$\Delta V_{HB} = (V_{DD} - V_f) \times 2\% = (10\ V - 1\ V) \times 2\% = 0.18\ V \quad \text{(eq. 1)}$$

Where:

- $V_{DD}$: Gate drive IC supply voltage
- $V_f$ : Static forward voltage drop of bootstrap diode

The discharging in Cboot is occurred by charging high side power MOSFET and by high driver current consumption during switching cycle. Of course, the leakage currents between HB and VSS pins are existed but it can be ignored due to small amount energy relatively. In design

example, if $Q_G$ of FDMS86101 have 39 nC, total charge during switching cycle can be estimated from Eq.2.

$$Q_{TOTAL} = Q_G + \frac{I_{HB}}{f_{SW}} = 39\ nC + 1\ nC = 40\ nC \quad \text{(eq. 2)}$$

Where:

- $Q_G$: Total MOSFET gate charge provided from datasheet
- $I_{HB}$ : the HB Quiescent current

The estimated total charge and ripple voltage can be used to calculate the minimum bootstrap capacitance as Eq.3

$$C_{BOOT.min} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{40\ nC}{0.18\ V} = 222\ nF \quad \text{(eq. 3)}$$

The calculated capacitance is the minimum values and it should be noted that capacitance is dependant on bias voltage applied. The value of bootstrap capacitance needs to be higher than calculated value because the parasitic components in whole driving circuits and unexpected transient noses in power stages may make $V_{HB}$ ripple voltage worse than estimated actually. It's recommended to use 470 nF for bootstrap capacitor value in this example.

$C_{VDD}$ capacitor should be at least over 10 times the chosen value of $C_{BOOT}$ and 4.7 μF is selected to make the ripple voltage of $V_{DD}$ sufficiently small in this example. Both $C_{BOOT}$ and $C_{VDD}$ capacitors need to be placed close to driver pins. Additionally, the ceramic capacitor with small size and around 100 nF value should be placed to filter high frequency noises in parallel with $C_{VDD}$.

### Select Gate Resistor

The external gate resistors depicted in Figure 27 are used to reduce ringing voltage occurred by the parasitic inductances, to reduce high dV/dt when high transient voltage is applied on HB pin and to attenuate EMI radiation. However, too high resistors make the switching speed of power MOSFETs slower and lead to increase switching losses because the gate resistors limits the current capability of the gate driver output by the resistance value. Therefore, the proper value should be selected depending on power MOFET and applications to keep balance between system efficiency and safe operations. The NCV51511 driving current capabilities can be calculated by following equations from Eq. 4 to 7.

$$I_{OHH} = \frac{V_{DD} - V_f - V_{OHH}}{R_{H.gate} + R_G} \quad \text{(eq. 4)}$$

Where:

- $I_{OHH}$: high side peak source current
- $V_{OHH}$: high level output voltage drop in high side
- $R_G$: the MOSFET internal gate resistance provided from datasheet

$$I_{OLH} = \frac{V_{DD} - V_f - V_{OLH}}{R_{H.gate} + R_G} \quad \text{(eq. 5)}$$

Where:

- $I_{OLH}$: high side peak sink current
- $V_{OLH}$: low level output voltage drop in high side

$$I_{OHL} = \frac{V_{DD} - V_{OHL}}{R_{L.gate} + R_G} \quad \text{(eq. 6)}$$

Where:

- $I_{OHL}$: low side peak source current
- $V_{OHL}$: high level output voltage drop in low side

$$I_{OLL} = \frac{V_{DD} - V_{OLL}}{R_{L.gate} + R_G} \quad \text{(eq. 7)}$$

Where:

- $I_{OLL}$: low side peak sink current
- $V_{OLL}$: low level output voltage drop in low side

### Gate Driver Power Dissipation

The total power dissipation is the sum of power losses in different function blocks of gate driver device. The gate driver losses include:

- Static losses related with static current at high and low side circuit blocks when driver is biased and not switching.
- Dynamic losses related with dynamic current when the switching signal is applied and also directly dependent on switching frequency.

The static losses are associated with the quiescent current drawn from device in no load stage and the leakage current in the level shifter circuits of high side driver which are dependent on the voltage supplied on the HS pin and proportional to the duty cycle when only the high side power MOSFET is turned on. The quiescent current is consumed by the device through all internal logic circuits such as input stage, reference voltage, etc. The power loss for the quiescent can be expressed from following equation.

$$P_Q = (V_{DD} \times I_{DD}) + (V_{DD} - V_f) \times I_{HB} = \\ = 10\ V \times 0.3\ mA + 9\ V \times 0.2\ mA = 4.8\ mW \quad \text{(eq. 8)}$$

Where:

- IDD: the Quiescent current when no input signal is applied
- IHB : the leakage current in level shift circuits

Power losses for leakage current between VHB and VSS can be obtained from Eq. 9.

$$P_L = V_{HB} \times I_{HBS} \times D_{Max} = 69\ V \times 10\ \mu A \times 0.74 = \\ = 0.51\ mW \quad \text{(eq. 9)}$$

Where, Dmax is the max duty cycle of high side MOSFET in example.

The dynamic losses in the gate driver are related to power losses consumed when switching signal is applied, hence those losses will be proportional to switching frequency. The first dynamic loss is defined as the losses occurened by the current driving the level shifter circuits for the high side drivers and it is proportional to total charges in level shifter circuits which is normally not specified in datasheet but the value can be assumed as 1 nC in this cases as a rule of thumb. The driving losses, $P_{LS}$, in level shifter can be expressed as Eq.10.

$$P_{LS} = V_{HB} \times Q_P \times f_{SW} = 69\ V \times 0.48\ nC \times 200\ kHz = = 6.62\ mW \quad \text{(eq. 10)}$$

Where, $Q_P$ is the total gate charge for internal level shifter.

The second dynamic loss is the driving loss resulting from supplying gate current to drive power MOSFET and it accounts over 90% of total power dissipations in the gate driver device because Power MOSFET has pretty big input capacitance as gate driver loads and the driving currents are dependent on the total charge value which is proportional to the capacitance and driving voltage. The driving loss are having coming from charging and discharging the input capacitor of MOSFET, so it can be obtained from the following equation.

$$P_{CH} = P_{DCH} = 0.5 \times V_{DD} \times Q_G \times f_{SW} \quad \text{(eq. 11)}$$

The total gate driving losses, $P_{DR}$, in high and low side drivers is then 4 times $P_{CH}$.

$$P_{DR} = 2 \times V_{DD} \times Q_G \times f_{SW} = = 2 \times 10\ V \times 39\ nC \times 200\ kHz = 156\ mW \quad \text{(eq. 12)}$$

The power dissipation in bootstrap circuit is the sum of the bootstrap diode losses and the bootstrap resistor losses if any exist. The bootstrap diode loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to switching frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor, resulting in more losses.

### PCB Layout Guideline

First of all, the influence of the parasitic inductance and capacitance on the PCB layout should be minimized to optimize the gate driving operation in high and low side. The following should be considered before beginning a PCB layout using the NCV51511.

- The gate driver should be located nearby switching MOSFET as possible.
- The $V_{DD}$ capacitor and bootstrap capacitor should be located near by the device.
- In order to reduce ringing voltage of the HS node, the length both high side source and low side drain of the MOSFET should be close as possible.
- The exposed pad should be connected to VSS plane and use at least four or more vias for better thermal performance.
- Avoid being close to the driver input pulse signal with HB node.

One of recommendation layout pattern for the driver is shown in Figure 28.

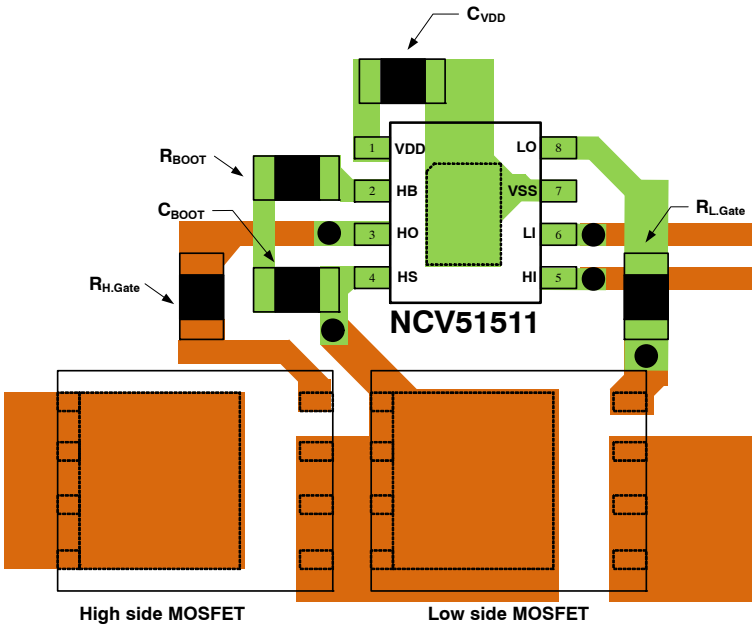



**Figure 28. Layout Recommendation**

## ORDERING INFORMATION

| Device | Output Configuration | Temperature Range (°C) | Package | Shipping† |
|---|---|---|---|---|
| NCV51511PDR2G | High−Side and Low−Side | −40 to 150 | SOIC8−EP (Pb−Free) | Tape & Reel |
| TBD | High−Side and Low−Side | −40 to 150 | SOIC (Pb−Free) | Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

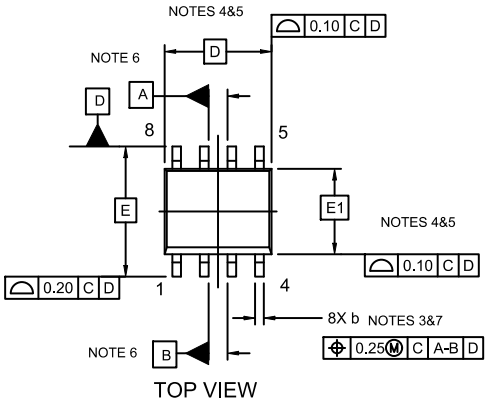
**SCALE 1:1**

**SOIC−8 EP**
CASE 751AC
ISSUE E

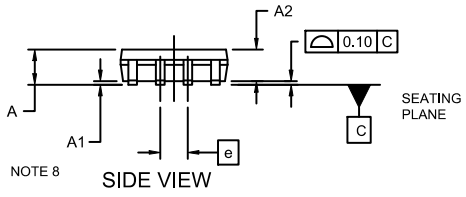
DATE 05 OCT 2022

NOTES:

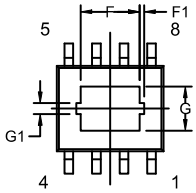
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



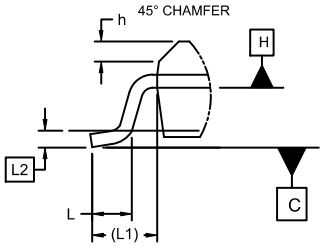
TOP VIEW



SIDE VIEW

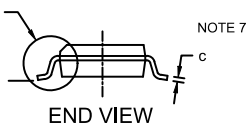


BOTTOM VIEW

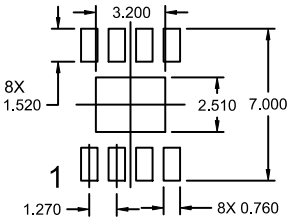


DETAIL A

DETAIL A



END VIEW

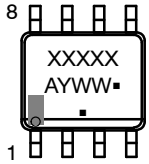


RECOMMENDED
MOUNTING FOOTPRINT*

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM.. | MAX. |
| A | 1.35 | 1.55 | 1.75 |
| A1 | --- | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.17 | 0.21 | 0.23 |
| D | 4.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| F | 2.24 | 2.72 | 3.20 |
| F1 | | 0.20 REF | |
| G | 1.55 | 2.03 | 2.51 |
| G1 | | 0.46 REF | |
| h | 0.25 | 0.38 | 0.50 |
| L | 0.40 | 0.84 | 1.27 |
| L1 | 1.04 REF | | |
| L2 | 0.25 REF | | |
| Ø | 0° | 4° | 8° |

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

## GENERIC MARKING DIAGRAM*




XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

| DOCUMENT NUMBER: | 98AON14029D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SOIC−8 EP | PAGE 1 OF 1 |

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**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

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**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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