STANDARD MICROSYSTEMS CORPORATION

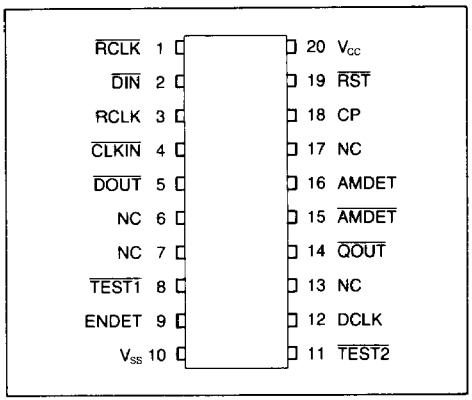
HDC 1100-03
PRELIMINARY

Hard Disk Address Mark Detector

FEATURES

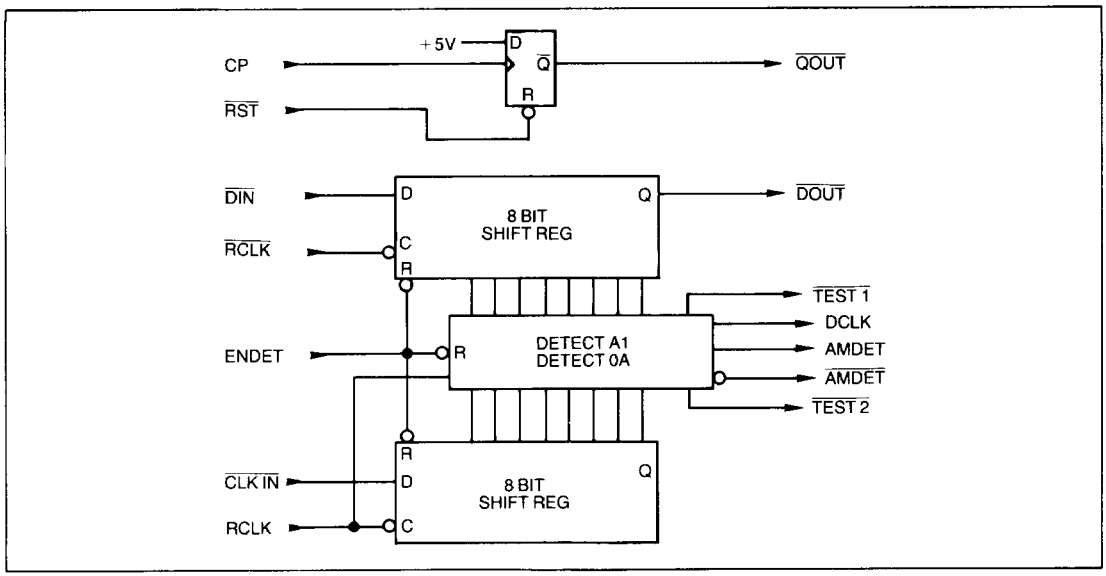
- ☐ Single +5 Volt Power Supply
- ☐ Decodes A1-0A
- ☐ Synchronous Clock/Data Outputs
- ☐ 5 MBit Data Rate
- ☐ Address Mark Detection
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-03 Address Mark Detector Provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM clocks and data are fed to the device along with a window clock generated by an external data separator. The HDC 1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces and AM DET signal when the pattern has been found. NRZ data is output from the device for driving a serial/parallel converter. An uncommitted latch is also provided for use by the data separator circuitry if required.



SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{RCLK}$	$\overline{READ\ CLOCK}$	Complimentary clock inputs used to clock DIN and $\overline{CLK\ IN}$ into the AM detector.
3	RCLK	READ CLOCK	
2	$\overline{DIN}$	$\overline{DATA\ INPUT}$	MFM data pulses from the external Data Separator are connected on this line.
4	$\overline{CLK\ IN}$	$\overline{CLOCK\ INPUT}$	MFM clock pulses from the external Data Separator are connected on this line.
5	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	Data Output from the internal Data Shift register, synchronized with DCLK.
6, 7, 13, 17	NC	No Connection	To be left open by the user.
8 11	$\overline{TEST\ 1}$ $\overline{TEST\ 2}$	$\overline{TEST\ 1}$ $\overline{TEST\ 2}$	To be left open by the user.
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search for a data $A1_{16}$ and clock.
10	V_{SS}	V_{SS}	GROUND.
12	DCLK	DATA CLOCK	Clock output that is synchronized with $\overline{DATA\ OUT}$ (Pin 5).
14	$\overline{QOUT}$	$\overline{LATCH\ OUTPUT}$	Signal output from the uncommitted latch.
15	$\overline{AMDET}$	$\overline{ADDRESS\ MARK\ DETECT}$	Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$ pattern is detected in the data stream.
16	AMDET	ADDRESS MARK DETECT	
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the $\overline{QOUT}$ (Pin 14) to be latched at a logic 0.
19	$\overline{RST}$	$\overline{RESET}$	A logic 0 on this line will cause the QOUT (Pin 14) signal to be set at a logic 1.
20	V_{CC}	V_{CC}	+5V power supply input.

OPERATION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and AMDET, $\overline{AMDET}$, DCLK, and $\overline{DATA\ OUT}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{DIN}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{RCLK}$ (Pin 1). NRZ clocks are entered on the $\overline{CLK\ IN}$ line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{DOUT}$ line (Pin 5) is tied to the last stage of the Internal Data Shift register and will reflect information clocked into the $\overline{DIN}$ line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$ CLK = $0A_{16}$ pattern. When this pattern is detected, $\overline{AMDET}$ will be set to a logic 0 and AMDET will be set to a logic 1. $\overline{AMDET}$ and AMDET will remain latched until the device is re-initialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{DOUT}$ line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high-frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{QOUT}$ (Pin 14) to a logic 0. $\overline{QOUT}$ may be reset back to a logic 1 by a low level on the RST line (Pin 19).

$\overline{TEST1}$ and $\overline{TEST2}$ are output lines. $\overline{TEST1}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{TEST2}$ is an active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +50°C
Storage Temperature Range	−55° to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+7.0V
Negative Voltage on any I/O Pin, with respect to ground	−0.2V
Power Dissipation	0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rat… …eration of the device at these or at any other condition above those indicated in the operational sections of t…

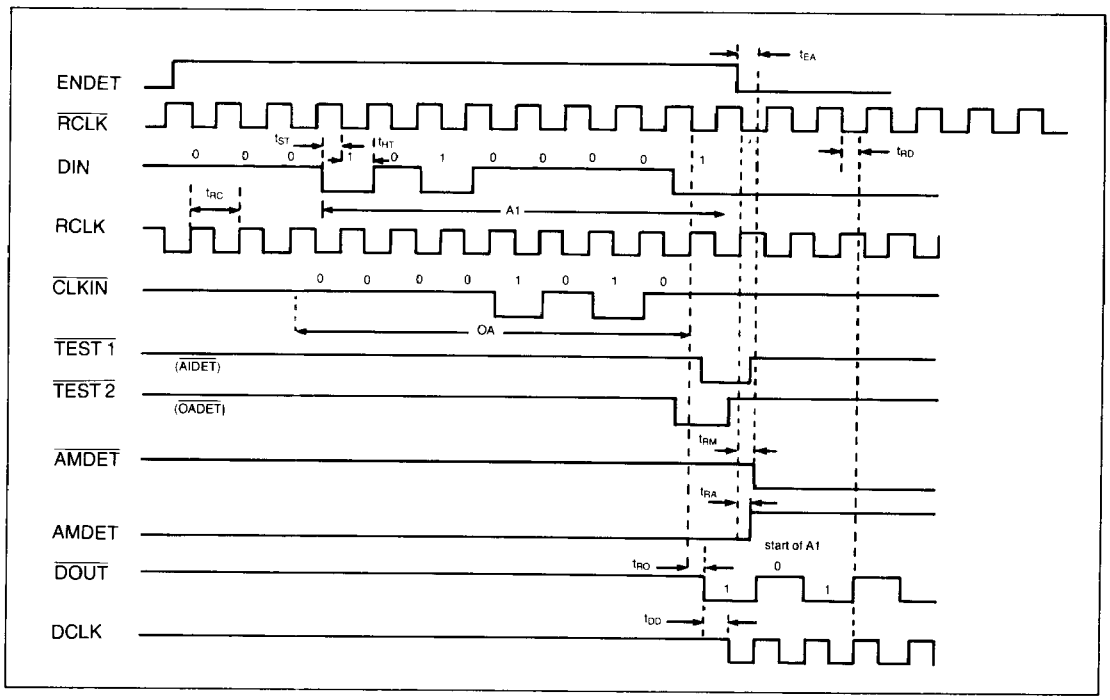
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.7	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{RC}	RCLK Frequency			5.25	MHZ	
t_{ST}	Data Setup time	40			nsec	
t_{HT}	Data Hold time	10			nsec	
t_{DD}	$\overline{DOUT}$ to DCLK DELAY			110	nsec	
t_{RD}	↓ $\overline{RCLK}$ to ˙DCLK			120	nsec	
t_{RA}	↓ $\overline{RCLK}$ to ˙$\overline{AMDET}$			115	nsec	
t_{RM}	↓ $\overline{RCLK}$ to ˙$\overline{AMDET}$			125	nsec	
t_{RO}	↓ $\overline{RCLK}$ to $\overline{DOUT}$			135	nsec	
t_{EA}	↓ $\overline{ENDET}$ to ↓ AMDET			130	nsec	
t_{RQ}	↓ $\overline{RST}$ to ˙$\overline{QOUT}$			110	nsec	
t_{RW}	Pulse width of $\overline{RST}$	50			nsec	
t_{CW}	CP Pulse width	90			nsec	
t_{CQ}	˙CP to ↓ $\overline{QOUT}$			106	nsec	



SECTION VI