International
IOR Rectifier

IR21364(S&J)PBF
3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 11.5 V to 20 V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Low side and High side outputs in phase with inputs.
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- RoHS Compliant

Product Summary

Topology	3 phase bridge driver
V_{OFFSET}	≤ 600 V
V_{OUT}	11.5 V – 20V
I_{O+} & I_{O-} (typical)	200 mA & 350 mA
t_{ON} & t_{OFF} (typical)	500 ns & 530 ns

Typical Applications

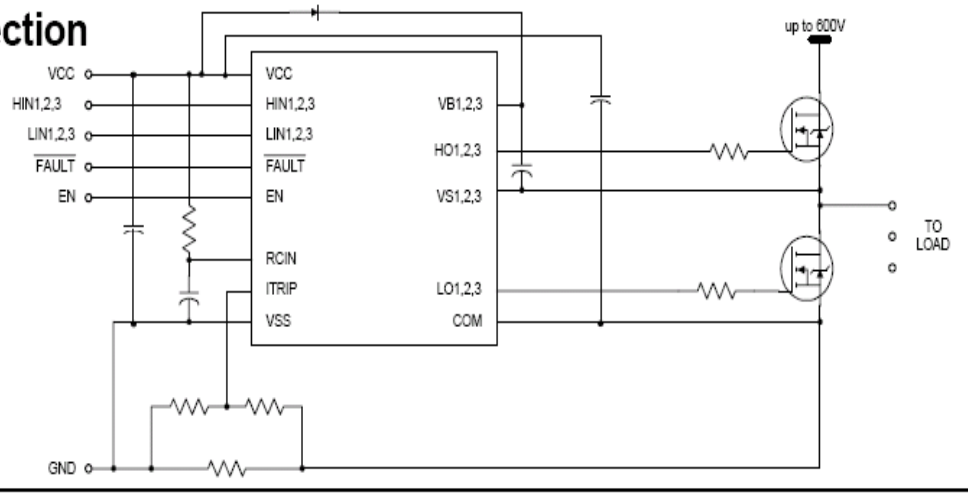
- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Package Options

28-Lead SOIC

44-Lead PLCC w/o 12 Leads

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Description

The IR21364(S&J)PBF is a high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC28W	MSL3†††, 260°C (per IPC/JEDEC J-STD-020)
		PLCC44	MSL3†††, 245°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)	
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
V_S	High side offset voltage		$V_{B\,1,2,3}$ - 25	$V_{B\,1,2,3}$ + 0.3	V
V_B	High side floating supply voltage		-0.3	625	
V_{HO}	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B\,1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{SS}	Logic ground		V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage LIN, HIN, ITRIP, EN, RCIN		V_{SS} -0.3	lower of V_{CC} + 0.3 or Vss+15	
V_{FLT}	FAULT output voltage		V_{SS} -0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C	(28 lead SOIC)	—	1.6	W
		(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead SOIC)	—	78	°C/W
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S & V_{SS} offset rating are tested with all supplies biased at a 15 V differential.

Symbol	Definition		Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	IR21364	$V_{S1,2,3}$ +11.5	$V_{S1,2,3}$ + 20	V
$V_{S\,1,2,3}$	High side floating supply voltage		Note 1	600	
V_{CC}	Low side supply voltage	IR21364	11.5	20	
$V_{HO\,1,2,3}$	High side output voltage		$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage		0	V_{CC}	
V_{SS}	Logic ground		-5	5	
V_{FLT}	FAULT output voltage		V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage		V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage		V_{SS}	V_{SS} + 5	
V_{IN}	Logic input voltage LIN, HIN, EN		V_{SS}	V_{SS} + 5	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of COM -5 V to COM + 600 V. Logic state held for V_S of COM -5 to COM – V_{BS}. (Please refer to the Design Tip DT97 -3 for more details).

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS\ 1,2,3}$) = 15 V, TA = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HIN1,2,3 and LIN1,2,3). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic “0” input voltage		—	—	0.8	V	
V_{IL}	Logic “1” input voltage		2.5	—	—		
$V_{EN,TH+}$	Enable positive going threshold		—	—	2.5		
$V_{EN,TH-}$	Enable negative going threshold		0.8	—	—		
$V_{IT,TH+}$	ITRIP positive going threshold		0.37	0.46	0.55		
$V_{IT,HYS}$	ITRIP hysteresis		—	0.07	—		
$V_{RCIN,\ TH+}$	RCIN positive going threshold		—	8	—		
$V_{RCIN,\ HYS}$	RCIN hysteresis		—	3	—		
V_{OH}	High level output voltage, V_{BIAS} - V_O		—	0.9	1.4		Io = 20 mA
V_{OL}	Low level output voltage, V_O		—	0.4	0.6		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	IR21364	9.6	10.4	11.2		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	IR21364	8.6	9.4	10.2		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	IR21364	—	1	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	IR21364	9.6	10.4	11.2		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	IR21364	8.6	9.4	10.2		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	IR21364	—	1	—		
Ilk	Offset supply leakage current		—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current		—	70	120		$V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V
I_{QCC}	Quiescent V_{CC} supply current		—	0.6	1.3	mA	V_{IN} = 0 V or 5 V
I_{LIN}+	Input bias current (LOUT = HI)		—	100	195	µA	V_{LIN} = 3.3 V
I_{LIN}-	Input bias current (LOUT = LO)		-1	—	—		V_{LIN} = 0 V
I_{HIN}+	Input bias current (HOUT = HI)		—	100	195		V_{HIN} = 3.3 V
I_{HIN}-	Input bias current (HOUT = LO)		-1	—	—		V_{HIN} = 0 V
I_{ITRIP+}	“High” ITRIP input bias current		—	3.3	6		V_{ITRIP} = 3.3 V
I_{ITRIP-}	“Low” ITRIP input bias current		-1	—	—		V_{ITRIP} = 0 V
I_{EN+}	“High” ENABLE input bias current		—	100	—		V_{EN} = 3.3 V
I_{EN-}	“Low” ENABLE input bias current		-1	—	—		V_{EN} = 0 V
I_{RCIN}	RCIN input bias current		—	—	1		Vrcin = 0 V or 15 V
Io+	Output high short circuit pulsed current		120	200	—	mA	Vo = 0 V, PW ≤ 10 µs
Io-	Output low short circuit pulsed current		250	350	—		Vo = 15 V, PW ≤ 10 µs
R_{on_RCIN}	RCIN low on resistance		—	50	100	Ω	I = 1.5 mA
R_{on_FAULT}	FAULT low on resistance		—	50	100		

Dynamic Electrical Characteristics

Dynamic Electrical Characteristics V_{CC} = V_{BS} = V_{BIAS} = 15 V, $V_{S1,2,3}$ = V_{SS} = COM, TA = 25°C and CL = 1000 pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	350	500	650	ns	V_{IN} = 0 V & 5 V
t_{off}	Turn-off propagation delay	375	530	685		
t_r	Turn-on rise time	—	125	190		
t_f	Turn-off fall time	—	50	75		
t_{EN}	ENABLE low to output shutdown propagation delay	300	450	600		$V_{IN,}$ V_{EN} = 0 V or 5 V
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1000		V_{ITRIP} = 5 V
t_{bl}	ITRIP blanking time	100	150	—		V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	800		
t_{FILIN}	Input filter time (HIN, LIN)	100	200	—		V_{IN} = 0 V & 5 V
$t_{filterEn}$	Enable input filter time	100	200	—		
DT	Deadtime	220	290	360		
MT	Ton, off matching time (on all six channels)	—	—	75		External dead time >450 nsec
MDT	DT matching (Hi->Lo & Lo->Hi on all channels)	—	—	70		
PM	pulse width distortion (pwin-pwout)	—	—	75		PW input =10 µs
t_{FLTCLR}	FAULT clear time RCIN: R = 2 MΩ, C = 1 nF	1.3	1.65	2	ms	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V

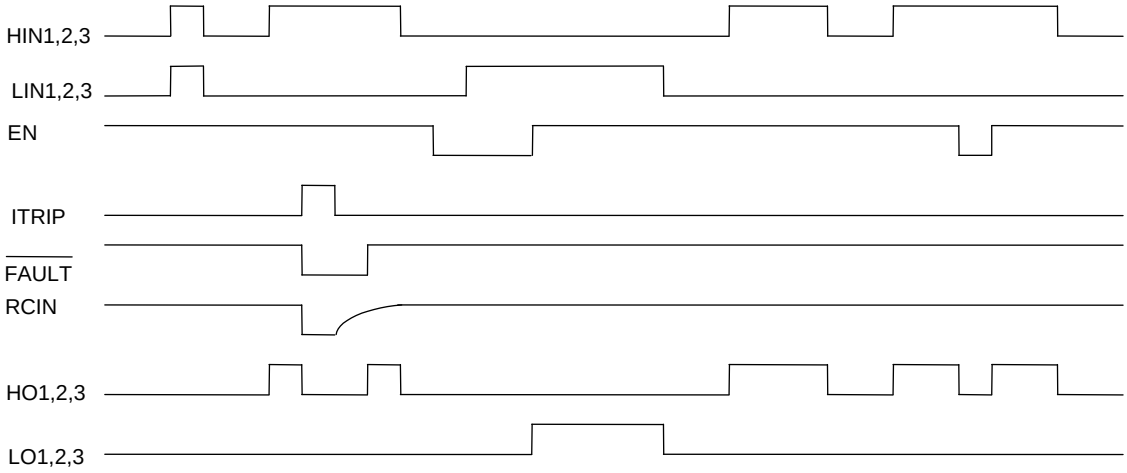


Fig. 1. Input/Output Timing Diagram

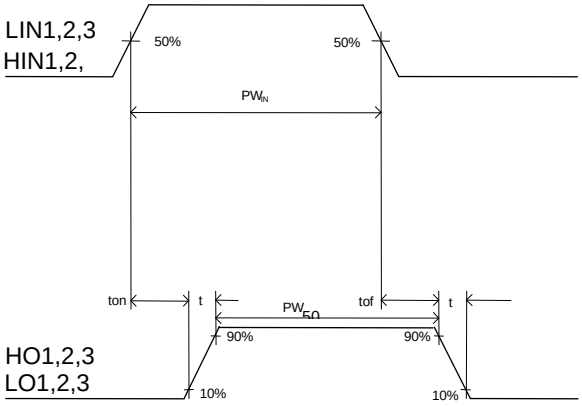


Fig. 2. Switching Time Waveforms

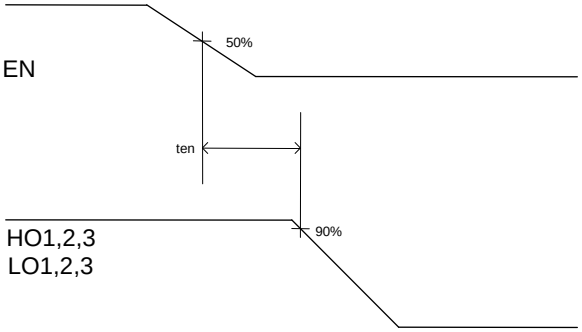


Fig. 3. Output Enable Timing Waveform

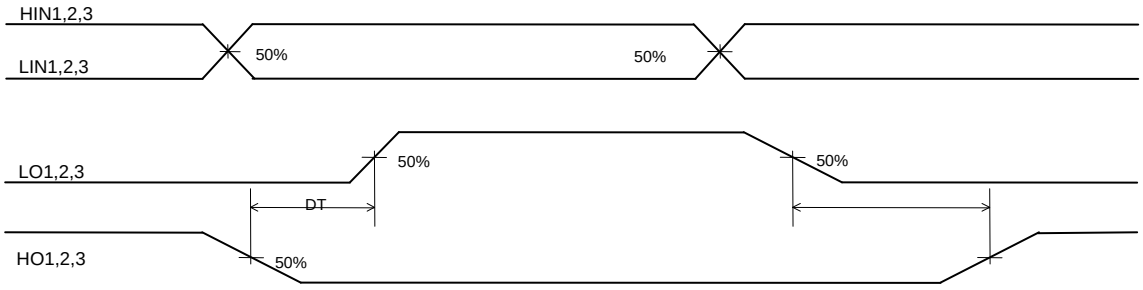


Fig. 4. Internal Deadtime Timing Waveforms

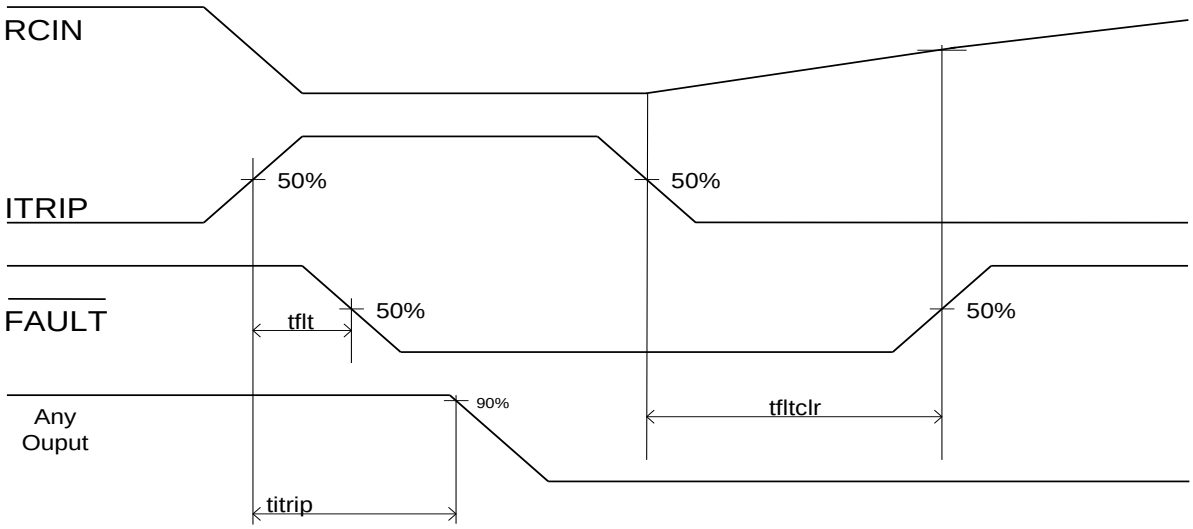


Fig. 5. ITRIP/RCIN Timing Waveforms

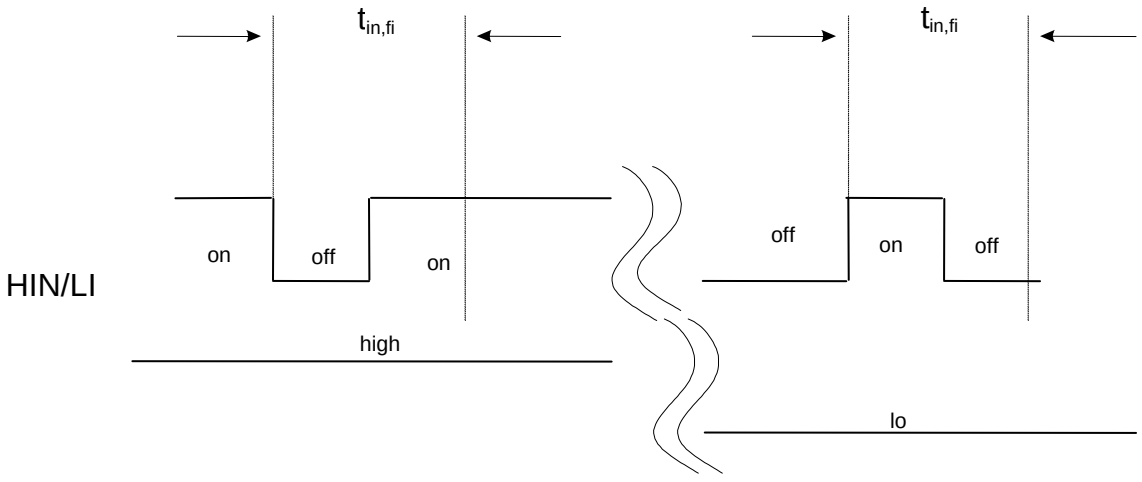
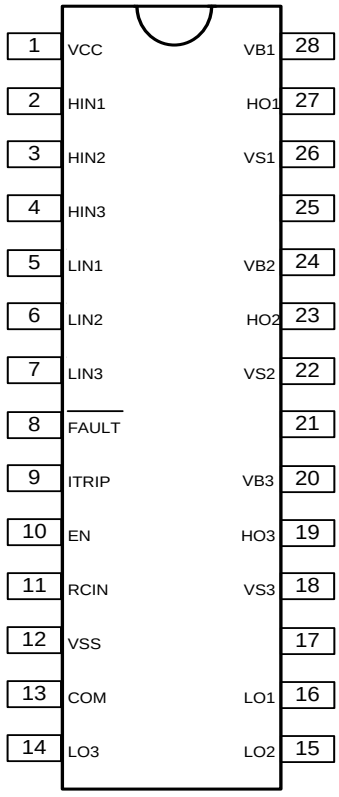


Fig. 6. Input Filter Function

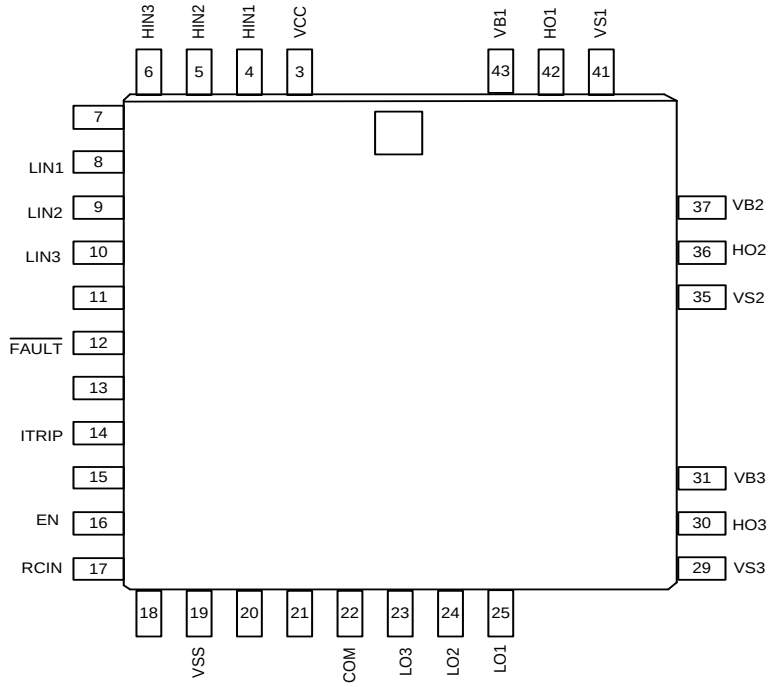
Lead Definitions

Symbol	Description
V_{CC}	Low side supply voltage
V_{SS}	Logic ground
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), in phase
LIN1,2,3	Logic input for low side gate driver outputs (LO1,2,3), in phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions When ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, $T_{FLTCLR,}$ approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate drivers return
$V_{B1,2,3}$	High side floating supply
HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply return
LO1,2,3	Low side gate driver outputs



28 Lead SOIC (wide body)

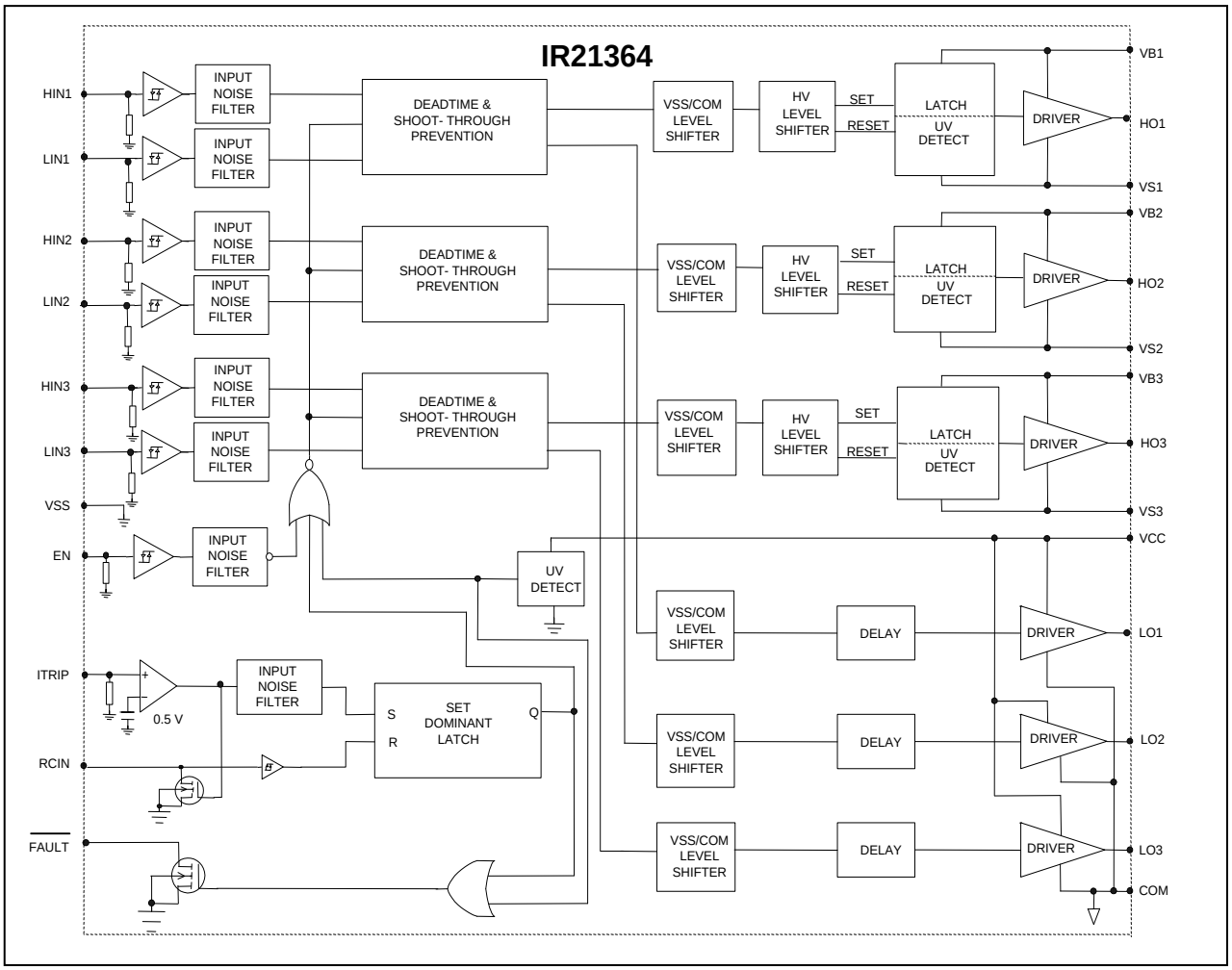
IR21364S



44 Lead PLCC w/o 12 leads

IR21364J

Functional Block Diagram



VCC	VBS	ITRIP	ENAB LE	FAULT	LO1,2,3	HO1,2,3
$<UV_{CC}$	X	X	X	0 (note 1)	0	0
15 V	$<U_{VBS}$	0 V	5 V	high imp	LIN1,2,3	0
15 V	15 V	0 V	5 V	high imp	LIN1,2,3	HIN1,2,3
15 V	15 V	$>V_{ITRIP}$	5 V	0 (note 2)	0	0
15 V	15 V	0 V	0 V	high imp	0	0

Note 1: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 2: U_{VCC} is not latched, when $V_{CC} > U_{VCC}$, FAULT return to high impedance.
Note 3: When ITRIP $<V_{ITRIP}$, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ V_{CC} = 15 V)

Parameter Temperature Trends

Figures 7-39 provide information on the experimental performance of the IR21364 HVIC. The line plotted in each figure is generated from actual lab data. A small number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood temperature trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

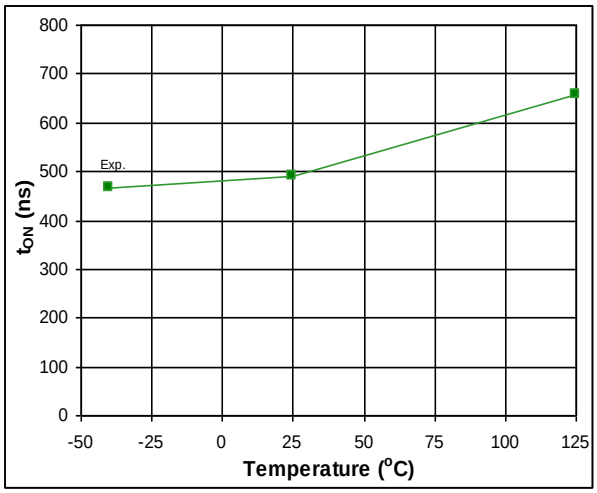


Fig. 7. (Ton_Ls1) Turn-on Propagation Delay vs. Temperature

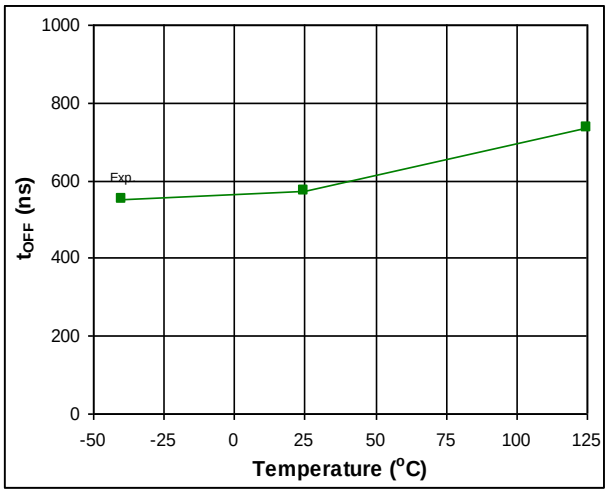


Fig. 8. (Toff_Ls1) Turn-off Propagation Delay vs. Temperature

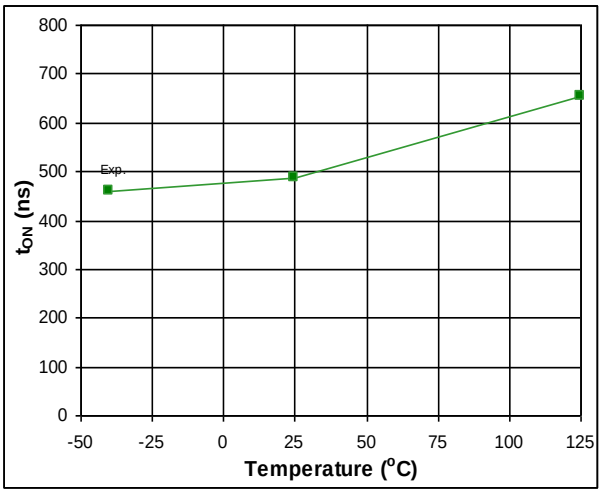


Fig. 9. (Ton_Hs11) Turn-on Propagation Delay vs. Temperature

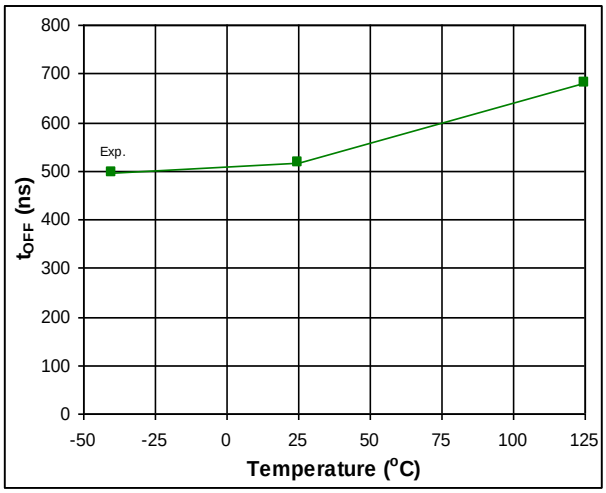


Fig. 10. (Toff_Hs21) Turn-off Propagation Delay vs. Temperature

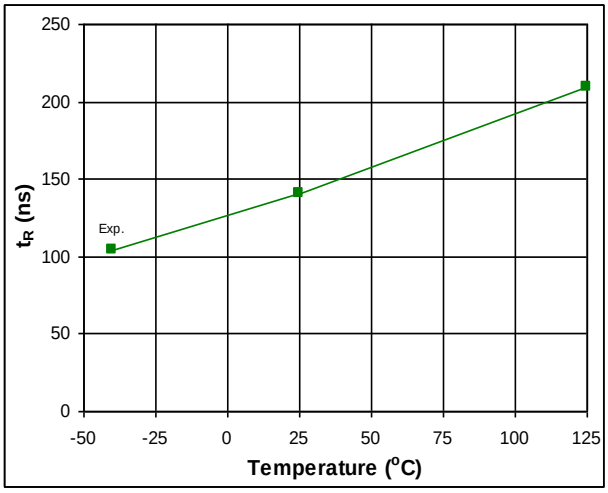


Fig. 11. Turn-on Rise Time vs. Temperature

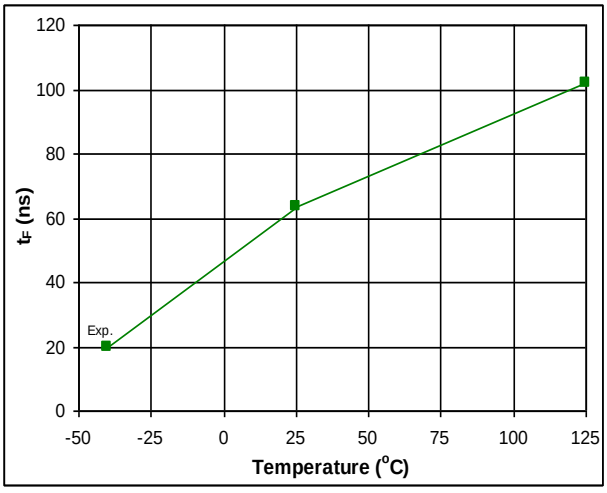


Fig. 12. Turn-off Fall Time vs. Temperature

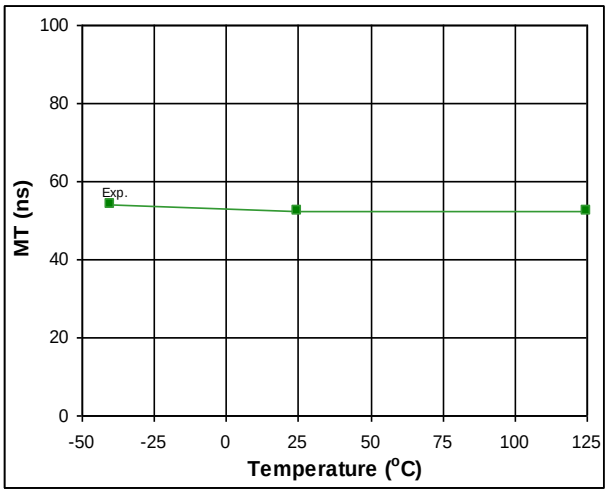


Fig. 13. Ton, off matching time vs. Temperature

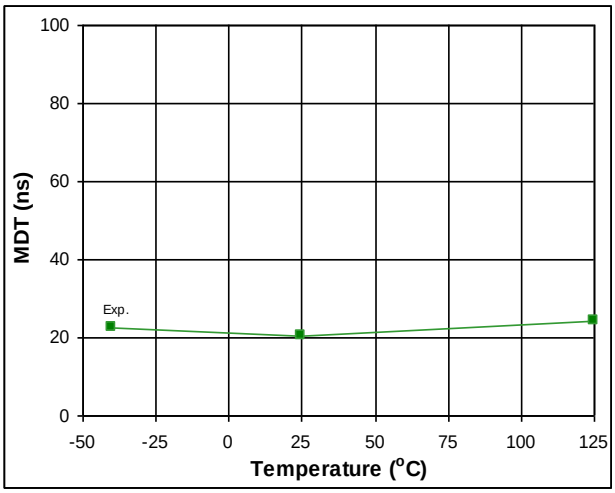


Fig. 14. DT matching time vs. Temperature

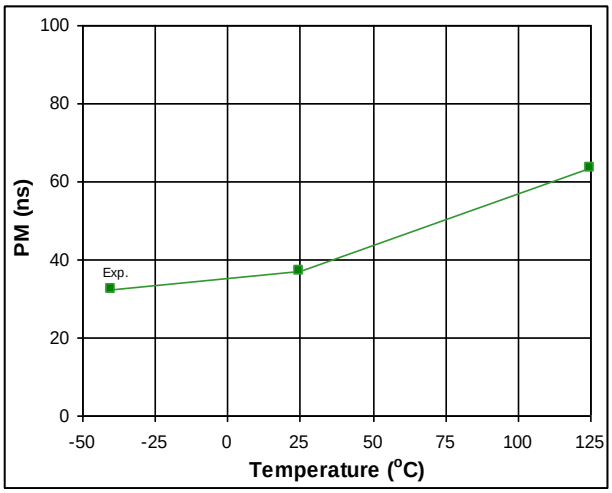


Fig. 15. Pulse Width Distortion vs. Temperature

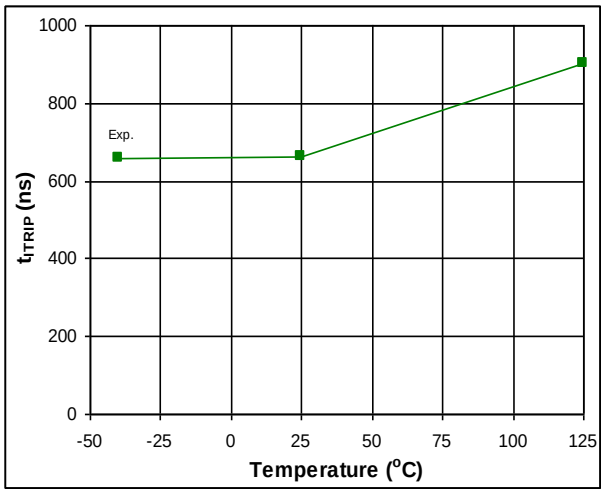


Fig. 16. ITRIP to Output Shutdown Propagation Delay vs. Temperature

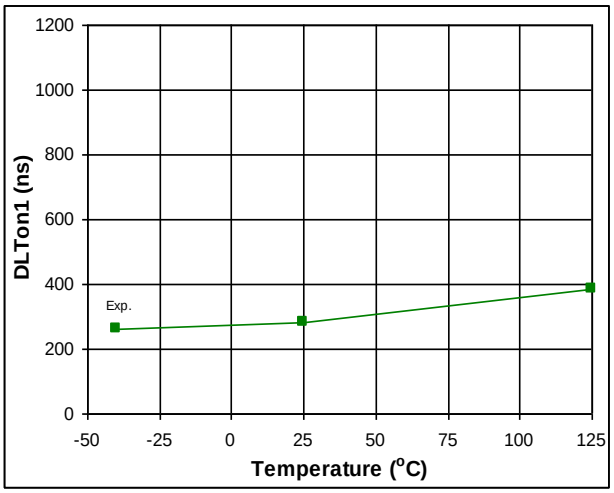


Fig. 17. Dead Time vs. Temperature

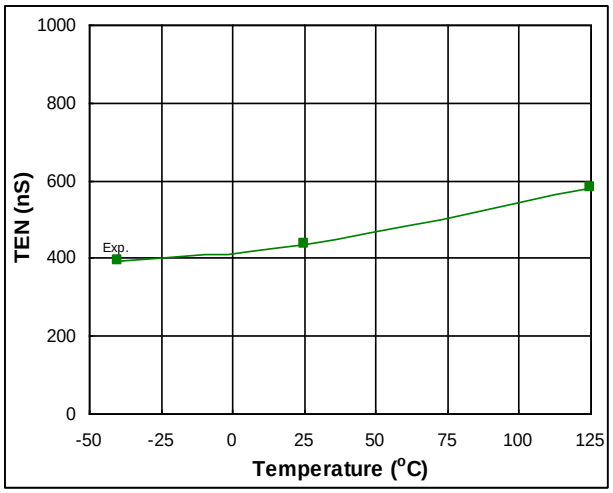


Figure 18. EN to Output Shutdown Time vs. Temperature

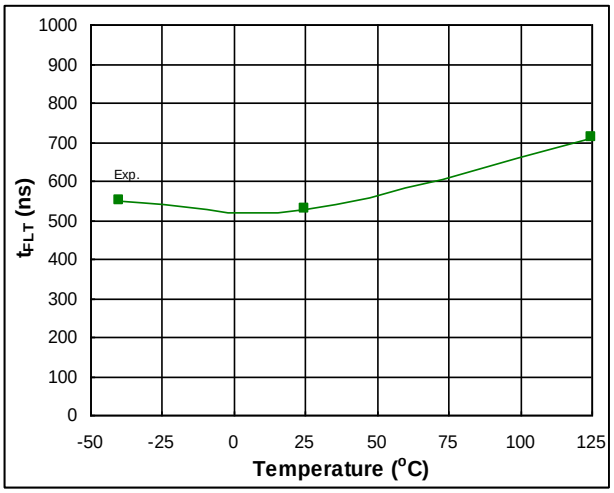


Fig. 19. ITRIP to FAULT Indication Delay vs. Temperature

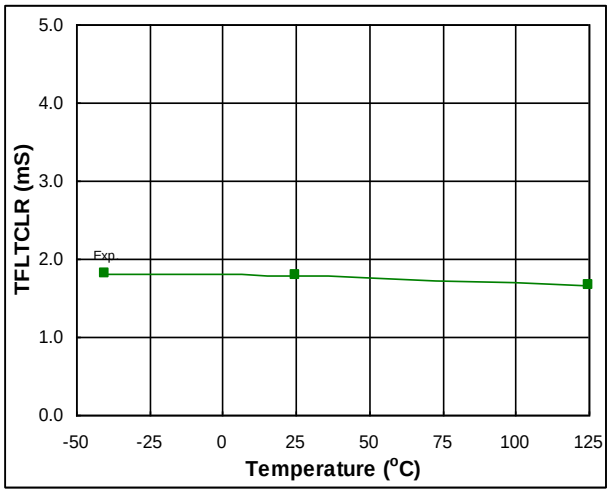


Fig. 20. FAULT Clear Time vs. Temperature

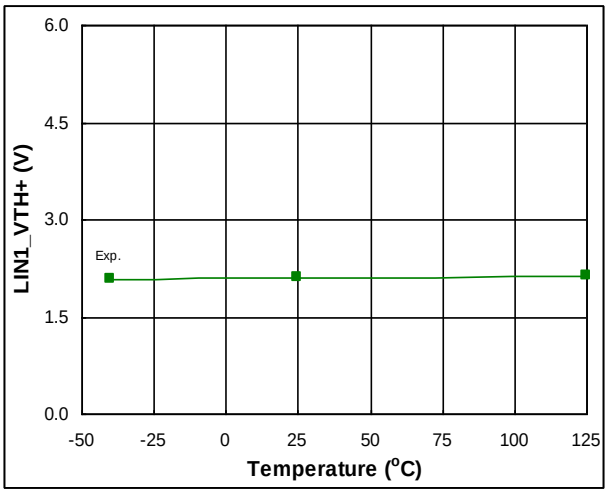


Fig. 21. Input Positive Going Threshold vs. Temperature

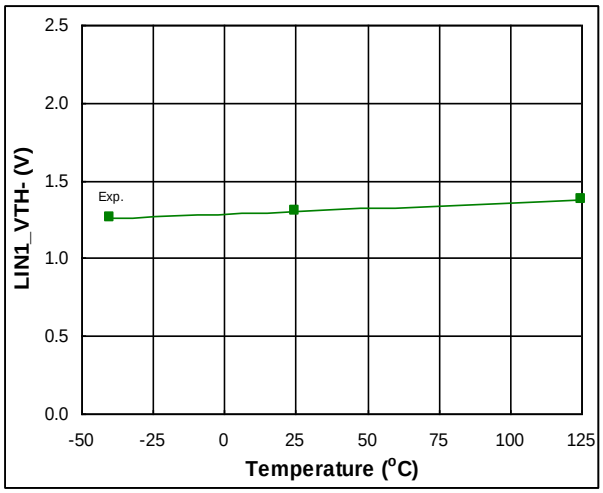


Fig. 22. Input Negative Going Threshold vs. Temperature

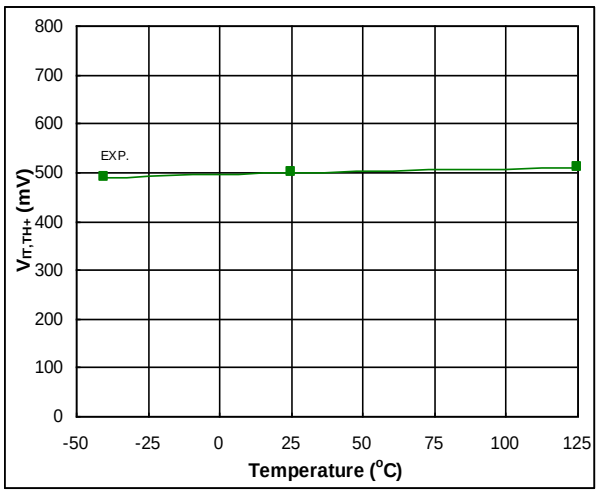


Fig. 23. ITRIP Input Positive Going Threshold vs. Temperature

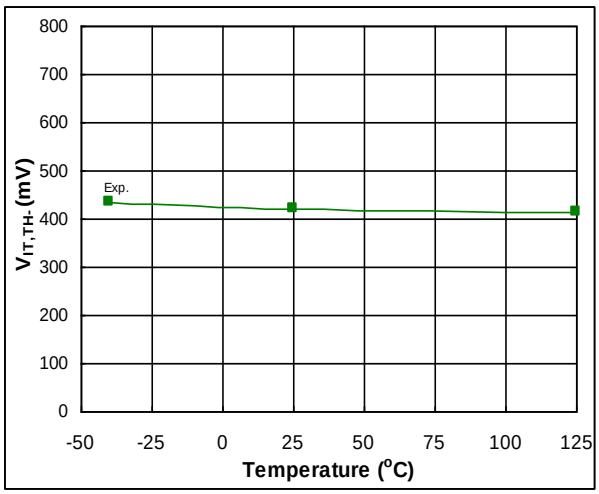


Fig. 24. ITRIP Input Negative Going Threshold vs. Temperature

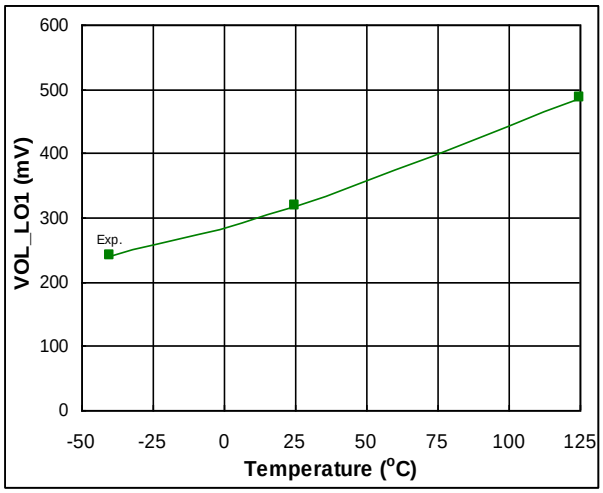


Fig. 25. Low Level Output Voltage vs. Temperature

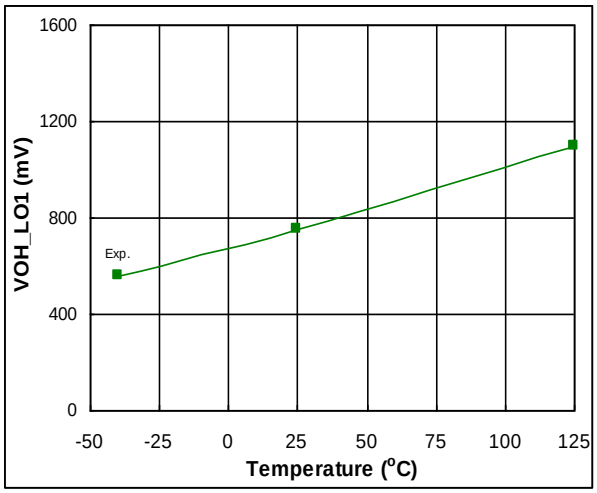


Fig. 26. High Level Output Voltage vs. Temperature

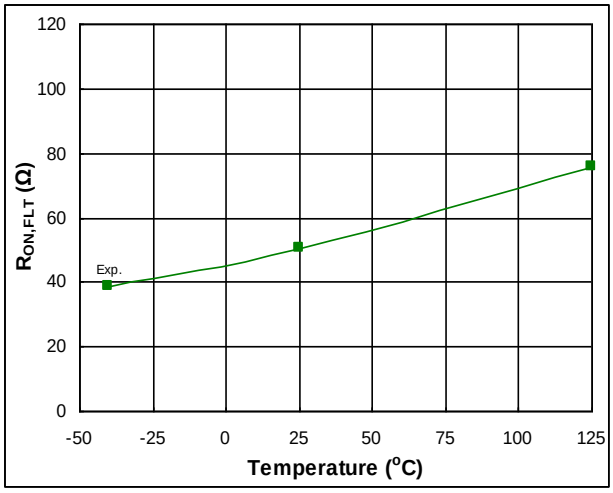


Fig. 27. FAULT Low On-Resistance vs. Temperature

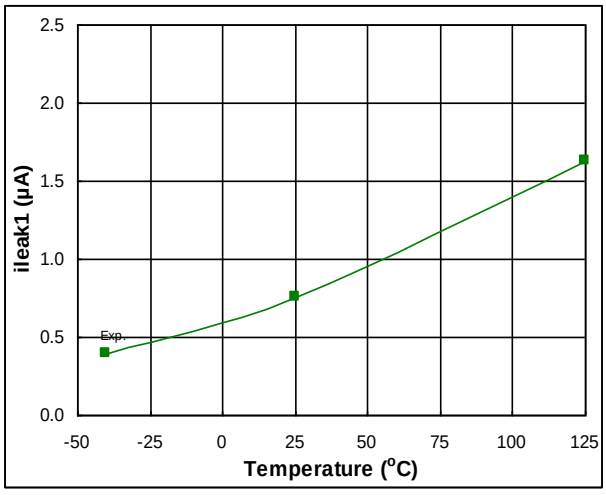


Fig. 28. Offset Supply Leakage Current vs. Temperature

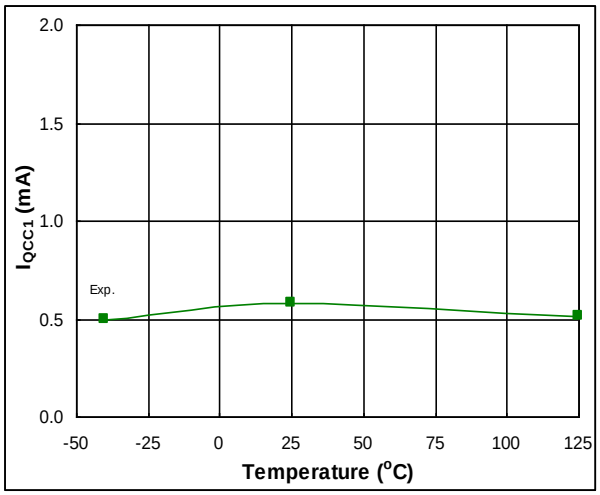


Fig. 29. Quiescent V_{CC} Supply Current vs. Temperature

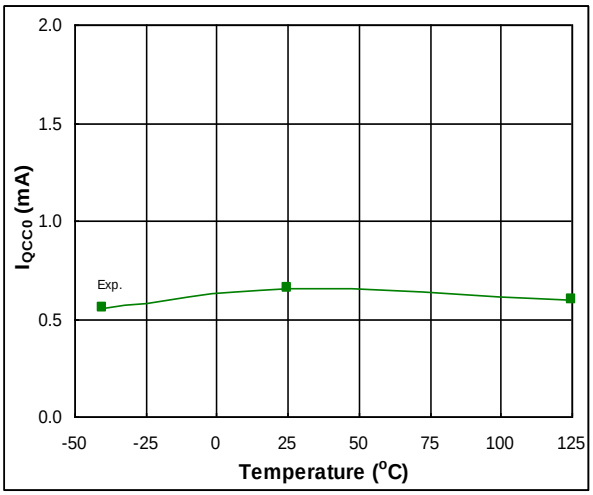


Fig. 30. Quiescent V_{CC} Supply Current vs. Temperature

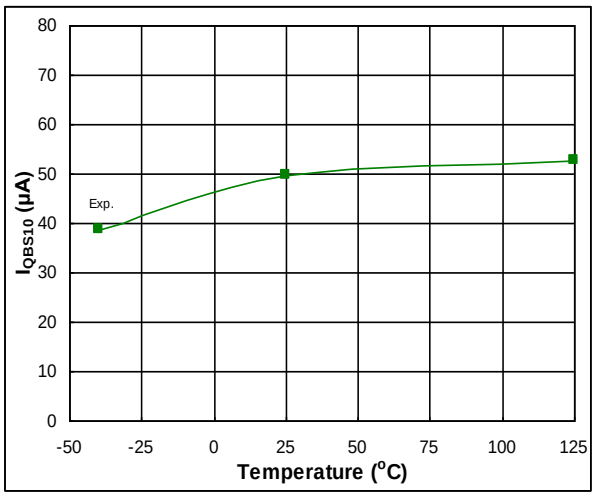


Fig. 31. Quiescent V_{BS} Supply Current vs. Temperature

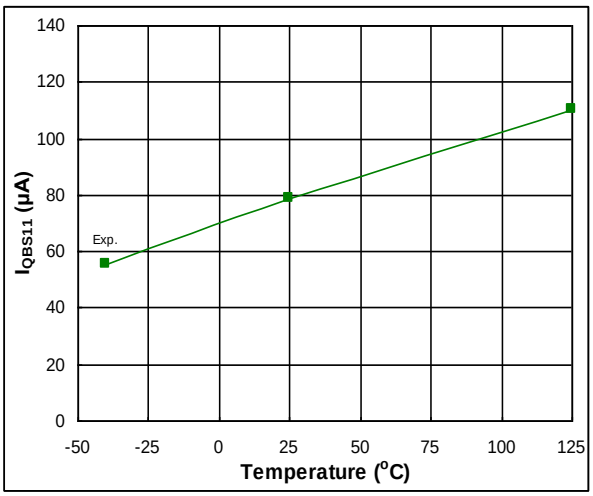


Fig. 32. Quiescent V_{BS} Supply Current vs. Temperature

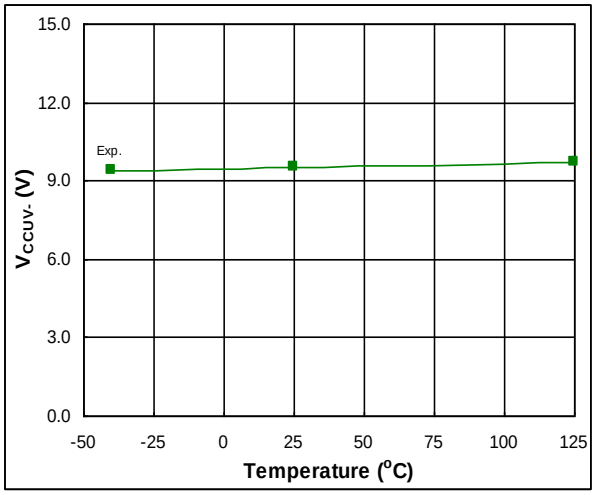


Fig. 33. V_{CC} Supply Undervoltage Negative Going Threshold vs. Temperature

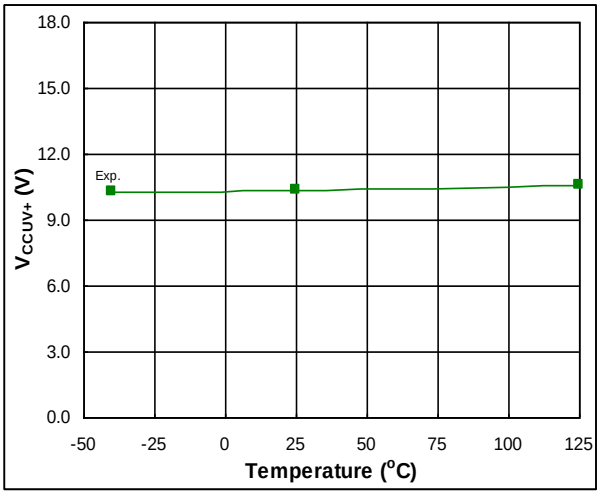


Fig. 34. V_{CC} Supply Undervoltage Positive Going Threshold vs. Temperature

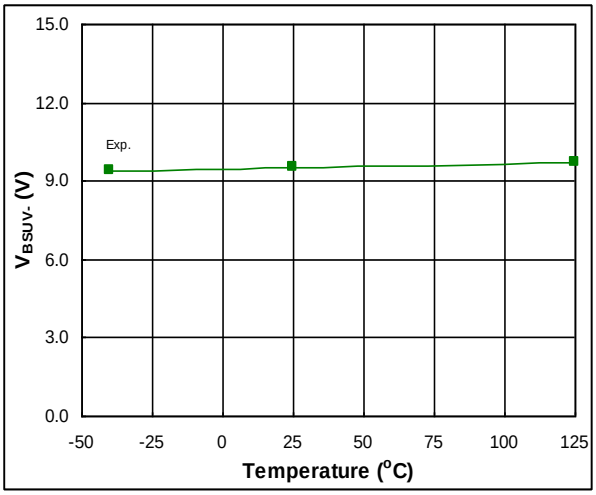


Fig. 35. V_{BS} Supply Undervoltage Negative Going Threshold vs. Temperature

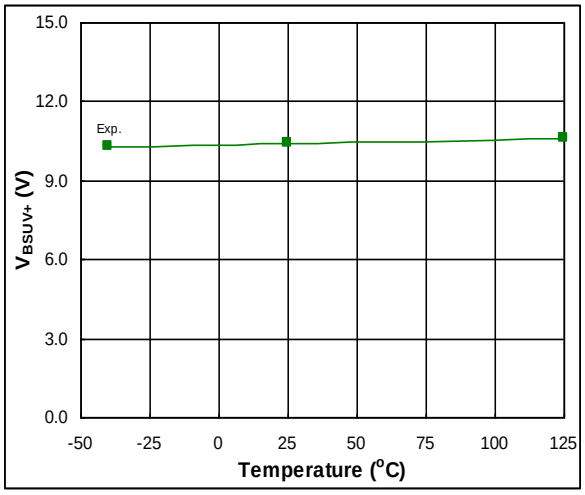


Fig. 36. V_{BS} Supply Undervoltage Positive Going Threshold vs. Temperature

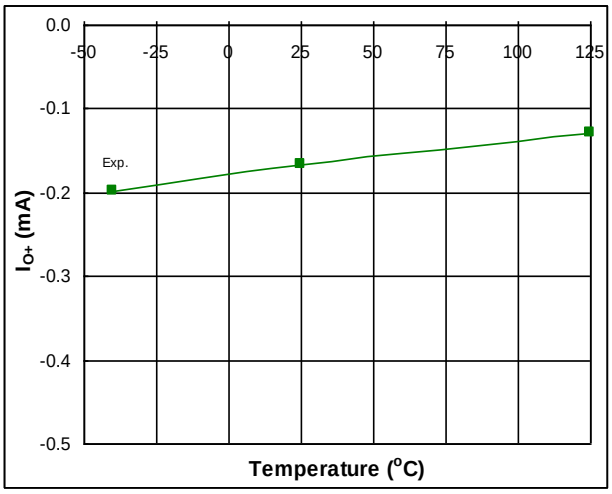


Fig. 37. Output High Short Circuit Pulsed Current vs. Temperature

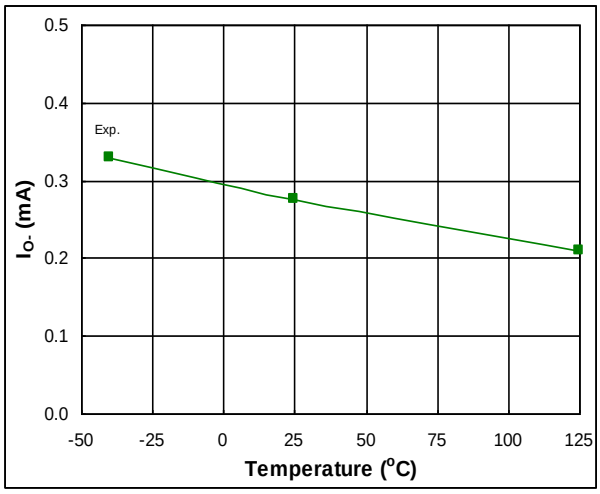


Fig. 38. Output Low Short Circuit Pulsed Current vs. Temperature

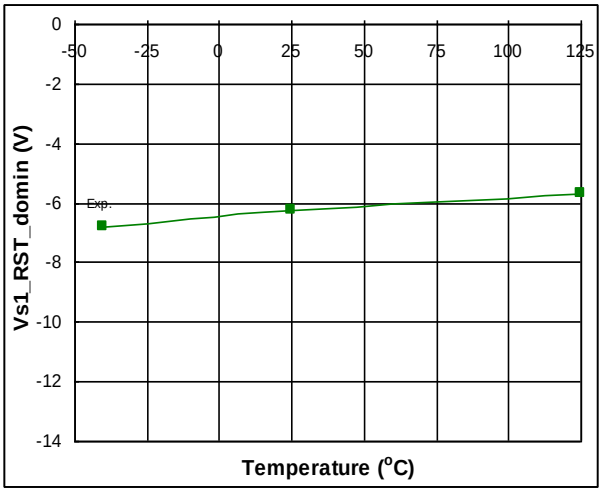
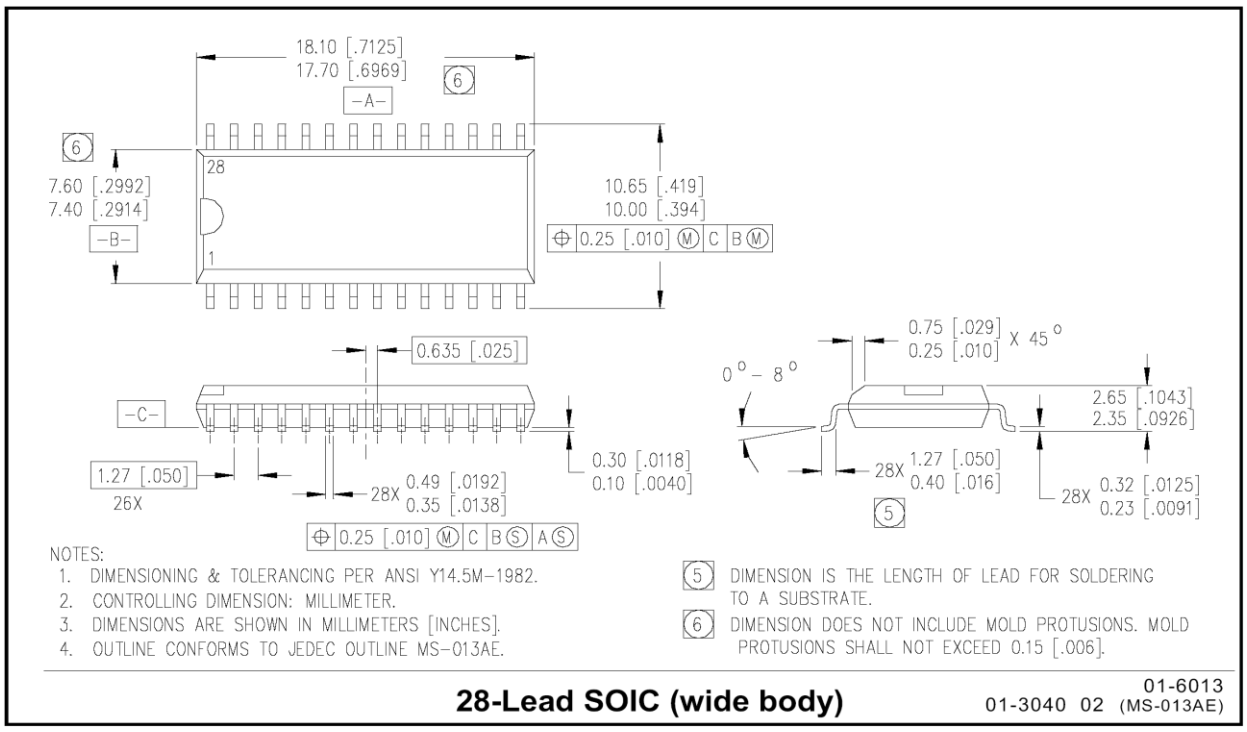


Fig. 39. Max -VS vs. Temperature

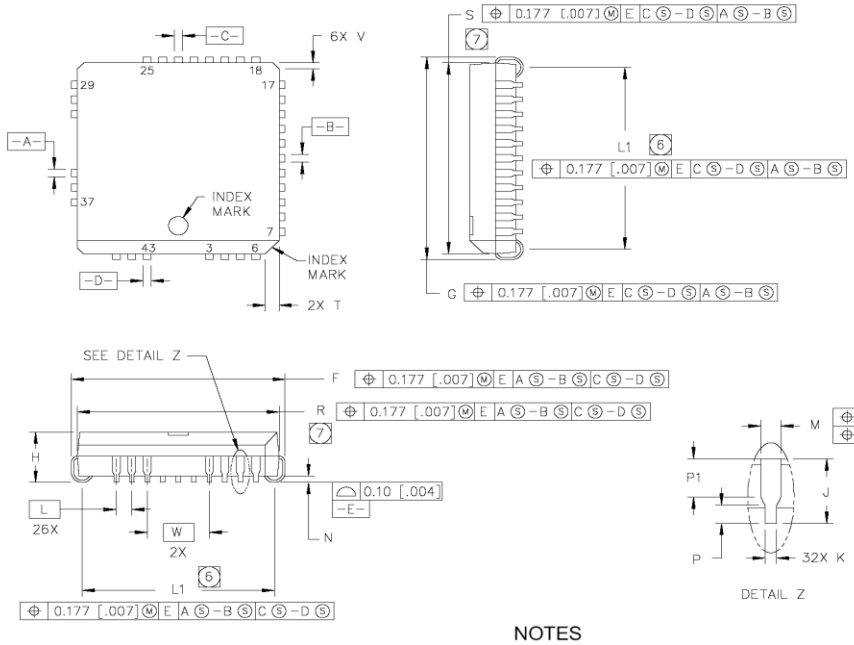
Case Outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body) 01-6013
01-3040 02 (MS-013AE)



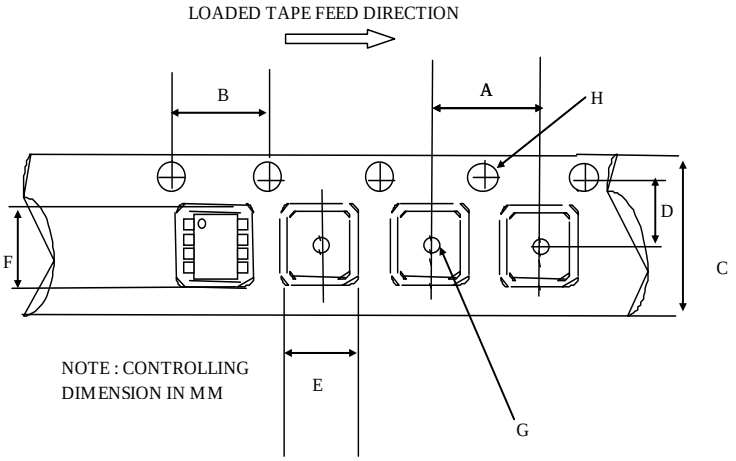
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.

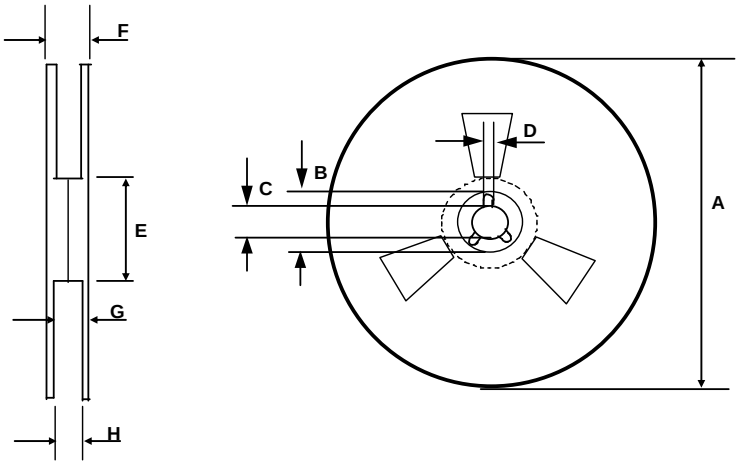
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads 01-6009 00
01-3004 02(mod.) (MS-018AC)



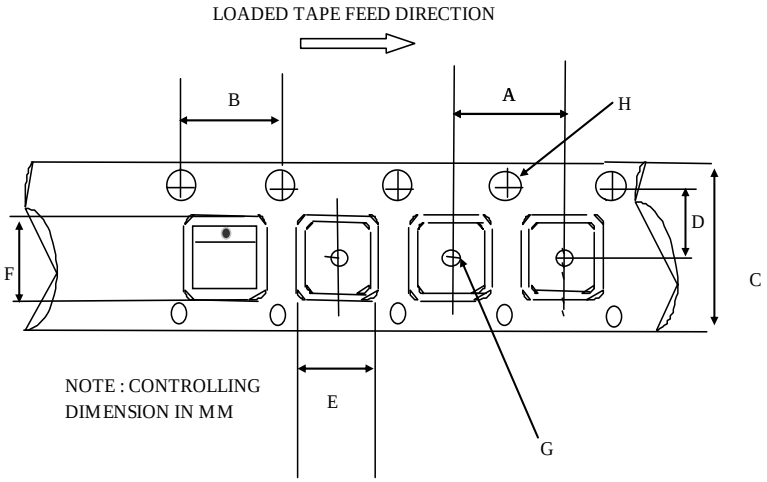
CARRIER TAPE DIMENSION FOR 28SOICW

	Metric		Imperial	
Code	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	18.20	18.40	0.716	0.724
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



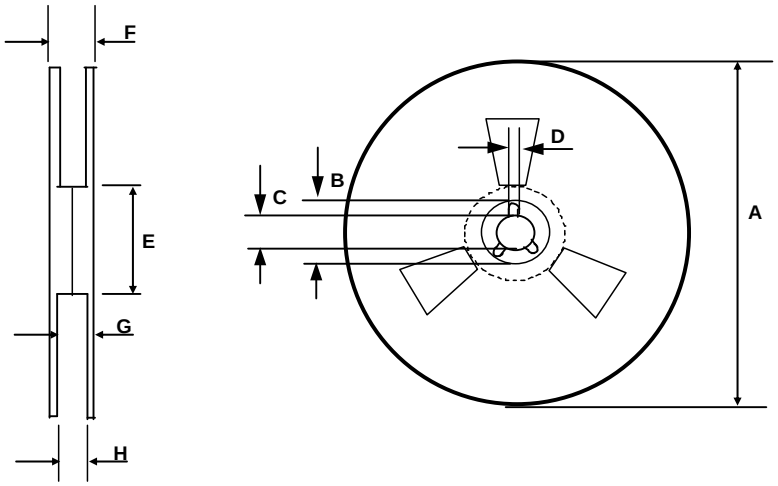
REEL DIMENSIONS FOR 28SOICW

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039



CARRIER TAPE DIMENSION FOR 44PLCC

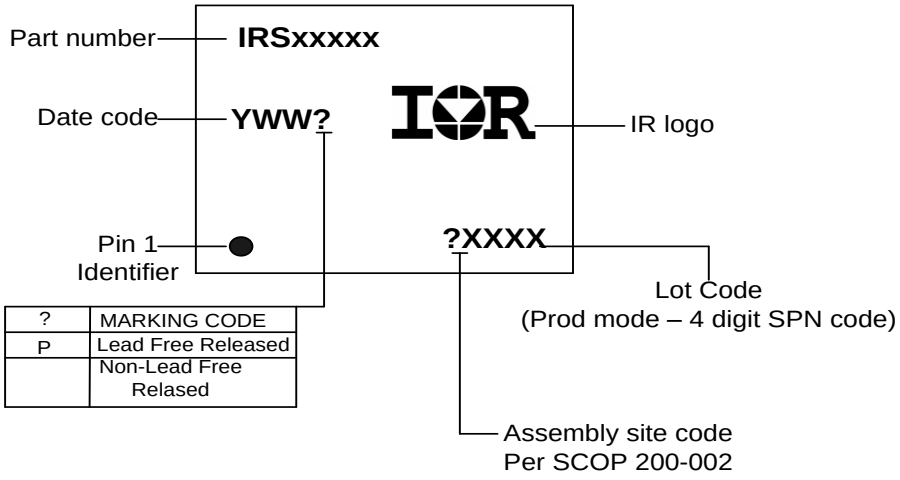
Code	Metric		Imperial	
	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 44PLCC

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

ORDER INFORMATION

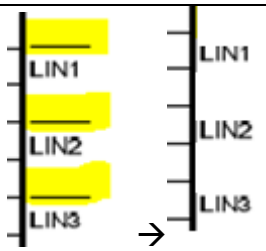
28-Lead SOIC IR21364SPbF
44-Lead PLCC IR21364JPbF

28-Lead SOIC Tape & Reel IR21364STRPbF
44-Lead PLCC Tape & Reel IR21364JTRPbF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

Change History

Revision	Date	Change comments
1.0	04/03/08	Included Qual Info, Replaced “Also available LEAD-FREE” statement in the front page with “RoHS Compliant”, removed typical spec limit for MT, MDT, & PM, added Tri-temp plots, and added disclaimer at end of the datasheet.
2.0	5/3/2016	 → in package drawing