SSC4S790

Description

SSC4S790 is a single channel high-side gate driver. The IC incorporates a floating drive circuit for a high-side power MOSFET, which can be used for a high-side gate driver such as a half-bridge converter or bridgeless PFC.

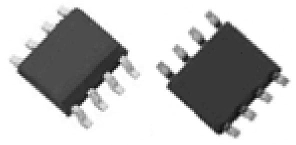
The IC is provided in the compact and low profile SOIC8 package.

Features

- Single Input and Output
- Breakdown Voltage of Floating Driver: 600 V
- 3.3 V Logic Signal Compatible
- CMOS Schmitt-trigger Input with Pull-down
- Output in Phase with Input
- Protections
  High-side Driver Undervoltage Lockout (UVLO): Auto-restart
  VCC Pin Overvoltage Protection (OVP): Latched shutdown
  Thermal Shutdown (TSD): Latched shutdown

Package

SOIC8



Not to scale

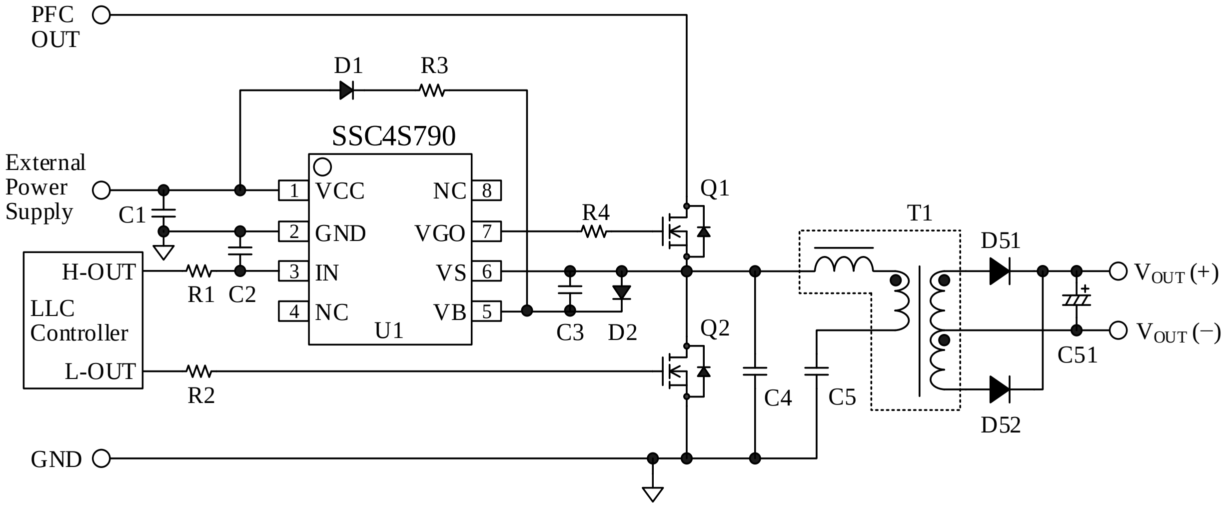
Specifications

- Power Supply Voltage, V_{CC}: 12 V to 18 V
- VGO Pin Peak Source Current: −300 mA
- VGO Pin Peak Sink Current: 550 mA

Applications

- White Goods
- Office Automation Equipment
- Audio Visual Equipment
- Industrial Equipment
- Other Switched Mode Power Supply (SMPS)

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless otherwise specified, T_A = 25 °C. Surge withstand capability (HBM) of the SSC4S790 is guaranteed up to 2000 V. Note that the following pins are guaranteed to withstand surges up to 1000 V: 5, 6, 7.

Parameter	Symbol	Conditions	Pins	Rating	Unit
VCC Pin Voltage	V_{CC}		1 − 2	−0.3 to 20	V
IN Pin Voltage	V_{IN}		3 − 2	−0.3 to 5	V
High-side Driver Control Voltage	V_{BS}	V_B−V_S	5 − 6	−0.3 to 20	V
VS Pin Voltage	V_S		6 − 2	−1 to 600	V
VGO Pin Voltage	V_{GO}		7 − 6	V_S − 0.3 to V_B + 0.3	V
Power Dissipation	P_D		—	0.69	W
Operating Ambient Temperature	T_{OP}		—	−40 to 85	°C
Storage Temperature	T_{STG}		—	−40 to 125	°C
Junction Temperature	T_J		—	150	°C

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C, V_{CC} = 17 V

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Start / Stop Operation							
Operation Start Voltage	$V_{CC(ON)}$		1 − 2	10.0	11.0	12.0	V
Operation Stop Voltage	$V_{CC(OFF)}$		1 − 2	7.4	8.3	9.2	V
Circuit Current in Operation	$I_{CC(ON)}$		1 − 2	—	0.52	1.1	mA
Circuit Current in Non-operation	$I_{CC(OFF)}$	V_{CC} = 9 V	1 − 2	—	0.25	0.60	mA
Input Side							
High Level Input Threshold Voltage	$V_{IN(H)}$		3 − 2	2.0	2.4	2.8	V
Low Level Input Threshold Voltage	$V_{IN(L)}$		3 − 2	0.6	1.0	1.4	V
IN Pin Bias Current	$I_{IN(B)}$	V_{IN} = 3.3 V	3 − 2	—	32	75	µA
High-side Driver							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		5 − 6	5.8	6.8	7.8	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		5 − 6	5.4	6.4	7.4	V
Output Side							
Turn-on Propagation Delay	t_{dLH}	See Figure 2-1	3 − 2 7 − 6	—	—	300	ns
Turn-off Propagation Delay	t_{dHL}	See Figure 2-1	3 − 2 7 − 6	—	—	300	ns
VGO Pin Source Current (Peak)	$I_{GO(SRC)}$	V_B = 17 V, V_{GO} = 0 V	7 − 6	—	−300	—	mA
VGO Pin Sink Current (Peak)	$I_{GO(SNK)}$	V_B = 17 V, V_{GO} = 17 V	7 − 6	—	550	—	mA
Protection							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		1 − 2	18.1	19.0	19.7	V
TSD Operating Temperature	$T_{J(TSD)}$		—	125	157	—	°C
Thermal Characteristic							
Junction-to-Air Thermal Resistance	θ_{J-A}		—	—	—	180	°C/W

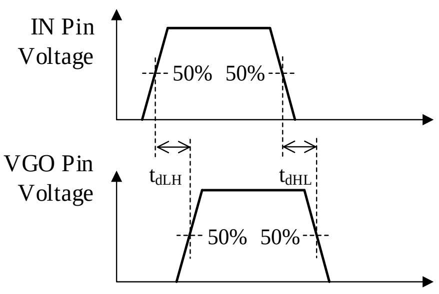
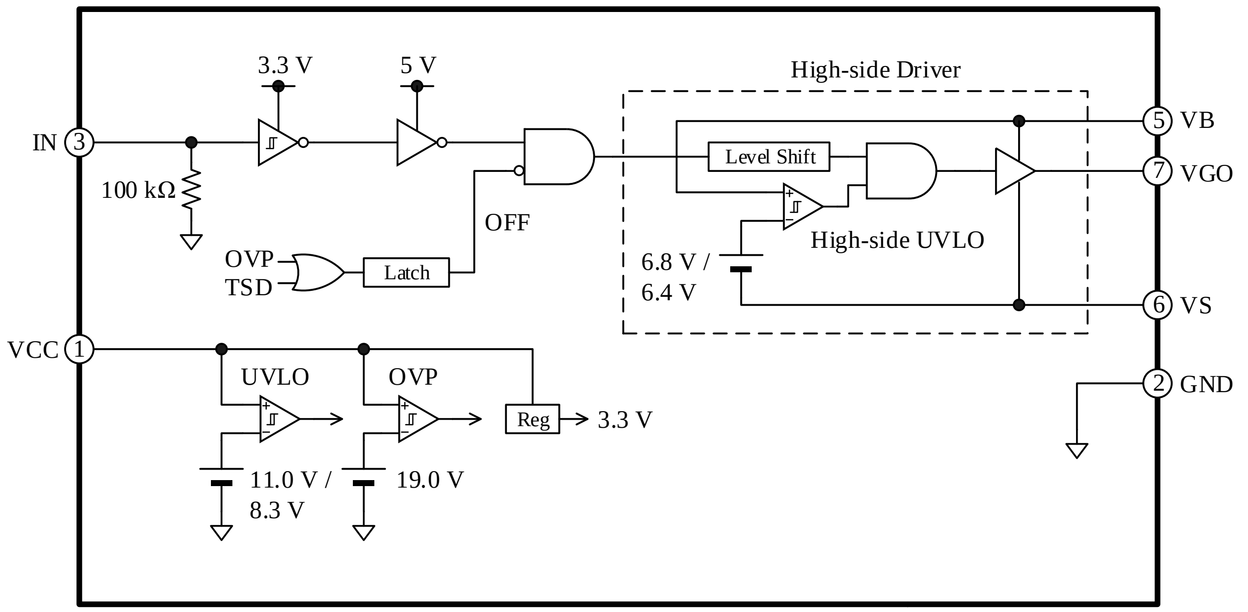
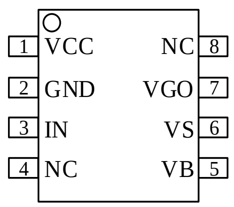


Figure 2-1. Input and Output Waveforms

3. Block Diagram



4. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	VCC	Logic power supply input with VCC pin OVP
2	GND	Ground
3	IN	Signal input
4	NC	No connection
5	VB	Power supply input for high-side gate drive with UVLO
6	VS	Floating ground of high-side driver
7	VGO	High-side gate drive output
8	NC	No connection

5. Typical Application

Figure 5-1 shows the half-bridge converter example using the SSC4S790.

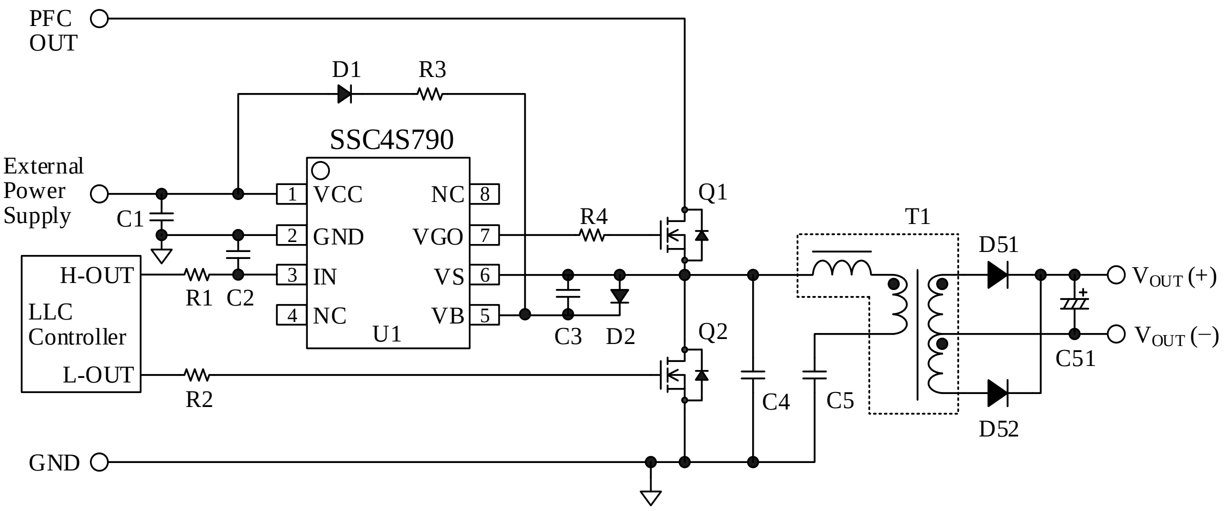
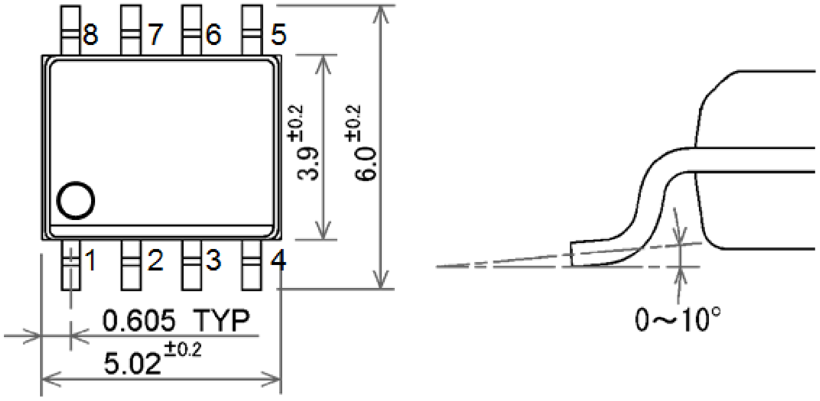
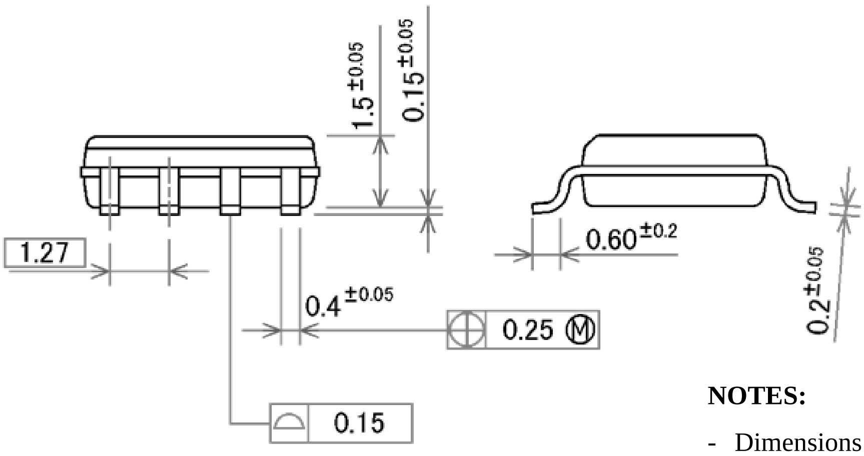


Figure 5-1. Half-bridge Converter Example Using SSC4S790

6. Physical Dimensions

- **SOIC8 Package**

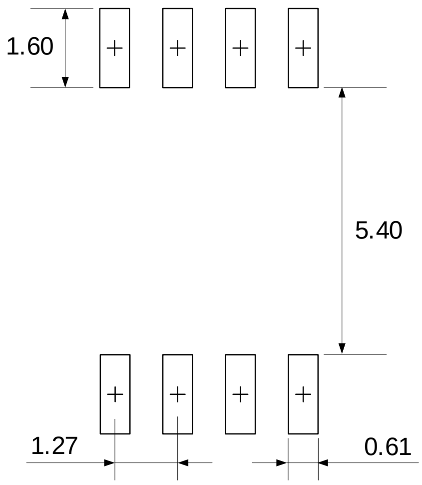




NOTES:

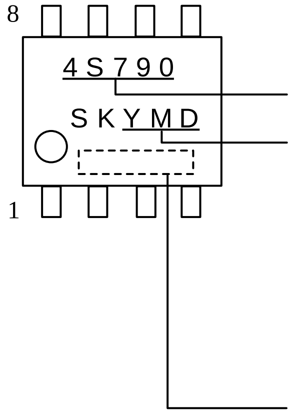
- Dimensions in millimeters
- Pb-free

- **SOIC8 Land Pattern Example**



Unit: mm

7. Marking Diagram



Part Number

Lot Number:
- Y is the last digit of the year of manufacture (0 to 9)
- M is the month of the year (1 to 9, O, N, or D)
- D is the period of days represented by:
  - 1: the first 10 days of the month (1st to 10th)
  - 2: the second 10 days of the month (11th to 20th)
  - 3: the last 10–11 days of the month (21st to 31st)

Control Number

8. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

8.1. Start / Stop Operation

Figure 8-1 shows the VCC pin peripheral circuit, Figure 8-2 shows the operational waveforms.

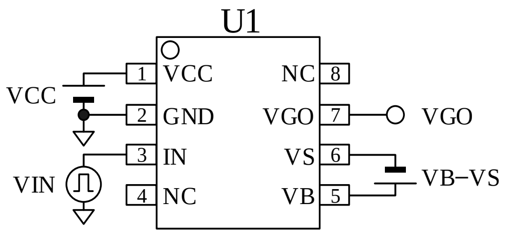


Figure 8-1. VCC Pin Peripheral Circuit

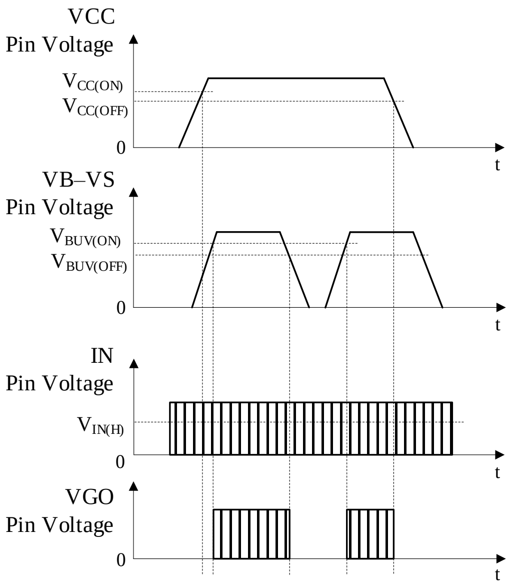


Figure 8-2. Operational Waveforms

This is the power supply pin for the built-in control circuit, and is connected to an external power supply. When the VCC pin voltage increases to $V_{CC(ON)}$ = 11.0 V, the control circuit starts operating. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.3 V or less, the control circuit stops operating by the VCC_UVLO (VCC Pin Undervoltage Lockout) (see Figure 8-3).

When the IC satisfies following conditions, the IC starts the switching operation according to the IN pin input signal (see Section 8.2.1):

- VCC pin voltage ≥ $V_{CC(ON)}$ = 11.0 V
- Voltage between VB and VS pins ≥ $V_{BUV(ON)}$= 6.8 V

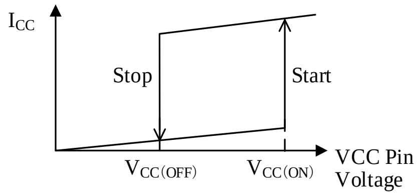


Figure 8-3. V_{CC} vs. I_{CC}

8.2. Pin Descriptions

8.2.1. IN

This is the signal input pin compatible with 3.3 V logic signal.

When the IN pin voltage increases to $V_{IN(H)}$ = 2.4 V or more, the VGO pin outputs "H". When the IN pin voltage decreases to $V_{IN(L)}$ = 1.0 V or less, the VGO pin outputs "L".

The IN pin is connected to the 100 kΩ pull-down resistor internally (see Section 3).

8.2.2. VB and VS

The VB pin is the input of the high-side floating power supply, whereas the VS pin is the ground of the high-side floating power supply. The SSC4S790 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins (see Section 8.3).

Figure 8-4 is a schematic diagram of the bootstrap circuit that drives the high-side power MOSFET (Q1).

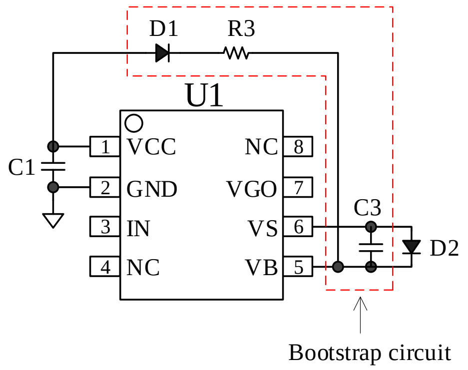


Figure 8-4. Bootstrap Circuit

In the condition where the high-side power MOSFET is turned off and the low-side power MOSFET (Q2) is turned on, the VS pin voltage has almost the same potential as the ground. Then, C3 is charged with the VCC pin. When the voltage between the VB and VS pins (hereafter "VB−VS voltage") increases to $V_{BUV(ON)}$ = 6.8 V or more, the internal high-side driver starts operating. When VB−VS voltage decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the internal high-side driver stops operating (i.e., VB_UVLO). The VB_UVLO protects the IC in case both ends of C3 and D2 are shorted. The bootstrap circuit components must meet the following:

- **D1**
  D1 should be a fast recovery diode with a short recovery time and a low reverse current. When the maximum supply input voltage is specified at 265 VAC, it is recommended to use a fast recovery diode with V_{RM} = 600 V.

- **C1, C3, R3**
  The values of C1, C3, and R3 are determined by the following parameters: the total amount of gate charges of the external power MOSFETs, Qg; the amount of a voltage dip between the VB and VS pins during operation at the lowest oscillation frequency. C1, C3, and R3 should be adjusted according to voltages measured by a high-voltage differential probe so that VB–VS voltage exceeds $V_{BUV(ON)}$ = 6.8 V. C1 and C3 should be film or ceramic capacitors with a low ESR and a low leakage current. The reference value of C1 is 0.47μF to 1 μF. C3 should have a capacitance of 0.047 μF or more. R3 should have a resistance of 1 Ω to 10 Ω.

- **D2**
  D2 is used for protecting the VS pin from having a negative potential. D2 should be a Schottky diode with a low forward voltage so that VB–VS voltage does not fall below −0.3 V of its absolute maximum rating.

8.2.3. VGO

The VGO pin is gate drive output for the external power MOSFET. This peak source and sink currents are −300 mA and 550 mA, respectively.

To increase a falling speed of the gate at power MOSFET turn-off, connect the diode D_S as shown in Figure 8-5. R_A and D_S should be adjusted based on the operation performance checked with an actual board, including a loss in the power MOSFET, gate waveform (e.g., ringing due to pattern layout), and EMI noise. To prevent malfunction caused by steep dv/dt at power MOSFET turn-off, connect R_{GS}, of about 10 kΩ to 100 kΩ, between the gate and source of the power MOSFET with a minimal length of traces.

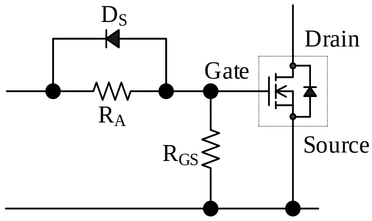


Figure 8-5. Power MOSFET Peripheral Circuit

8.3. High-side Driver Undervoltage Lockout

The SSC4S790 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins.
When the voltage between the VB and VS pins (i.e., "VB–VS voltage") increases to $V_{BUV(ON)}$ = 6.8 V or more, the internal high-side driver starts operating. When the VB–VS voltage decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the internal high-side driver stops operating. The VB_UVLO protects the IC in case both ends of the capacitor C3 for bootstrap circuit and the protective diode D2 are shorted.

8.4. VCC Pin Overvoltage Protection (OVP)

When the voltage between the VCC and GND pins increases to $V_{CC(OVP)}$ = 19.0 V or more, the VCC pin overvoltage protection (VCC_OVP) is activated. Then, the IC stops switching operation at the latched state. To release the latched state, decrease the VCC pin voltage to $V_{CC(OFF)}$ = 8.3 V or less.

The VCC pin input voltage must be set less than the its absolute maximum rating of 20 V.

8.5. Thermal Shutdown (TSD)

When the control circuit temperature reaches $T_{J(TSD)}$ = 157 °C, the thermal shutdown (TSD) is activated. Then, the IC stops switching operation at the latched state. To release the latched state, decrease the VCC pin voltage to $V_{CC(OFF)}$ = 8.3 V or less.

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