ISL89160, ISL89161, ISL89162

High Speed, Dual Channel, 6A, 4.5 to 16V_{OUT}, Power MOSFET Drivers

FN7719
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The ISL89160, ISL89161, and ISL89162 are high-speed, 6A, dual channel MOSFET drivers. These parts are identical to the ISL89163, ISL89164, ISL89165 drivers but without the enable inputs for each channel.

Two input logic thresholds are available: 3.3V (CMOS and TTL compatible) and 5.0V (CMOS).

Precision thresholds on all logic inputs allow the use of external RC circuits to generate accurate and stable time delays on both inputs, INA and INB. This capability is very useful for dead time control.

At high switching frequencies, these MOSFET drivers use very little bias current. Separate, non-overlapping drive circuits are used to drive each CMOS output FET to prevent shoot-thru currents in the output stage.

The start-up sequence is design to prevent unexpected glitches when V_{DD} is being turned on or turned off. When V_{DD} < ~1V, an internal 10kΩ resistor between the output and ground helps to keep the output voltage low. When ~1V < V_{DD} < UV, both outputs are driven low with very low resistance and the logic inputs are ignored. This insures that the driven FETs are off. When V_{DD} > UVLO, and after a short delay, the outputs now respond to the logic inputs.

Features

- Dual output, 6A peak currents, can be paralleled
- Typical ON-resistance <1Ω
- Specified Miller plateau drive currents
- Very low thermal impedance (θ_{JC} = 3°C/W)
- Hysteretic input logic levels for 3.3V CMOS, 5V CMOS, and TTL
- Precision threshold inputs for time delays with external RC components
- 20ns rise and fall time driving a 10nF load.
- NC pins may be connected to ground or VDD to ease PCB layout difficulties.

Applications

- Synchronous Rectifier (SR) driver
- Switch mode power supplies
- Motor drives, class D amplifiers, UPS, inverters
- Pulse transformer driver
- Clock/line driver

Related Literature

- AN1603 “ISL6752/54EVAL1Z ZVS DC/DC Power Supply with Synchronous Rectifiers User Guide”

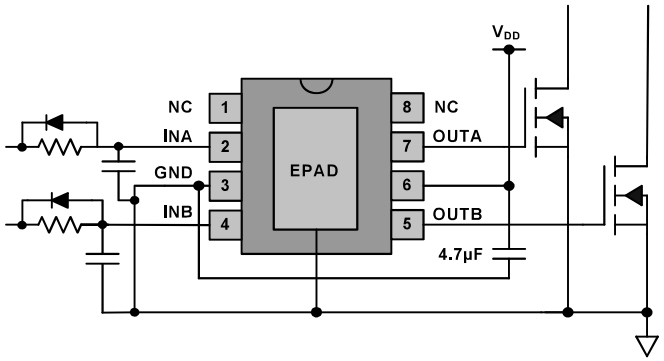


FIGURE 1. TYPICAL APPLICATION

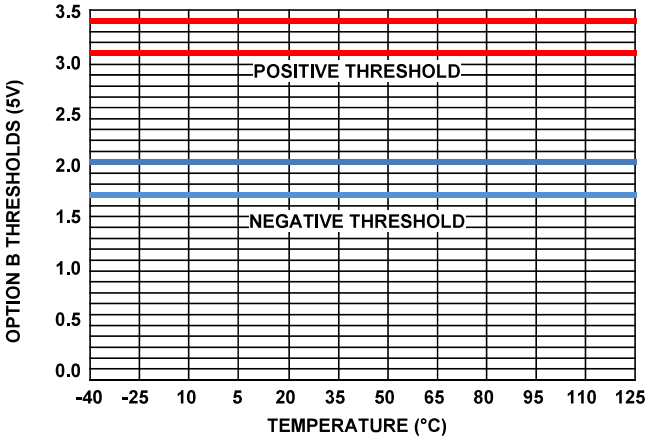
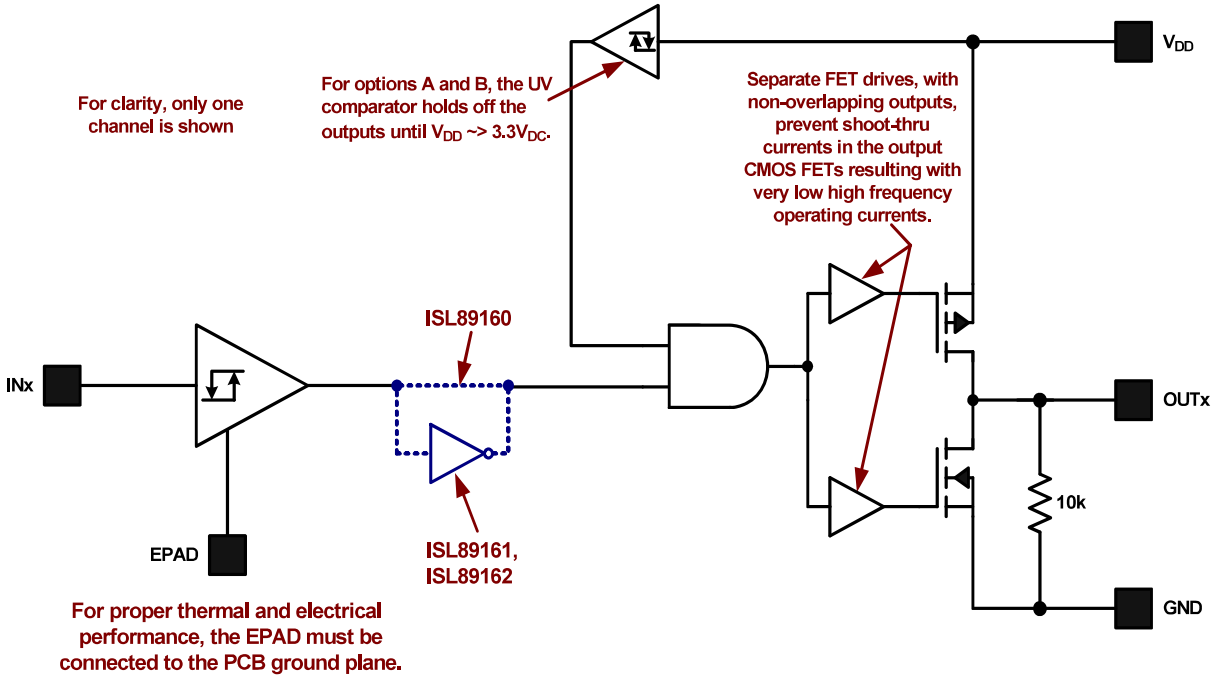


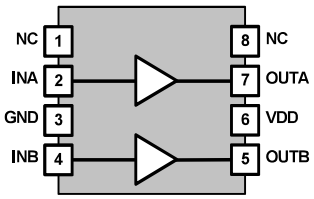
FIGURE 2. TEMPERATURE STABLE LOGIC THRESHOLDS

Block Diagram

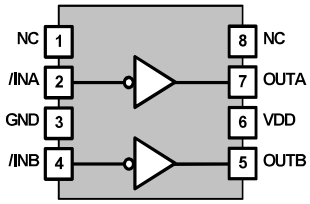


Pin Configurations

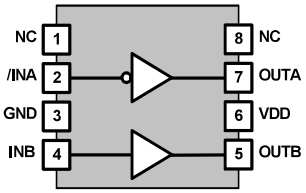
ISL89160FR, ISL89160FB
(8 LD TDFN, EPSOIC)
TOP VIEW



ISL89161FR, ISL89161FB
(8 LD TDFN, EPSOIC)
TOP VIEW



ISL89162FR, ISL89162FB
(8 LD TDFN, EPSOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 8	NC	No Connect. This pin may be left open or connected to 0V or VDD
2	INA or /INA	Channel A input, 0V to VDD
3	GND	Power Ground, 0V
4	INB or /INB	Channel B enable, 0V to VDD
5	OUTB	Channel B output
6	VDD	Power input, 4.5V to 16V
7	OUTA	Channel A output, 0V to VDD
	EPAD	Power Ground, 0V

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	INPUT CONFIGURATION	INPUT LOGIC	PACKAGE (Pb-Free)	PKG. DWG. #
ISL89160FRTAZ	160A	-40 to +125	non-inverting	3.3VDC	8 Ld 3x3 TDFN	L8.3x3I
ISL89161FRTAZ	161A	-40 to +125	inverting		8 Ld 3x3 TDFN	L8.3x3I
ISL89162FRTAZ	162A	-40 to +125	inverting + non-inverting		8 Ld 3x3 TDFN	L8.3x3I
ISL89160FBEAZ	89160 FBEAZ	-40 to +125	non-inverting		8 Ld EPSOIC	M8.15D
ISL89161FBEAZ	89161 FBEAZ	-40 to +125	inverting		8 Ld EPSOIC	M8.15D
ISL89162FBEAZ	89162 FBEAZ	-40 to +125	inverting + non-inverting		8 Ld EPSOIC	M8.15D
ISL89160FRTBZ	160B	-40 to +125	non-inverting	5.0VDC	8 Ld 3x3 TDFN	L8.3x3I
ISL89161FRTBZ	161B	-40 to +125	inverting		8 Ld 3x3 TDFN	L8.3x3I
ISL89162FRTBZ	162B	-40 to +125	inverting + non-inverting		8 Ld 3x3 TDFN	L8.3x3I
ISL89160FBEBZ	89160 FBEBZ	-40 to +125	non-inverting		8 Ld EPSOIC	M8.15D
ISL89161FBEBZ	89161 FBEBZ	-40 to +125	inverting		8 Ld EPSOIC	M8.15D
ISL89162FBEBZ	89162 FBEBZ	-40 to +125	inverting + non-inverting		8 Ld EPSOIC	M8.15D

NOTES:

1. Add "-T*", suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL89160, ISL89161, ISL89162. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings

Supply Voltage, V_{DD} Relative to GND . . . . . -0.3V to 18V
Logic Inputs (INA, INB) . . . . . GND - 0.3V to V_{DD} + 0.3V
Outputs (OUTA, OUTB) . . . . . GND - 0.3V to V_{DD} + 0.3V
Average Output Current (Note 6) 150mA
ESD Ratings
Human Body Model Class 2 (Tested per JESD22-A114E) 2000V
Machine Model Class B (Tested per JESD22-A115-A) 200V
Charged Device Model Class IV 1000V
Latch-Up (Tested per JESD-78B; Class 2, Level A) Output Current. . . 500mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package (Notes 4, 5)	44	3
8 Ld EPSOIC Package (Notes 4, 5)	42	3

Max Power Dissipation at +25°C in Free Air 2.27W
Max Power Dissipation at +25°C with Copper Plane 33.3W
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temp Range . . . . . -40°C to +125°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Maximum Recommended Operating Conditions

Junction Temperature . . . . . -40°C to +125°C
Supply Voltage, V_{DD} Relative to GND . . . . . 4.5V to 16V
Logic Inputs (INA, INB) . . . . . 0V to V_{DD}
Outputs (OUTA, OUTB) . . . . . 0V to V_{DD}

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. The average output current, when driving a power MOSFET or similar capacitive load, is the average of the rectified output current. The peak output currents of this driver are self limiting by transconductance or $r_{DS(ON)}$ and do not required any external components to minimize the peaks. If the output is driving a non-capacitive load, such as an LED, maximum output current must be limited by external means to less than the specified absolute maximum.

DC Electrical Specifications

V_{DD} = 12V, GND = 0V, No load on OUTA or OUTB, unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C.**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN (Note 7)	MAX (Note 7)	
POWER SUPPLY								
Voltage Range	V_{DD}		-	-	-	**4.5**	**16**	V
V_{DD} Quiescent Current	I_{DD}	INx = GND	-	5	-	-	-	mA
		INA = INB = 1MHz, square wave	-	25		-	-	mA
UnderVoltage								
V_{DD} Undervoltage Lock-out (Note 9, Figure 9)	V_{UV}	INA = INB = True (Note 10)	-	3.3	-	-	-	V
Hysteresis			-	~25	-	-	-	mV
INPUTs (Note 11)								
Input Range for INA, INB	V_{IN}		-	-	-	**GND**	**V_{DD}**	V
Logic 0 Threshold for INA, INB (Note 9)	V_{IL}	Option A, nominally 37% x 3.3V	-	1.22	-	**1.12**	**1.32**	V
		Option B, nominally 37% x 5.0V	-	1.85	-	**1.70**	**2.00**	V
Logic 1 Threshold for INA, INB (Note 9)	V_{IH}	Option A, nominally 63% x 3.3V	-	2.08	-	**1.98**	**2.18**	V
		Option B, nominally 63% x 5.0V	-	3.15	-	**3.00**	**3.30**	V
Input Capacitance of INA, INB (Note 8)	C_{IN}		-	2	-	-	-	pF

DC Electrical Specifications

V_{DD} = 12V, GND = 0V, No load on OUTA or OUTB, unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C. (Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN (Note 7)	MAX (Note 7)	
Input Bias Current for INA, INB	I_{IN}	GND < V_{IN} < V_{DD}	-	-	-	**-10**	**+10**	µA
OUTPUTS								
High Level Output Voltage	V_{OHA} V_{OHB}		-	-	-	**V_{DD} - 0.1**	**V_{DD}**	V
Low Level Output Voltage	V_{OLA} V_{OLB}		-	-	-	**GND**	**GND + 0.1**	V
Peak Output Source Current	I_O	V_O (initial) = 0V, C_{LOAD} = 10nF	-	-6	-	-	-	A
Peak Output Sink Current	I_O	V_O (initial) = 12V, C_{LOAD} = 10nF	-	+6	-	-	-	A

NOTES:

7. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.
8. This parameter is taken from the simulation models for the input FET. The actual capacitance on this input will be dominated by the PCB parasitic capacitance.
9. A 400µs delay further inhibits the release of the output state when the UV positive going threshold is crossed. See Figure 9
10. The true state of a specific part number is defined by the input logic symbol.
11. The true state input voltage for the non-inverted inputs is greater than the Logic 1 threshold voltage. The true state input voltage for the inverted inputs is less than the logic 0 threshold voltage.

AC Electrical Specifications

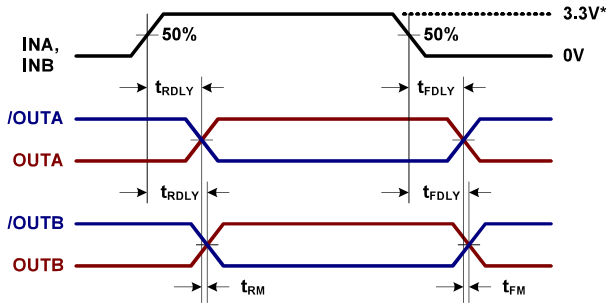
V_{DD} = 12V, GND = 0V, No Load on OUTA or OUTB, Unless Otherwise Specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C.**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Output Rise Time (see Figure 4)	t_R	C_{LOAD} = 10nF, 10% to 90%	-	20	-	-	**40**	ns
Output Fall Time (see Figure 4)	t_F	C_{LOAD} = 10nF, 90% to 10%	-	20	-	-	**40**	ns
Output Rising Edge Propagation Delay for Non-Inverting Inputs (see Figure 3)	t_{RDLYn}	No load	-	25	-	-	**50**	ns
Output Rising Edge Propagation Delay with Inverting Inputs (see Figure 3)	t_{RDLYi}	No load	-	25	-	-	**50**	ns
Output Falling Edge Propagation Delay with Non-Inverting Inputs (see Figure 3)	t_{FDLYn}	No load	-	25	-	-	**50**	ns
Output Falling Edge Propagation Delay with Inverting Inputs (see Figure 3)	t_{FDLYi}	No load	-	25	-	-	**50**	ns
Rising Propagation Matching (see Figure 3)	t_{RM}	No load	-	<1	-	-	-	ns
Falling Propagation Matching (see Figure 3)	t_{FM}	No load	-	<1	-	-	-	ns
Miller Plateau Sink Current (See Test Circuit Figure 5)	$-I_{MP}$	V_{DD} = 10V, V_{MILLER} = 5V	-	6	-	-	-	A
	$-I_{MP}$	V_{DD} = 10V, V_{MILLER} = 3V	-	4.7	-	-	-	A
	$-I_{MP}$	V_{DD} = 10V, V_{MILLER} = 2V	-	3.7	-	-	-	A

AC Electrical Specifications V_{DD} = 12V, GND = 0V, No Load on OUTA or OUTB, Unless Otherwise Specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C. (Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Miller Plateau Source Current (See Test Circuit Figure 6)	I_{MP}	V_{DD} = 10V, V_{MILLER} = 5V	-	5.2	-	-	-	A
	I_{MP}	V_{DD} = 10V, V_{MILLER} = 3V	-	5.8	-	-	-	A
	I_{MP}	V_{DD} = 10V, V_{MILLER} = 2V	-	6.9	-	-	-	A

Test Waveforms and Circuits



* Logic levels: A option = 3.3V, B option = 5.0V

FIGURE 3. PROP DELAYS AND MATCHING

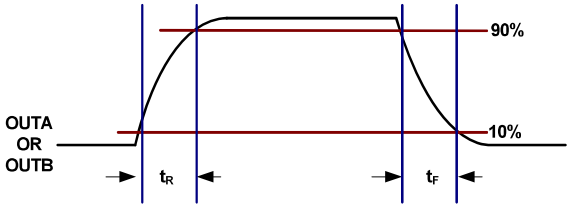


FIGURE 4. RISE/FALL TIMES

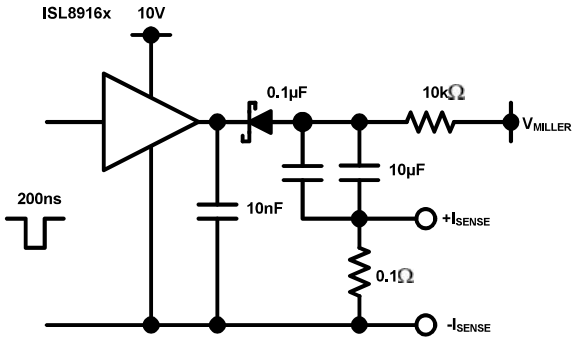


FIGURE 5. MILLER PLATEAU SINK CURRENT TEST CIRCUIT

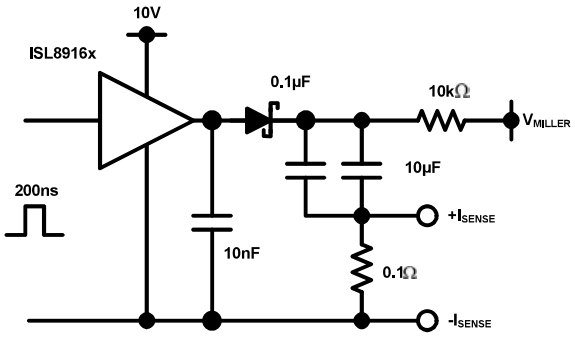


FIGURE 6. MILLER PLATEAU SOURCE CURRENT TEST CIRCUIT

Test Waveforms and Circuits (Continued)

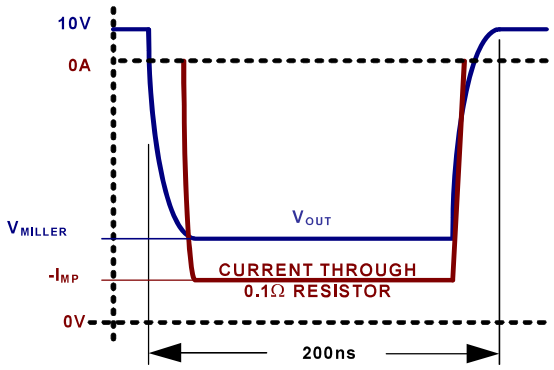


FIGURE 7. MILLER PLATEAU SINK CURRENT

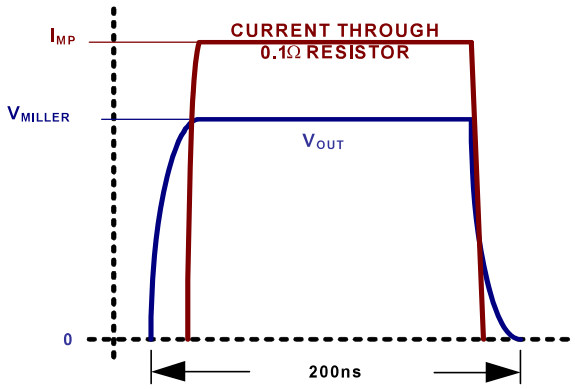


FIGURE 8. MILLER PLATEAU SOURCE CURRENT

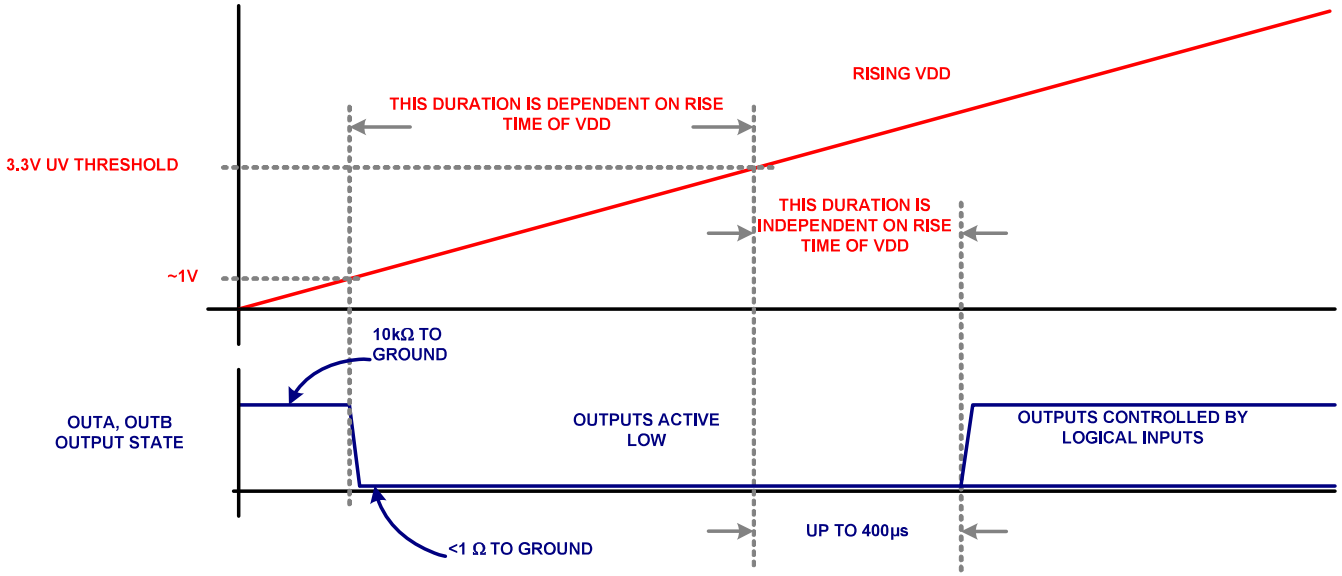


FIGURE 9. START-UP SEQUENCE

Typical Performance Curves

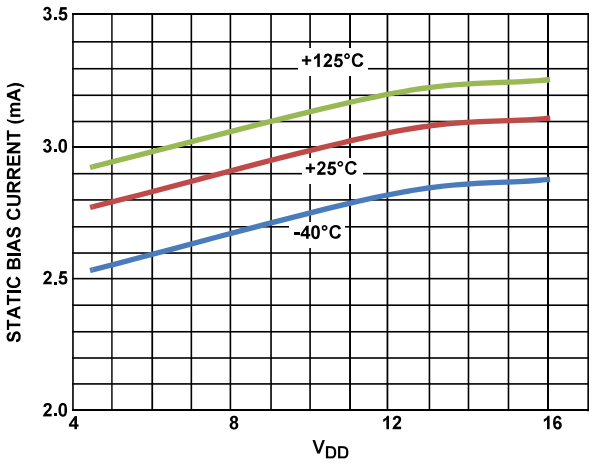


FIGURE 10. I_{DD} vs V_{DD} (STATIC)

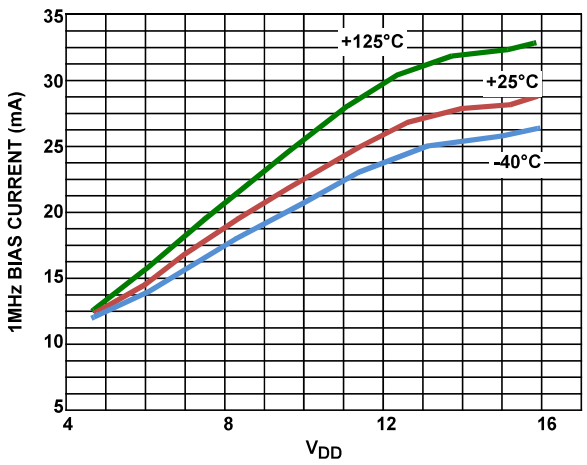


FIGURE 11. I_{DD} vs V_{DD} (1MHz)

Typical Performance Curves (Continued)

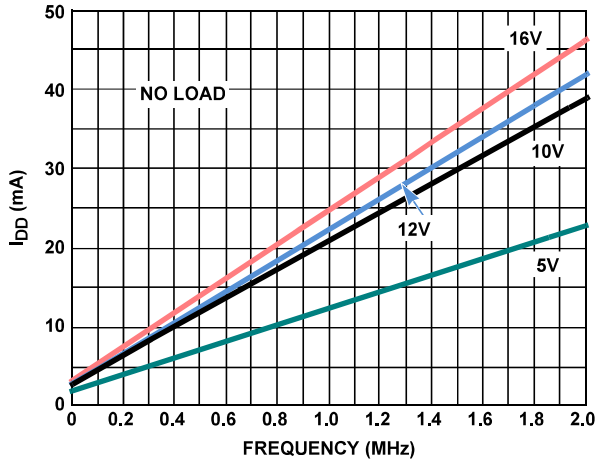


FIGURE 12. I_{DD} vs FREQUENCY (+25°C)

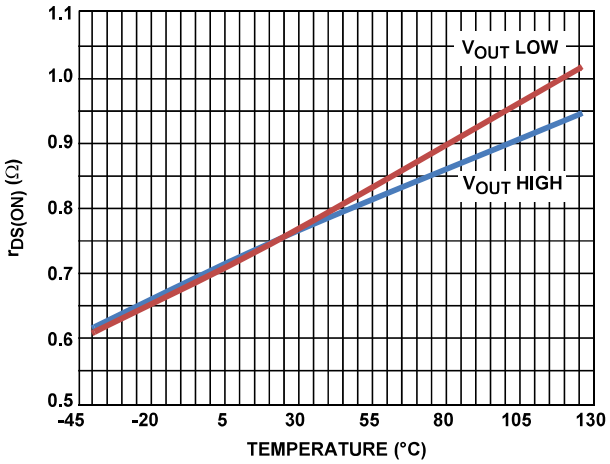


FIGURE 13. $r_{DS(ON)}$ vs TEMPERATURE

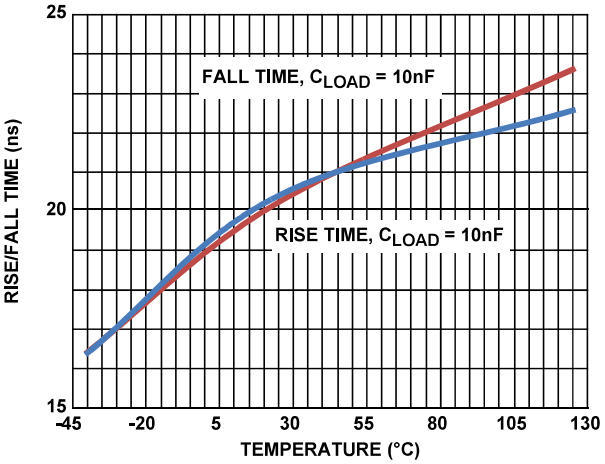


FIGURE 14. OUTPUT RISE/FALL TIME

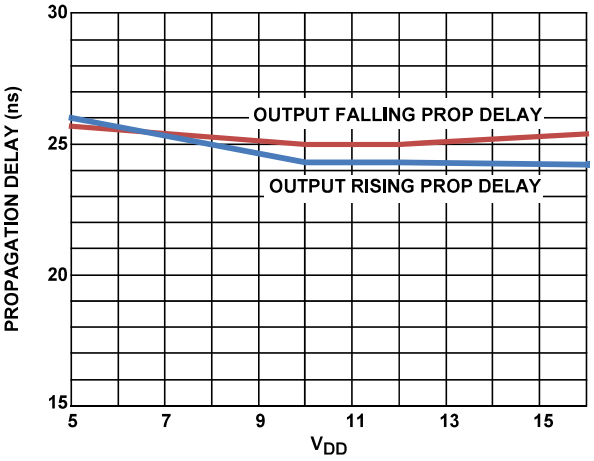


FIGURE 15. PROPAGATION DELAY vs V_{DD}

Functional Description

Overview

The ISL89160, ISL89161, ISL89162 drivers incorporate several features including precision input logic thresholds, undervoltage lock-out, and fast rising high output drive currents.

The precision input thresholds facilitate the use of an external RC network to delay the rising or falling propagation of the driver output. This is a useful feature to create dead times for bridge applications to prevent shoot through.

The fast rising (or falling) output drive currents of the ISL89160, ISL89161, ISL89162 minimize the turn-on (off) delays due to the input capacitance of the driven FET. The switching transition period at the Miller plateau is also minimized by high drive currents even at these lower output voltages. (See the specified Miller plateau currents in “AC Electrical Specifications” on page 5).

The start-up sequence is designed to prevent unexpected glitches when V_{DD} is being turned on or turned off. When V_{DD} < ~1V, an internal 10kΩ resistor connected between the output and ground, help to keep the gate voltage close to ground. When ~1V < V_{DD} < UV, both outputs are driven low while ignoring the logic inputs. This low state has the same current sinking capacity as during normal operation. This insures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates via the Miller capacitance. When V_{DD} > UVLO, and after a 400µs delay, the outputs now respond to the logic inputs. See Figure 9 for complete details.

For the negative transition of V_{DD} through the UV lockout voltage, the outputs are active low when V_{DD} < ~3.2V_{DC} regardless of the input logic states.

Application Information

Precision Thresholds for Time Delays

For input logic voltage option A, the nominal input negative transition threshold is 1.22V and the positive transition threshold is 2.08V (37% and 63% of 3.3V) Likewise, for input logic option B, the nominal input negative transition threshold is 1.85V and the positive transition threshold is 3.15V (37% and 63% of 4.0V).

In Figure 16, R_{del} and C_{del} delay the rising edge of the input signal. For the falling edge of the input signal, the diode shorts out the resistor resulting in a minimal falling edge delay. If the diode polarity is reversed, the falling edge is delayed and the rising delay is minimal.

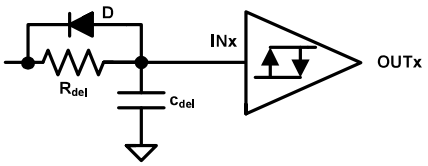


FIGURE 16. DELAY USING RCD NETWORK

The 37% and 63% thresholds were chosen to simplify the calculations for the desired time delays. When using an RC circuit to generate a time delay, the delay is simply T (secs) = R (ohms) x C (farads). Please note that this equation only applies if the input logic voltage amplitude is 3.3V. If the logic high amplitude is higher than 3.3V, the equations in Equation 1 can be used for more precise delay calculations.

$V_H = 5V$ High level of the logic signal into the RC

$V_{THRESH} = 63\% \times 3.3V$ Positive going threshold

$V_L = 0.1V$ Low level of the logic signal into the RC

$R_{del} = 100\Omega$ Timing values

$C_{del} = 1nF$

$$t_{del} = -R_{del}C_{del} \times LN\left(\frac{V_L - V_{THRESH}}{V_H - V_L} + 1\right)$$

$t_{del} = 51.731ns$ Nominal delay time (EQ. 1)

In this example, the high input logic voltage is 5V, the positive threshold is 63% of 3.3V and the low level input logic is 0.1V. **Note the rising edge propagation delay of the driver must be added to this value.**

The minimum recommended value of C is 100pF. The parasitic capacitance of the PCB and any attached scope probes will introduce significant delay errors if smaller values are used. Larger values of C will further minimize errors.

Acceptable values of R are primarily effected by the source resistance of the logic inputs. Generally, 100Ω resistors or larger are usable. A practical maximum value, limited by contamination on the PCB, is 1MΩ

Paralleling Outputs to Double the Peak Drive Currents

The typical propagation matching of the ISL89160 and ISL89161 is less than 1ns. The matching is so precise that carefully matched and calibrated scopes probes and scope channels must be used to make this measurement. Because of this excellent performance, these driver outputs can be safely paralleled to double the current drive capacity. It is important that the INA and INB inputs be connected together on the PCB with the shortest possible trace. This is also required of OUTA and OUTB. Note that the ISL89162 cannot be paralleled because of the complementary logic.

Power Dissipation of the Driver

The power dissipation of the ISL89160, ISL89161, ISL89162 is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation but is usually not significant as compared to the gate charge losses.

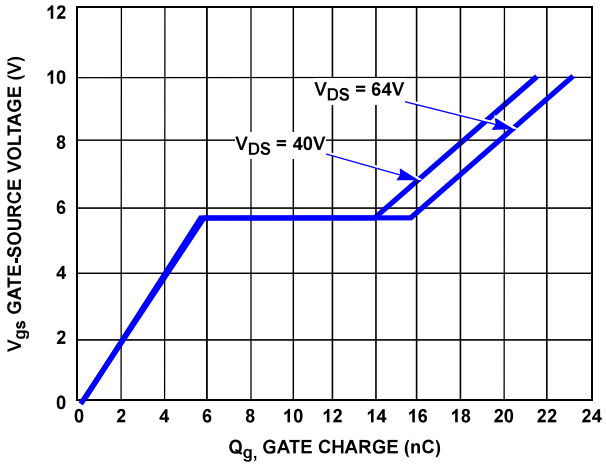


FIGURE 17. MOSFET GATE CHARGE vs GATE VOLTAGE

Figure 17 illustrates how the gate charge varies with the gate voltage in a typical power MOSFET. In this example, the total gate charge for V_{gs} = 10V is 21.5nC when V_{DS} = 40V. This is the charge that a driver must source to turn-on the MOSFET and must sink to turn-off the MOSFET.

Equation 2 shows calculating the power dissipation of the driver:

$$P_D = 2 \bullet Q_c \bullet freq \bullet V_{GS} \bullet \frac{R_{gate}}{R_{gate} + r_{DS(ON)}} + I_{DD}(freq) \bullet V_{DD}$$

(EQ. 2)

where:

freq = Switching frequency,

$V_{GS} = V_{DD}$ bias of the ISL89160, ISL89161, ISL89162

Q_c = Gate charge for V_{GS}

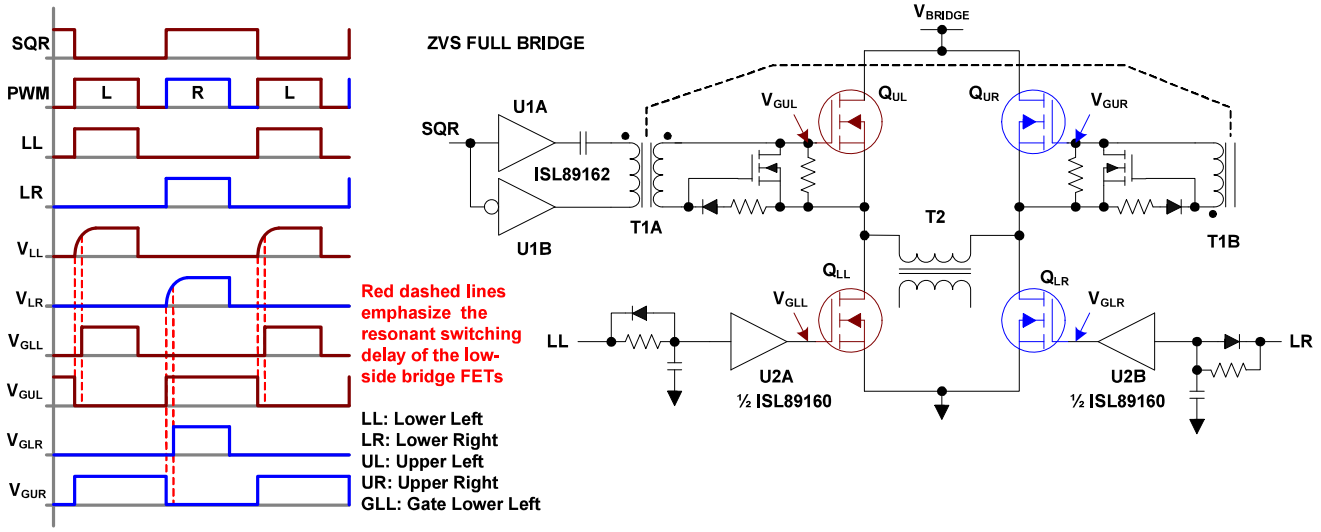
I_{DD}(freq) = Bias current at the switching frequency (see Figure 10)

$r_{DS(ON)}$ = ON-resistance of the driver

R_{gate} = External gate resistance (if any).

Note that the gate power dissipation is proportionally shared with the external gate resistor and the output $r_{DS(ON)}$. When sizing an external gate resistor, do not overlook the power dissipated by this resistor.

Typical Application Circuit



This is an example of how the ISL89160, ISL89161, ISL89162, MOSFET drivers can be applied in a zero voltage switching full bridge. Two main signals are required: a 50% duty cycle square wave (SQR) and a PWM signal synchronized to the edges of the SQR input. An ISL89162 is used to drive T1 with alternating half cycles driving Q_{UL} and Q_{UR}. An ISL89160 is used to drive Q_{LL} and Q_{LR} also with alternating half cycles. Unlike the two high-side bridge FETs, the two low side bridge FETs are turned on with a rising edge delay. The delay is setup by the RCD network on the inputs to the ISL89160. The duration of the delay is chosen to turn on the low-side FETs when the voltage on their respective drains is at the resonant valley. For a complete description of the ZVS topology, refer to AN1603 “ISL6752_54 Evaluation Board Application Note”.

General PCB Layout Guidelines

The AC performance of the ISL89160, ISL89161, ISL89162 depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt will induce currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. The noise, magnetically induced on a 10k resistor, is 10x larger than the noise on a 1k resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the VDD and GND leads. To be effective, these caps must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits especially on OUTA and OUTB. If an external gate resistor is unacceptable, then the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL89160, ISL89161, ISL89162.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. This will inject di/dt currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic caps, power resistors, etc.) will have internal parasitic inductance which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components especially parasitic inductance.

General EPAD Heatsinking Considerations

The thermal pad is electrically connected to the GND supply through the IC substrate. The epad of the ISL89160, ISL89161, ISL89162 has two main functions: to provide a quiet GND for the input threshold comparators and to provide heat sinking for the IC. The EPAD must be connected to a ground plane and no switching currents from the driven FET should pass through the ground plane under the IC.

Figure 18 is a PCB layout example of how to use vias to remove heat from the IC through the epad.

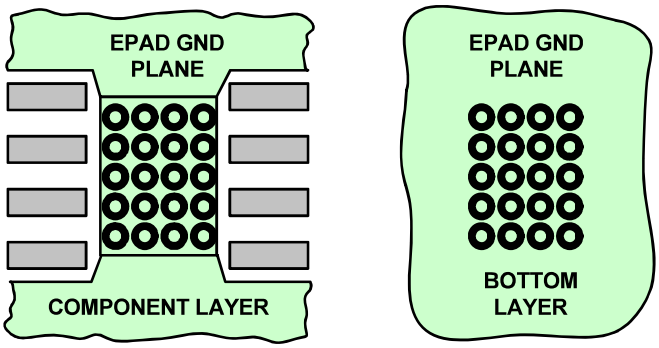


FIGURE 18. TYPICAL PCB PATTERN FOR THERMAL VIAS

For maximum heatsinking, it is recommended that a ground plane, connected to the EPAD, be added to both sides of the PCB. A via array, within the area of the EPAD, will conduct heat from the EPAD to the GND plane on the bottom layer. The number of vias and the size of the GND planes required for adequate heatsinking is determined by the power dissipated by the ISL89160, ISL89161, ISL89162, the air flow and the maximum temperature of the air around the IC.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
December 20, 2012	FN7719.3	Page 3 - Removed all ISL8916xFBECZ part numbers from Ordering Information table Page 4 - ESD CDM value changed from 1500V to 1000V
January 31, 2012	FN7719.2	(page 1) Figure 1 illustration improved. (page 1) Related literature added (AN1603). (page 1) Last paragraph of the product description is changed to better describe the improved turn on characteristics. (page 1) Features list is revised to improve readability and to add new product specific features. (page 3) Added parts for release in ordering information. (page 4) Abs Max Ratings ESD Ratings Charged Device Model changed from “1000” to “1500” (page 4) Note and figure references are added to the VDD Under-voltage lock-out parameter. (page 5) Note 9 is revised to more clearly describe the turn-on characteristics. (page 5) No load test conditions added to the rising and falling propagation matching parameters. (page 7) Figure 9 added to clearly define the startup characteristics. (page 8) The paragraphs of the Functional Description Overview describing the turn-on sequence is replaced by 3 paragraphs to more clearly describe the under voltage and turn-on and turn-off characteristics. (page 9) A new section is added to the application information describing how the drivers outputs can be paralleled. (pages 1..12) Various minor corrections to text for grammar and spelling. M8.15D POD on page 14 - Converted to new POD format. Removed table of dimensions and moved dimensions onto drawing. Added land pattern.
January 13, 2011	FN7719.1	Removed Option C Reference from Visio Graphics due to parts not releasing yet.
January 12, 2011		Converted to New Intersil Template Updated page 1 Graphic by depicting 2 lines showing positive threshold and 2 lines showing negative threshold: page 1 - Updated copyright to include 2011 page 1 - Removed Related Literature from due to documentation being nonexistent at this time. page 2 - Updated Pin Description Table by placing both pin numbers 1 and 8 on same line page 3 - Updated Ordering Information by adding option B parts page 4 - Added Note Reference to Inputs section in Electrical Spec Table page 5 - Changed Note in Electrical Spec Table From: Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. To: Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.
November 2, 2010	FN7719.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

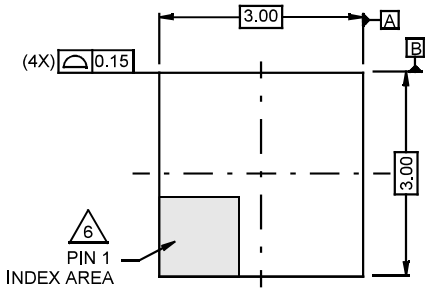
For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL89160, ISL89161, ISL89162

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

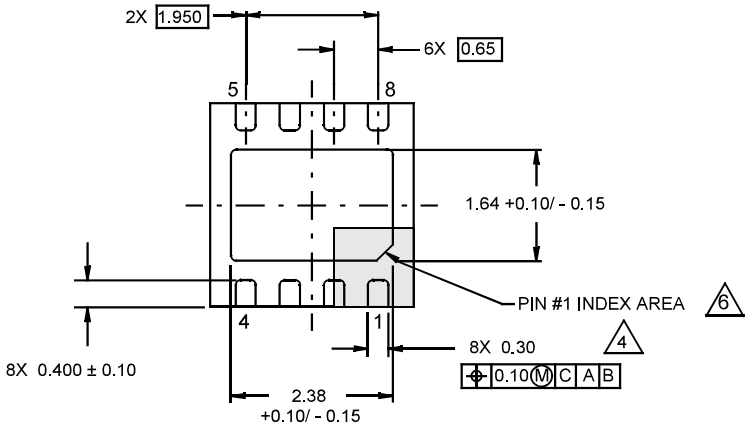
Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

Package Outline Drawing
L8.3x3I
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

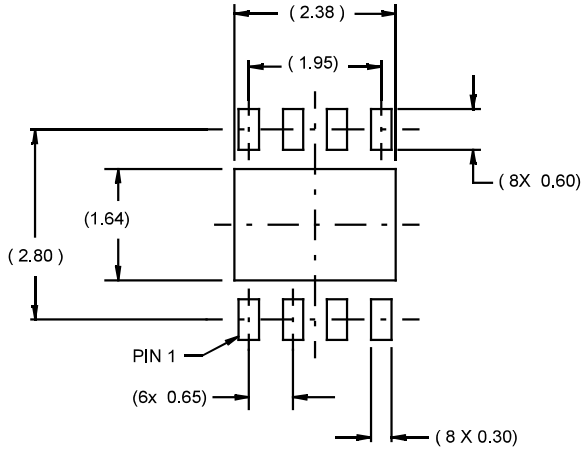
Rev 1 6/09



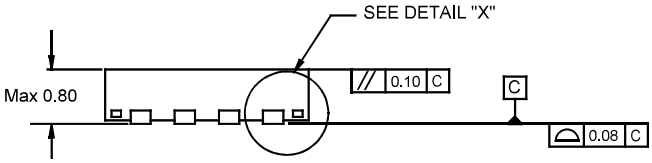
TOP VIEW



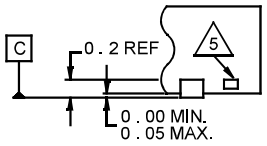
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

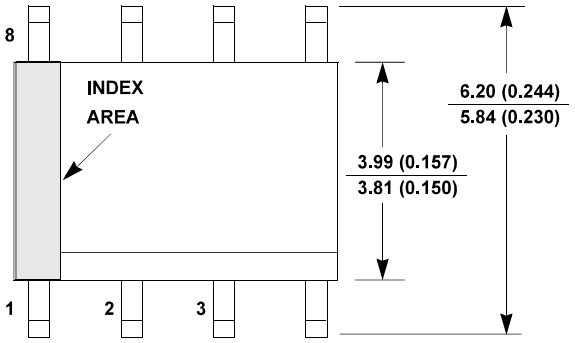
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

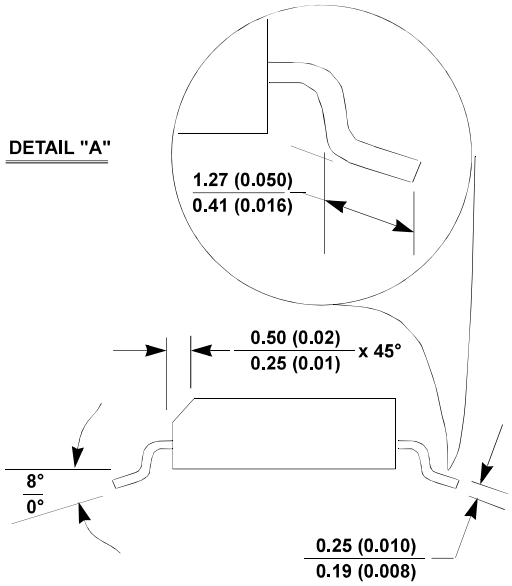
Package Outline Drawing
M8.15D

8 LEAD NARROW BODY SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE

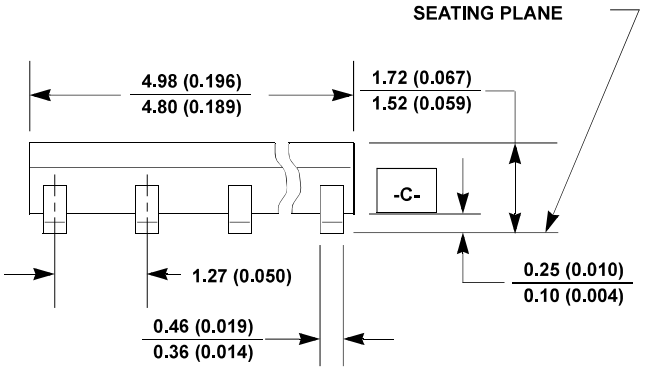
Rev 1, 3/11



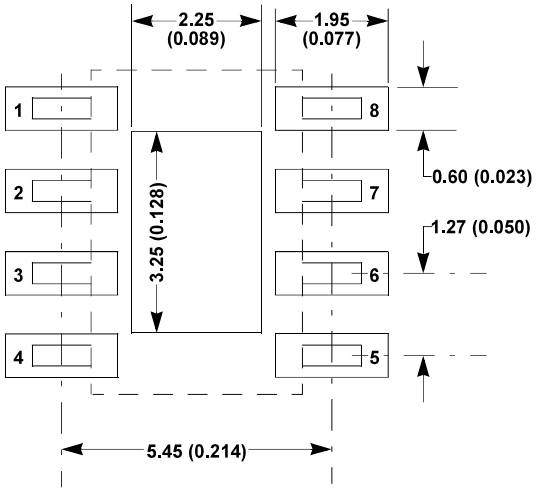
TOP VIEW



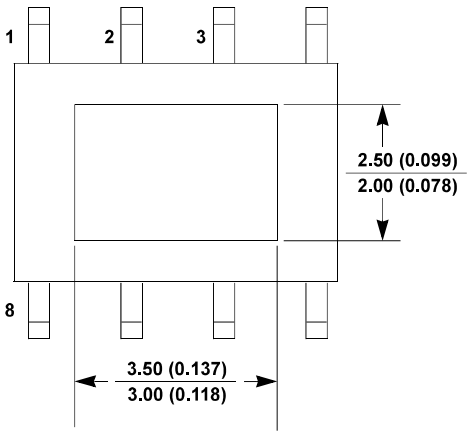
SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The Pin 1 identifier may be either a mold or a mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.