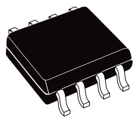
L6389E

High voltage high and low-side driver

Datasheet - production data



SO-8

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
  – 400 mA source
  – 650 mA sink
- Switching times 70/40 nsec rise/fall with 1 nF load
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down
- Internal bootstrap diode
- Outputs in phase with inputs
- Deadtime and interlocking function

Applications

- Home appliances
- Industrial applications and drives
- Motor drivers
  – DC, AC, PMDC and PMAC motors
- Induction heating
- HVAC
- Factory automation
- Lighting applications
- Power supply systems

Description

The L6389E is a high voltage gate driver, manufactured with the BCD ™ “offline” technology, and able to drive a half-bridge of power MOSFET/IGBT devices. The high-side (floating) section is enabled to work with voltage rail up to 600 V. Both device outputs can sink and source 650 mA and 400 mA respectively and cannot be simultaneously driven high thanks to an integrated interlocking function. Further prevention from outputs cross conduction is guaranteed by the deadtime function.

The L6389E device has two input and two output pins, and guarantees the outputs switch in phase with inputs. The logic inputs are CMOS/TTL compatible (3.3 V, 5 V and 15 V) to ease the interfacing with controlling devices.

The bootstrap diode is integrated in the driver allowing a more compact and reliable solution.

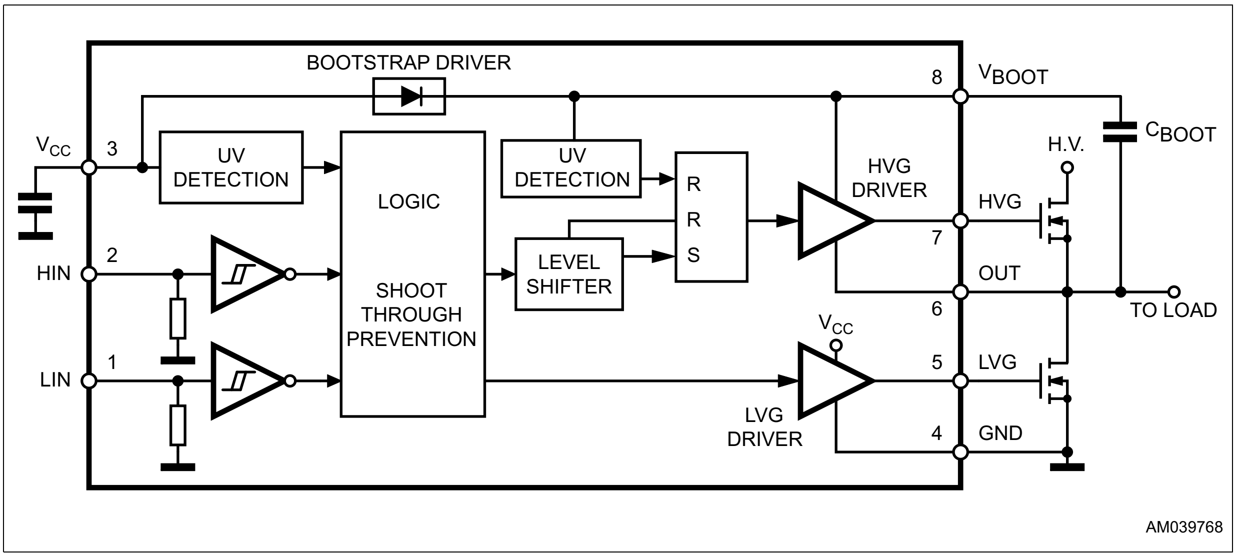
The L6389E device features the UVLO protection on both supply voltages (V_{CC} and V_{BOOT}) ensuring greater protection against voltage drops on the supply lines.

The device is available in an SO-8 tube, and tape and reel packaging options.

Contents

1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{OUT}	Output voltage	V_{BOOT} -18	V_{BOOT}	V
V_{CC}	Supply voltage	- 0.3	18	V
V_{BOOT}	Floating supply voltage	- 0.3	618	V
V_{hvg}	High-side gate output voltage	V_{OUT} -0.3	V_{BOOT}	V
V_{lvg}	Low-side gate output voltage	-0.3	V_{CC} +0.3	V
V_i	Logic input voltage	-0.3	V_{CC} +0.3	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)	750		mW
T_J	Junction temperature	-45	150	°C
T_s	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	SO-8	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	150	°C/W

2.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OUT}	6	Output voltage		(1)		580	V
V_{BS}(2)	8	Floating supply voltage		(1)		17	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF			400	kHz
V_{CC}	3	Supply voltage				17	V
T_J		Junction temperature		-45		125	°C

1. If the condition V_{BOOT} - V_{OUT} < 18 V is guaranteed, V_{OUT} can range from -3 to 580 V.
2. V_{BS} = V_{BOOT} - V_{OUT}.

3 Pin connection

Figure 2. Pin connection (top view)

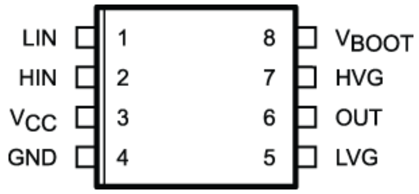


Table 4. Pin description

No.	Pin	Type	Function
1	LIN	I	Low-side driver logic input
2	HIN	I	High-side driver logic input
3	V_{CC}	P	Low-voltage power supply
4	GND	P	Ground
5	LVG(1)	O	Low-side driver output
6	OUT	P	High-side driver floating reference
7	HVG(1)	O	High-side driver output
8	V_{BOOT}	P	Bootstrap supply voltage

1. The circuit guarantees 0.3 V maximum on the pin (at I_{sink} = 10 mA). This allows the omission of the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

4 Electrical characteristics

4.1 AC operation

Table 5. AC operation electrical characteristics (V_{CC} = 15 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{on}	1 vs. 5 2 vs. 7	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V		225	300	ns
t_{off}		High/low-side driver turn-off propagation delay	V_{OUT} = 0 V		160	220	ns
t_r	5, 7	Rise time	C_L = 1000 pF		70	100	ns
t_f	5, 7	Fall time	C_L = 1000 pF		40	80	ns
DT	5, 7	Deadtime		325	470	615	ns

4.2 DC operation

Table 6. DC operation electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low supply voltage section							
V_{CCth1}	3	V_{CC} UV turn-on threshold		9.1	9.6	10.1	V
V_{CCth2}		V_{CC} UV turn-off threshold		7.9	8.3	8.8	V
V_{CChys}		V_{CC} UV hysteresis		0.9			V
I_{QCCU}		Undervoltage quiescent supply current	$V_{CC} \leq$ 9 V		250	330	µA
I_{QCC}		Quiescent current	V_{CC} = 15 V		350	450	µA
$R_{DS(on)}$		Bootstrap driver on resistance(1)	$V_{CC} \geq$ 12.5 V		125		Ω
Bootstrapped supply voltage section							
V_{BSth1}	8	V_{BS} UV turn-on threshold		8.5	9.5	10.5	V
V_{BSth2}		V_{BS} UV turn-off threshold		7.2	8.2	9.2	V
V_{BShys}		V_{BS} UV hysteresis		0.9			V
I_{QBS}		V_{BS} quiescent current	HVG ON			250	µA
I_{LK}		High voltage leakage current	$V_{hvg} = V_{OUT} = V_{BOOT}$ = 600 V			10	µA
High/low-side driver							
I_{so}	5, 7	Source short-circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	300	400		mA
I_{si}		Sink short-circuit current	$V_{IN} = V_{il}$ (t_p < 10 µs)	500	650		mA

Table 6. DC operation electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic inputs							
V_{il}	1, 2	Low logic level input voltage				1.1	V
V_{ih}		High logic level input voltage		1.8			V
I_{ih}		High logic level input current	V_{IN} = 15 V	13	20	25	µA
I_{il}		Low logic level input current	V_{IN} = 0 V	-1			µA
R_{P-DN}		Logic inputs pull-down resistor	V_{IN} = 15 V	600	750	1150	kΩ

1. $R_{DS(on)}$ is tested in the following way:

$$R_{DSON} = \frac{(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})}{I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})}$$

where:

I_1 is pin 8 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

5 Waveform definitions

Figure 3. Input to output waveform definition

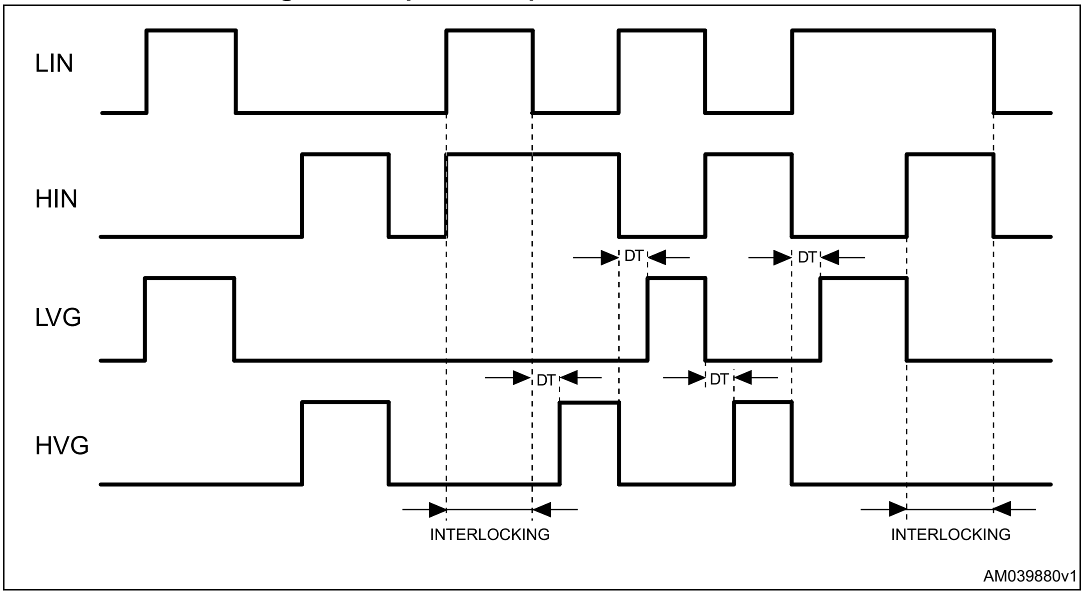


Figure 4. Propagation delay waveform definition

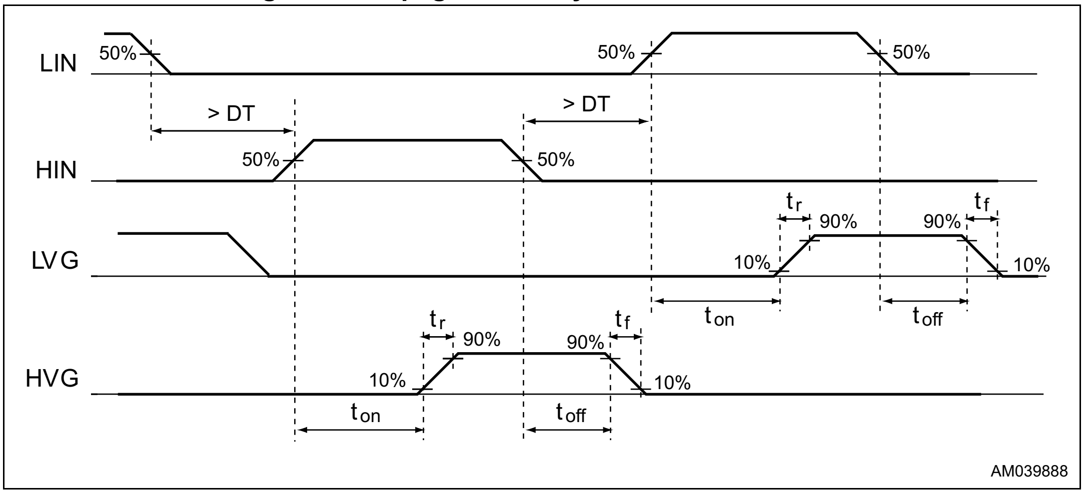
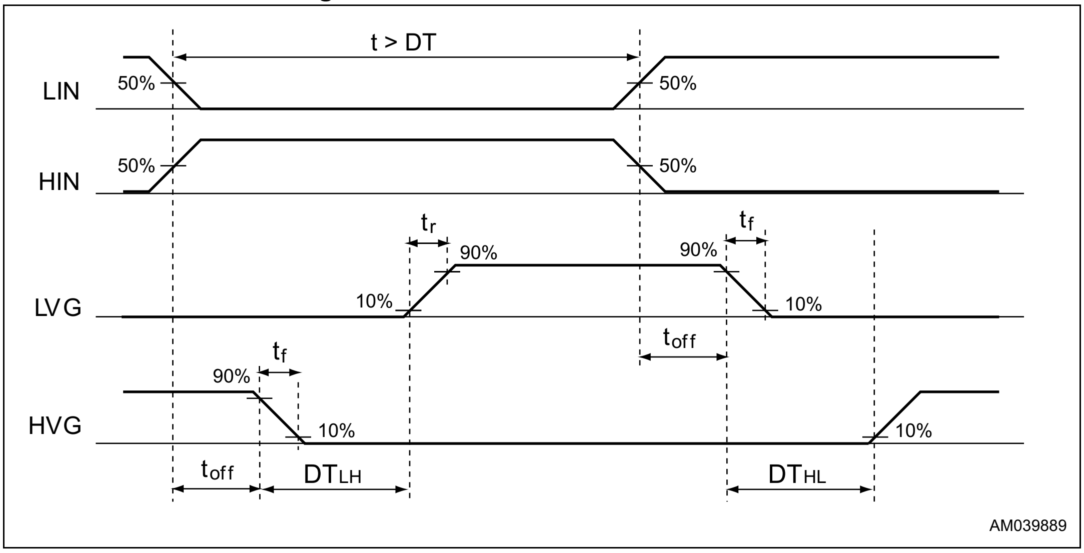


Figure 5. Deadtime waveform definition



6 Input logic

Table 7. Truth table

Input		Output	
HIN	**LIN**	**HVG**	**LVG**
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Input logic is provided with an interlocking circuitry which avoids the two outputs (LVG, HVG) being active at the same time when both the logic input pins (LIN, HIN) are at a high logic level. In addition, to prevent cross conduction of the external MOSFETs, after each output is turned off, the other output cannot be turned on before a certain amount of time (DT) (see *Figure 3*).

7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 6* a). In the L6389E device, a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 6* b. An internal charge pump (*Figure 6* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid an undesirable turn-on.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value, the external MOSFET can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOSFET total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It must be:

$$C_{BOOT} >>> C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop is 300 mV.

If HVG must be supplied for a long period, the C_{BOOT} selection must also take the leakage losses into account.

E.g.: HVG steady-state consumption is typical 250 μA, so, if HVG T_{ON} is 5 ms, C_{BOOT} must supply 1.25 μC to C_{EXT}. This charge on a 1 μF capacitor means a voltage drop of 1.25 V.

The internal bootstrap driver offers important advantages: the external fast recovery diode can be avoided (it usually has a high leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and, at the same time, the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 125 Ω). This drop can be neglected at low switching frequency, but it should be taken into account when operating at high switching frequency.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOSFET, $R_{DS(on)}$ is the on-resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 μs.

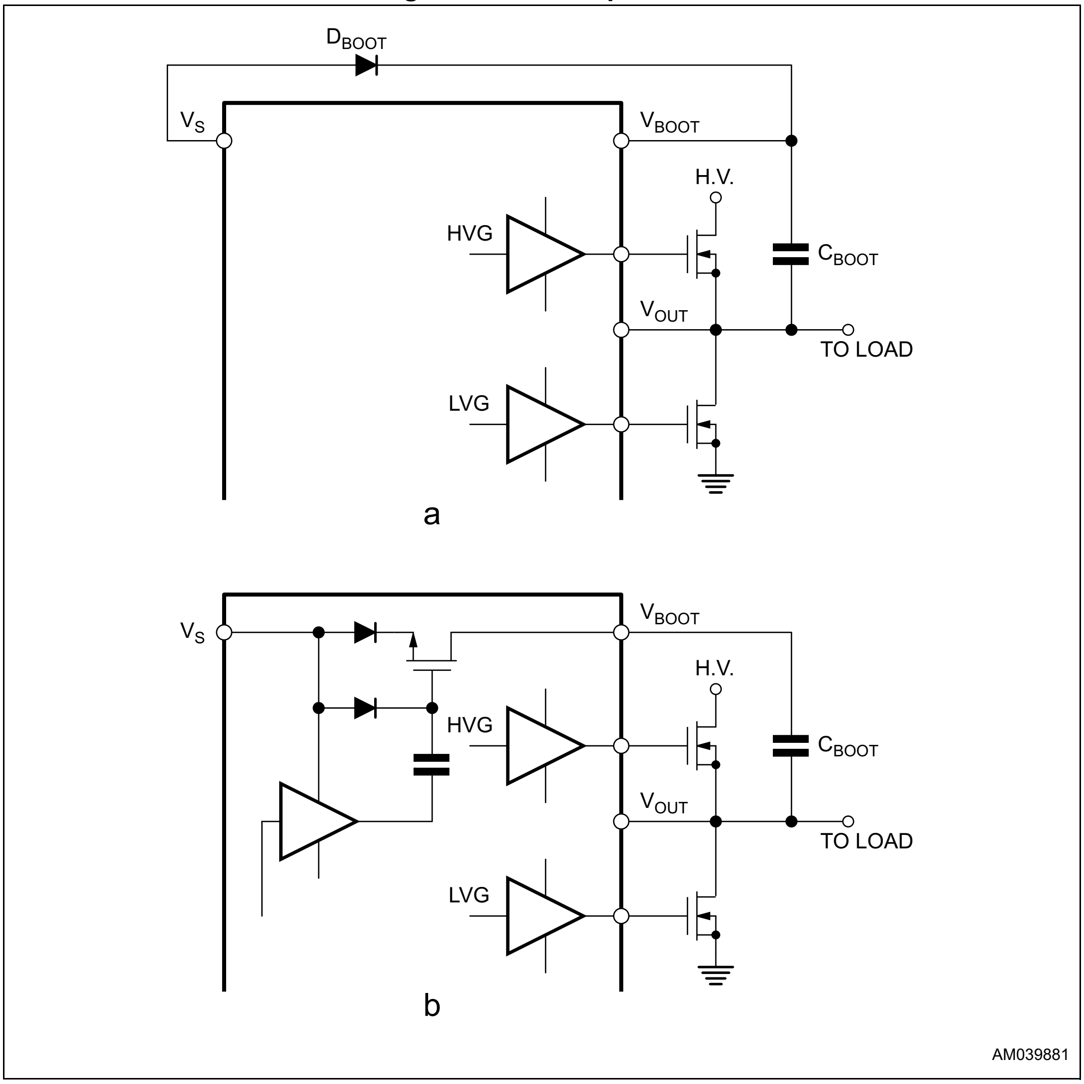
In fact:

Equation 3

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} should be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver



8 Typical characteristics

Figure 7. Typical rise and fall times vs. load capacitance

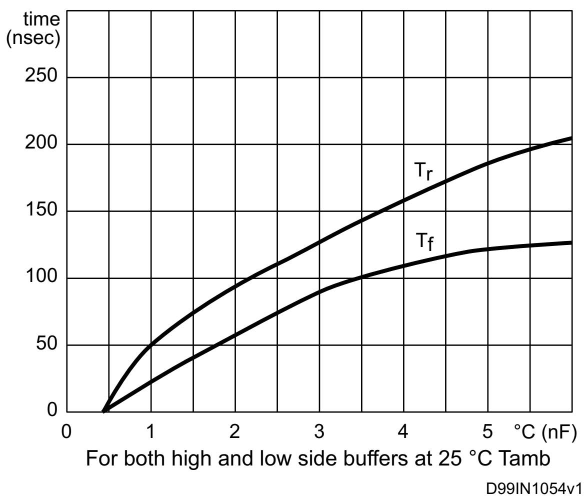


Figure 8. Quiescent current vs. supply voltage

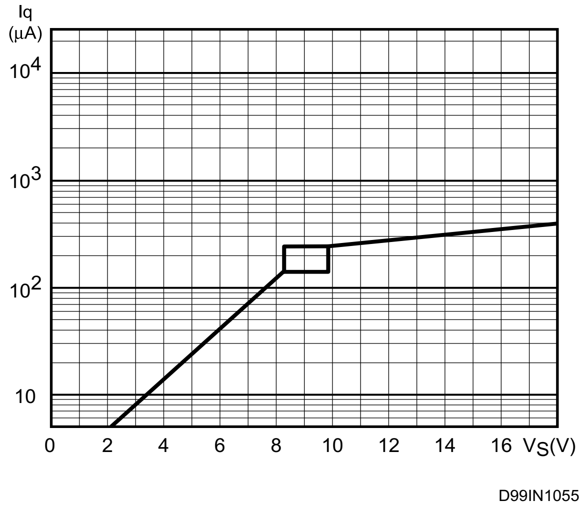


Figure 9. V_{BOOT} UV turn-on threshold vs. temperature

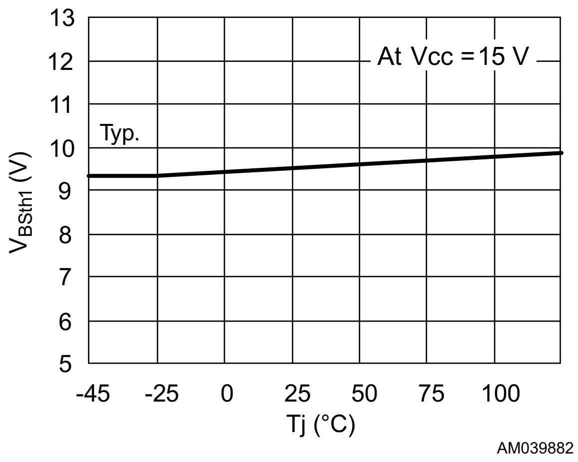


Figure 10. V_{CC} UV turn-off threshold vs. temperature

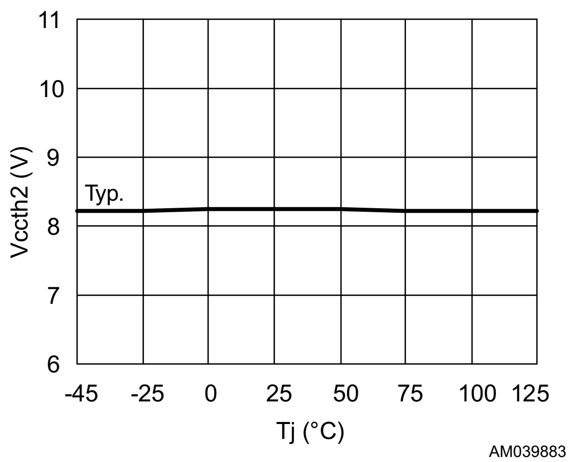


Figure 11. V_{BOOT} UV turn-off threshold vs. temperature

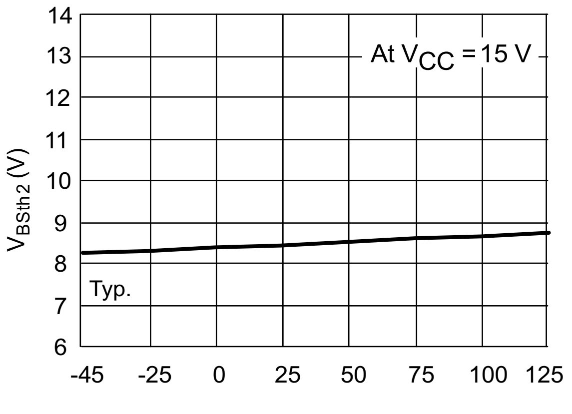


Figure 12. Output source current vs. temperature

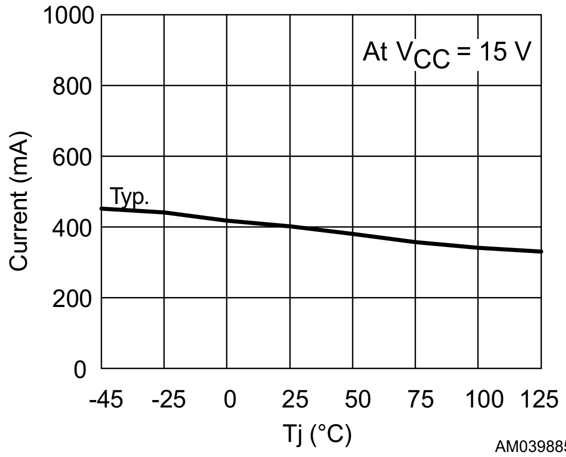


Figure 13. V_{CC} UV turn-on threshold vs. temperature

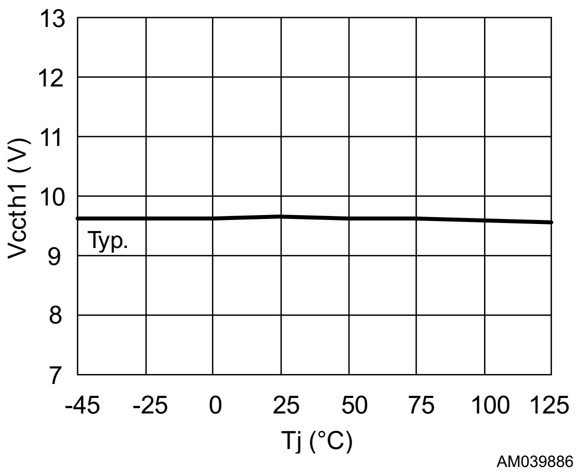
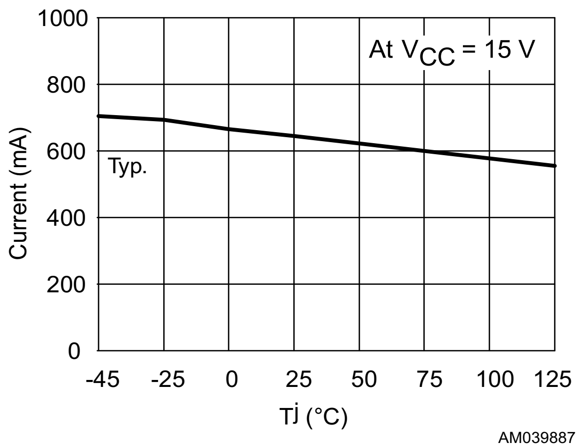


Figure 14. Output sink current vs. temperature



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 SO-8 package information

Figure 15. SO-8 package outline

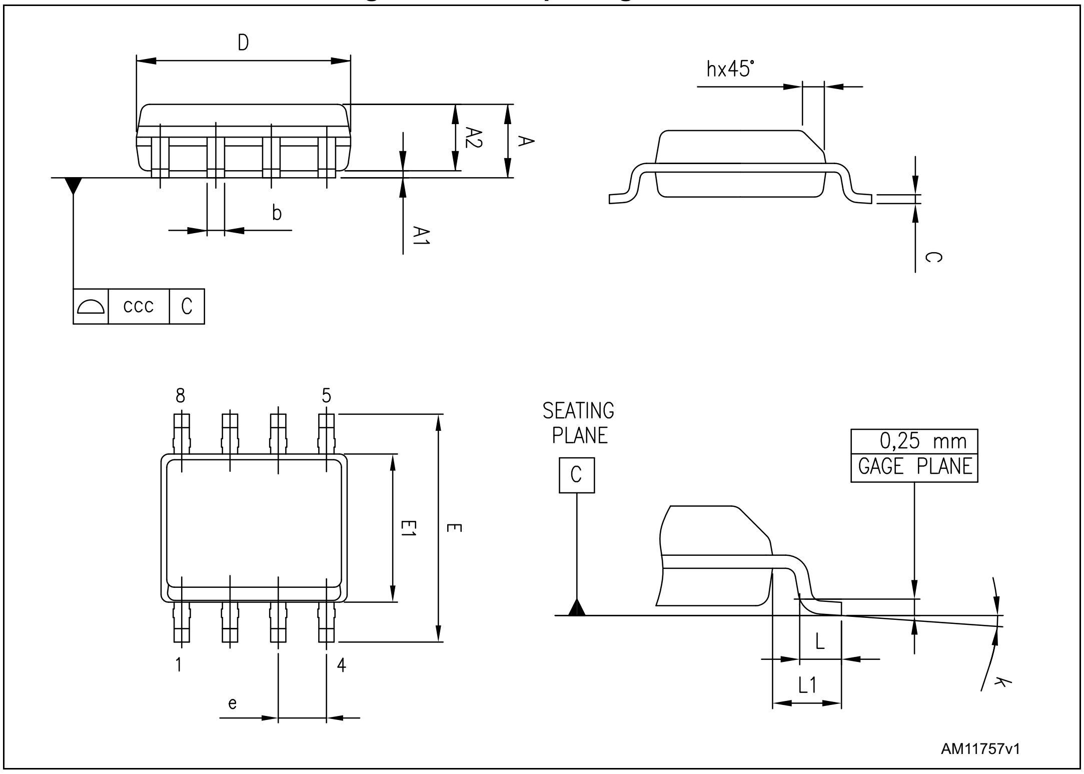


Table 8. SO-8 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

10 Order codes

Table 9. Order codes

Part number	Package	Packaging
L6389ED	SO-8	Tube
L6389EDTR	SO-8	Tape and reel

11 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-Sep-2016	1	First release