International
IOR Rectifier

May 2nd, 2014

Automotive Grade AUIRS20302S

Pre-regulated Three Phase Gate Driver

Features

- 3 phase gate driver for 24V & higher drives
- Under-voltage lockout for all channels
- Cross-conduction prevention logic
- High voltage pre-regulator MOSFET
- Power-on reset architecture
- FAULT detection and Reset
- Current sense comparator
- Over-current blanking time
- 3.3V logic compatible
- Matched propagation delay for all channels
- Fully operational up to +200V
- Floating channels for bootstrap operation
- High negative transients immunity
- Pre-regulated supply line for uP
- Automotive qualified
- Leadfree, RoSH Compliant

Typical Applications

24V to 150V – 3 Phase Motor Drives
Automotive & Truck HVAC, PUMP
BLDC Motor Drives

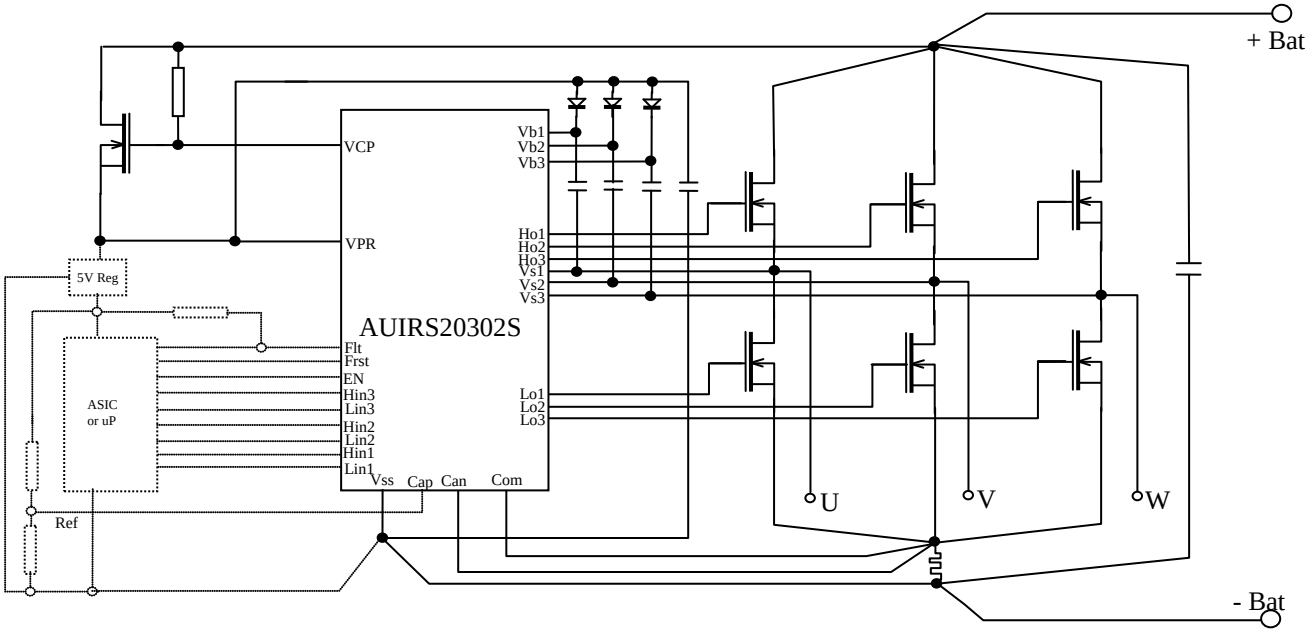
Product Summary

Topology	3-phase gate driver
V_{OFFSET}	200 V
V_{OUT}	8.0 V – 17 V
I_{o+} & I_{o-} (typical)	0.20 A & 0.35 A
t_{ON} & t_{OFF} (typical)	530 ns / 530 ns
Deadtime (typical)	0.7 us

Package

SOIC 28WB

Typical Connection Diagram



Description

The AUIRS20302S is a three phase gate driver dedicated to BLDC motor drive up to 600W. Proprietary HVIC technology enables this rugged monolithic design with enforced Automotive ESD & Latch-up grades. Primarily designed for 24V battery application, its drive capability goes from 12v to 200V which cover all the abnormal conditions of the vehicle. The gate drive circuitry features cross-conduction preventive and minimum dead-time blocks. It is powered by a constant voltage so that the gate drives never exceed 17V including during Load Dump condition.

An external MOSFET is acting as a pre-regulator. The inner charge pump and voltage control loop drives its gate in order to keep the VPR pin constant when the battery voltage varies. The AUIRS20302S also features an over-current protection that definitively shuts down all gates in case of short-circuit. The fault condition is reset by cycling the FRST pin while the I.C is disabled. A blanking time, synchronized with each high side switch command, avoids any premature triggering of the protection.

The logic control block of the AUIRS20302S is developed in order to support a fast and reliable 3 phase BLDC design. For example, its inputs are compatible with the 3.3V logic processors and feature a short-pulse/noise rejection filter. The 6 commands include matched propagation delays, shoot-through protections and minimum dead-time. The bootstrap capacitor voltage of each phase is monitored independently (UVLO). Also, the maximum gate voltage is controlled by the pre-regulator in all conditions. No linear or abnormal gate drive is possible. The VPR pin can also supply the surrounding system components if the total consumption doesn't exceed 0.1A.

Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC28	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	M1 (+/-200V) (per AEC-Q100-003)	
	Human Body Model	H1B (+/-2000V) (per AEC-Q100-002)	
	Charged Device Model	C3B (+/-500 V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to VSS, all currents are defined positive into any lead. An operation above the absolute maximum limit is not implied and could damage the part. The thermal resistance and power dissipation ratings are measured under board mounted and free air conditions

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	-0.3	220	V
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$ - 0.3	$V_{B\ 1,2,3}$ + 0.3	
$V_{S1,2,3}$	High side offset voltage	$V_{B\ 1,2,3}$ - 20	$V_{B\ 1,2,3}$ + 0.3	
VPR	Low side supply voltage	-0.3	17	
VCP	Charge pump output voltage	-0.3	17	
COM	Power ground	-5	5	
$V_{LO1,2,3,\ /\ FLT}$	Low side output voltage LO#; FLT pin	-0.3	VPR + 0.3	
V_{IN}	Input pin voltage (LIN#, HIN#,)	-0.3	VPR + 0.3	
Can/Cap	Over-current comparator inputs	-0.3	VPR + 0.3	
EN/Frst	Enable & Fault Reset inputs	-0.3	VPR + 0.3	
dV/dt	High side floating voltage slew rate	—	50	V/ns
Rth_{JA}	Junction to ambient thermal resistance	—	80	°C/W
T_J	Maximum operating junction temperature		150	°C
T_S	Maximum storage temperature	-55	150	
T_{Reflow}	Reflow max. temperature (60 sec.)	—	260	

Recommended Operating Conditions

The Input/Output timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are referenced to VSS. The VS & COM offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ +6	$V_{S1,2,3}$ +19	V
$V_{HO\ 1,2,3}$	High side output voltage HO#	$V_{S1,2,3}$-0.3	$V_{B1,2,3}$+0.3	
$V_{S\ 1,2,3}$	High side floating supply voltage	(Note 1)	200	
VPR	Low side supply voltage	6	17	
$V_{LO1,2,3}$	Low side output voltage LO#	-0.3	VPR+0.3	
COM	Power ground	-5	5	
$V_{HO1,2,3}$	High side output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage	COM	VPR	
V_{IN}	Logic input voltage LIN, HIN, EN, CAp, CAn, FRST	V_{SS}-0.3	VPR	
Vcan/cap	Common mode voltage on the CAN & CAP inputs	0	5	
VCP	Charge Pump Output Voltage	-	15	

Note 1: Logic operational for V_S between COM -5V to COM +200V. Logic state held for V_S of COM -5 to COM – V_{BS}. (Please refer to the Design Tip DT97 -3 for more details).

Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of VBIAS (VPR,VBS 1,2,3) = 15V. The VIN , VTH and IN parameters are referenced to VSS and are applicable to all six channels (HS 1,2,3 and LS 1,2,3). The VO and IO parameters are referenced to COM and VS 1,2,3 and are applicable to the respective output leads: LO1,2,3 and HO1,2,3.

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
VIN,th+	Input positive going threshold (Hin#, Lin#, EN, FRST)		-	1.9	2.5	V	
VIN,th-	Input negative going threshold (Hin#, Lin#, EN, FRST)		0,7	1	-		
Iin+	Input bias current (Lin#, Hin#, EN, FRST)		15	100	220	µA	Vin=5V
Iin-	Input bias current (Lin#, Hin#, EN, FRST)		-1	0	1		Vin=0V
VPR,UVth+	VPR supply undervoltage positive going threshold **(note 2)**		6.4	7.2	8,2	V	
VPR,UVth-	VPR supply undervoltage negative going threshold **(note 2)**		6	6.7	7.6		
VPR,UVhys	VPR supply undervoltage hysteresis **(note 2)**		0.4	0.5	0.7		
VBS, UVth+	VBS supply undervoltage positive going threshold		6.4	7.2	8,2		
VBS, UVth-	VBS supply undervoltage negative going threshold		6	6.7	7.6		
VBS, UVhys	VBS supply undervoltage hysteresis		0.4	0.5	0.7		
I_{LK}	Offset supply leakage current		-	5	50	µA	VB=VS=200V
Iqbs	Quiescent VBS supply current		20	45	120		
Iqpr	Quiescent VPR supply current		1	2,5	5	mA	VPR=14V
V_{OH}	High level output voltage, VPR – VO, HO#		0,2	0.9	1.4	V	Io =20mA
V_{OL}	Low level output voltage, VO, HO#		0,05	0.2	0.6		
Io+	Output high short circuit pulsed current, HO#,LO#		105	200	450	mA	Vo =0V, PW ≤10 µs
Io-	Output low short circuit pulsed current, HO#,LO#		210	350	650	mA	Vo =15V, PW ≤10 µs
VCP	Charge pump output voltage	VPR=4V	5	6	7,5	V	Rext=100kΩ
		VPR=8V	10	13	15		
		VPR=9V	13	15	17		
		VPR=14V	13	15	17		
ICP+	Charge Pump source current	VPR=6V	100	200	400	µA	
		VPR=14V	200	500	1000		
ICP-	Charge Pump sink current		-	5	10	mA	
Vcl_Vcp	Vcp pin Active Clamp		17	18.6	21		Icp=10mA
V_{FLT}	FLT low output voltage		-	-	0.8	V	I_{FLT} = 10mA
Ican1	Comparator input high bias current		-	-	7	µA	Can=5V
Ican0	Comparator input low bias current		-	-	7		Can=0V
Voff	Comparator input offset		-33	-	33	mV	Vcap= 5V
Tfrst	Minimum FAULT RESET time		20	-	-	us	
Ton_EN	Minimum ENABLE time		20	-	-	us	

(note 2):. UVPR is latched; when VPR>UVPR, FAULT remains pulled down. This leads to have the FAULT active and latched at VPR ramp up if no fault reset occurs.

Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of VPR = VBS = 15V, VS1,2,3 = VSS = COM, and CL = 1000 pF.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Ton	Turn-on propagation delay, LO#, HO#	350	550	850	nS	V_{IN} = 0 & 5V
Toff	Turn-off propagation delay, LO#, HO#	350	600	850		
LOt_r , HOt_r	Turn-on rise time LO#, HO#	10	100	300		
LOt_f , HOt_r	Turn-off fall time LO#, HO#	5	35	75		
T_{oc}	Over-current to output shutdown response time	-	1	1.7	uS	$V_{(Can)}$-$V_{(Cap)}$=1V
T_{FLT}	Over-current FLT response time	-	0.7	1.2		
t_{blank}	Current limit blanking time	5	6	7.5		
tFILIN	Input filter time (HIN, LIN)	200	270	510	nS	V_{IN} = 0 & 5V
DT	Dead-time	420	700	1000		VPR=15V

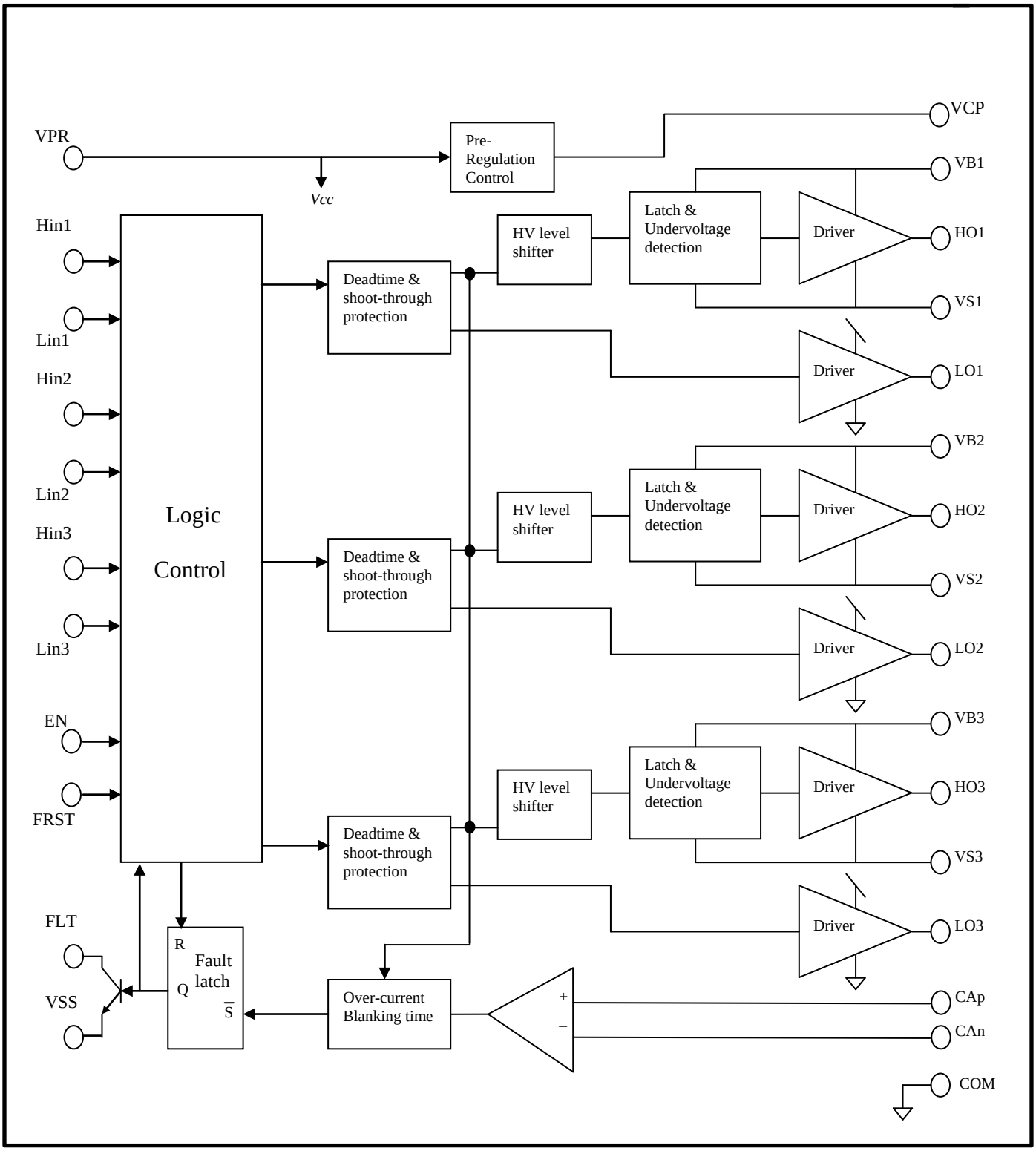
Truth Table

This table is valid for voltages ranges defined in the recommended operating conditions section.

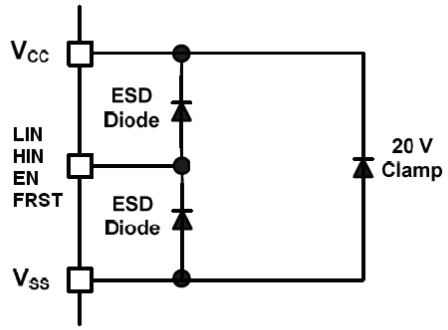
ENABLE	CAN>CAP	FRST	LIN#/HIN#		LO#/HO#	FLT	Comments
0	0	0	X		0	No Change	FLT keeps showing same status
0	1	0	X		0	Vss	
0	0	1	X		0	Open	FLT Reset Sequence (Note3)
0	1	1	X		0	Vss	
1	0	X	LIN#/HIN#		LO#/HO#	Open	Normal Operation: An anti-shoot-through logic prevents each channel from turning on simultaneously the HS and LS switches
1	1	0	LIN#/HIN#		0	Vss	Over-current detection (FLT)
1 *	**1 ***	**1 ***	**LIN#/HIN# ***		**LO#/HO# ***	**Open***	***** **Not recommended** **(cycling on default)**

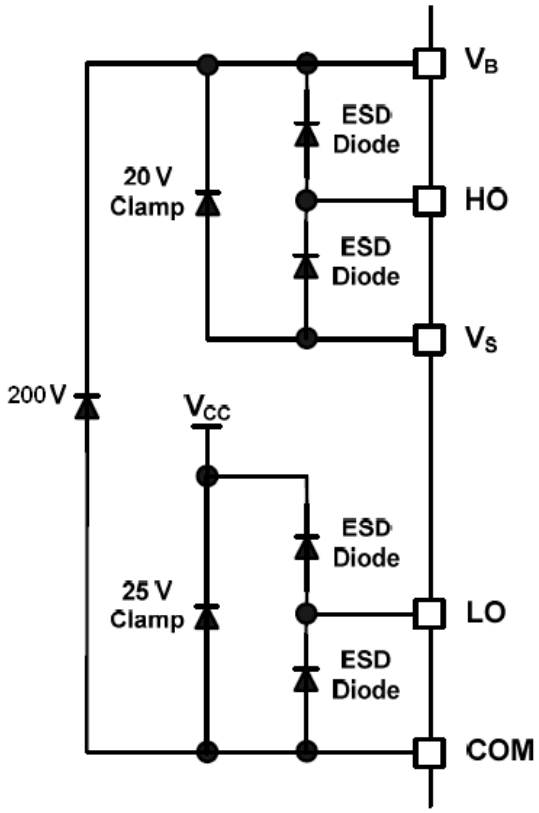
Note 3: The proper sequence to reset the Fault latch is to first set EN at 0V and then cycle the FRST pin. The gate drives return to normal operation when EN is set again at 5V.

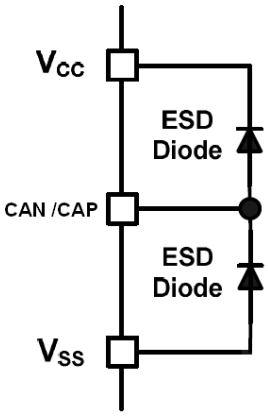
Functional Block Diagram

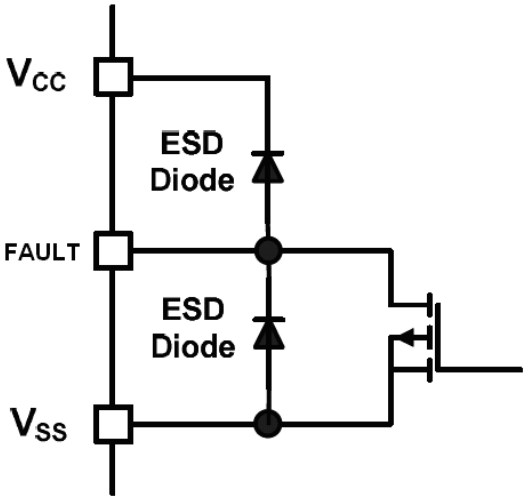


Input/Output Pin Equivalent Circuit Diagram





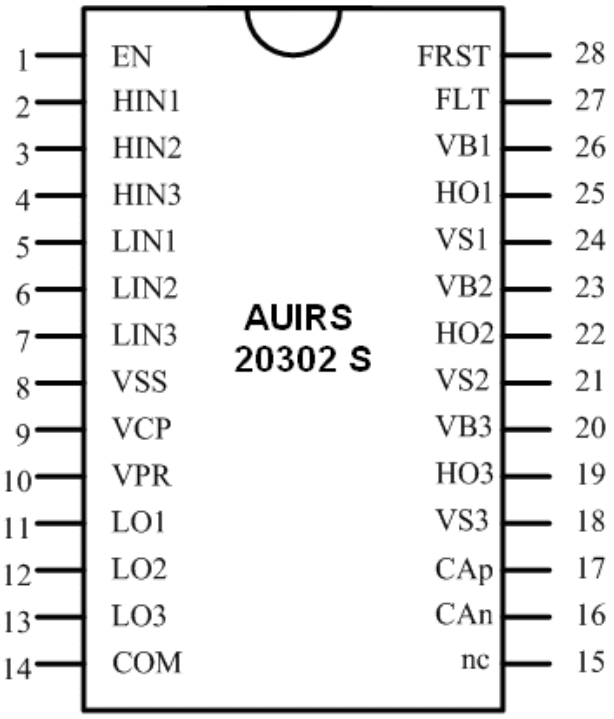




Lead Definitions

Symbol	Description
HIN#	Input for high side gate drive – Active high
LIN#	Input for low side gate drive – active high
VSS	Logic Ground
VCP	Pre-regulated MOSFET gate output – Analog gate drive
VPR	Power supply pin of the I.C (equivalent to Vcc)
LO#	Low side gate driver outputs (1,2 & 3)
COM	Common low side gate drive return pin & Power Ground
CAP	Non inverting input of the over-current comparator
CAN	Inverting input of the over-current comparator
VS#	High side floating supply return (1, 2 & 3)
HO#	High side gate driver outputs (1, 2 & 3)
VB#	High side floating supply (1, 2 & 3)
EN	Enable input – Active high
FAULT	Fault output pin – Open collector
FRST	Fault Reset input pin – Active high

Lead Assignments



Application Information and Additional Details

Input Short-Pulse / Noise Rejection Filter

The inputs of this I.C are compatible with CMOS and TTL standards. The AUIRS20302S has been designed in order to also interface the 3.3V logic signals. The VIN th+ and VIN th- thresholds of the input Schmitt trigger were set to 1.9V and 1V (typical). Figure #1 shows the inner logic signal versus the input profile.

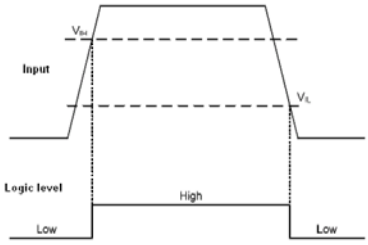


Figure 1: Input Thresholds

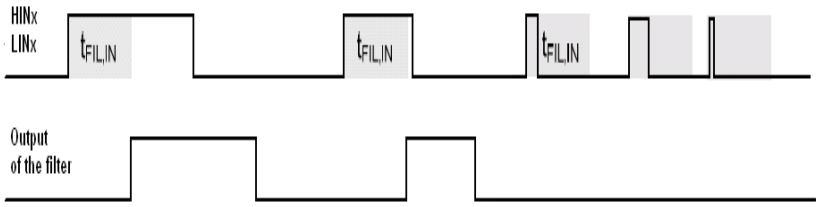


Figure 2: Input Filter

A filter is then implemented just after the Schmitt trigger on every input pin. HIN & LIN feature a 270 ns filter (typical) while FRST & EN have a 50 ns one. Its principle greatly improves the input/output pulse symmetry as well as helps reject noise spikes. The behaviour of the input filters is presented in the Figure #2. The parameter tFILIN represents the minimum pulse duration to pass the filter.

Logic Control Block

This block centralizes all the logic signals in order to: Generate the proper Outputs drives with minimum dead-time insertion, prevent shoot-through sequences, blank premature triggering of the short-circuit comparator and reset the FAULT flag. The enable pin (EN) switches off all outputs immediately in case of an urgent system request. It actually can be used to cycle the gates. The figure #3 shows all the signals timing.

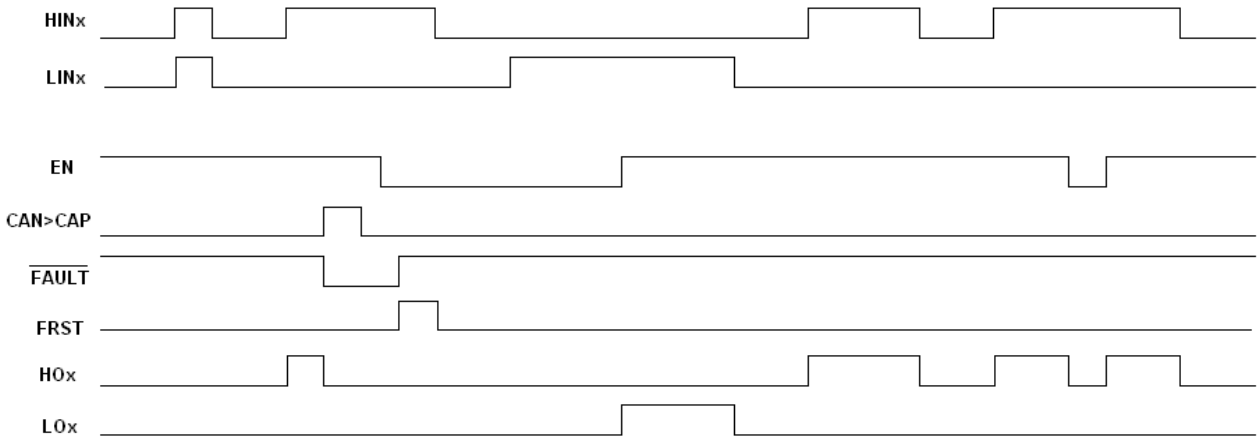


Figure 3: Input/Output Timing Diagram

The AUIRS20302S features an embedded dead-time circuitry. It inserts a minimum time period in which both the high and low side switches are forced OFF. By this mean and for each leg, each power switch is fully off before the next one turns on. This dead-time is automatically inserted by the AUIRS20302S including when the command sequence does include a shorter DT. Sequences with larger dead-time are not affected by the driver. Figures #4 & 5 show the dead-time principle and timing on the outputs. The dead-times are matched not only for each leg (high side / low side matching) but also among the three legs.

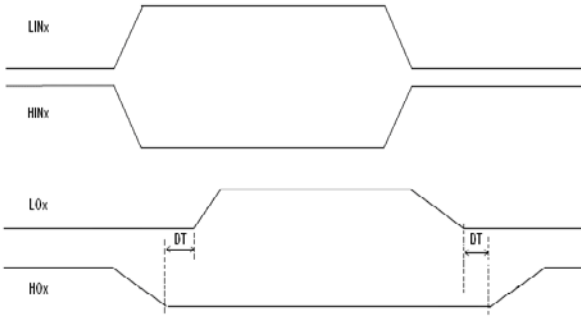


Figure 4: Dead-time Principle

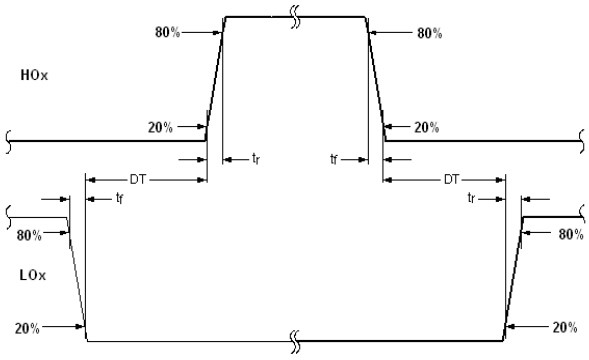


Figure 5: Output Timing (dead-time)

Protection Blanking time & Fault Reset Sequence

The CAN and CAP pins are intended to interface a shunt. In case of over-current protection (CAN>CAP), the FLT pin and all the gates are pulled down. There is a blanking time circuitry on the over-current protection. The comparator output is ignored for (t_{blank}) µS after each HINx rising edge. The fault reset is achieved by the following sequence: a) force EN pin to Gnd and b) cycle the FRST pin for the recommended minimum time (t_{frst}). Then, pulling-up again the EN pin resumes normal operation. Figure #6 shows the fault and output sequences while figure #7 emphasizes the reset sequence.

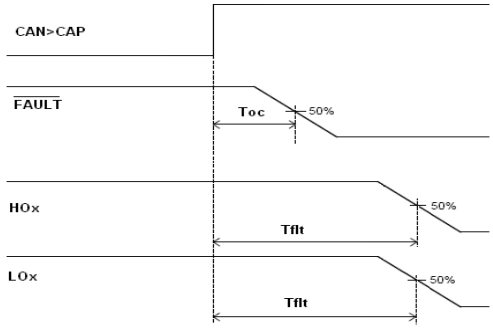


Figure 6: Fault/Output after SC

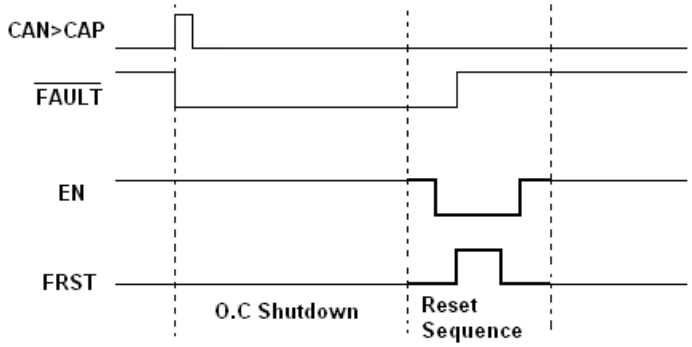


Figure 7: Fault Reset Sequence

Pre-regulated VPR voltage

The AUIRS20302S features a pre-regulated supply in order to maintain reasonable gate voltages in all conditions. This circuitry is composed of a VCO controlled charge pump, a comparator and a protective active clamp. Those three blocks were specifically designed in order to minimize their EMI contribution to the whole system. The MOSFET gate is regulated at 15V. Depending on the MOSFET gate threshold, VPR is then stabilized at ‘’ VCP – Vt ‘’ which usually ends up between 12V and 13.5 V. A higher VPR voltage is achievable by using a logic level MOSFET. The gate voltage and the charge pump output are protected by a 17V clamp. The figure #8 presents the block diagram of the pre-regulator circuitry with the 100K resistor needed between the Gate and the Drain of the MOSFET.

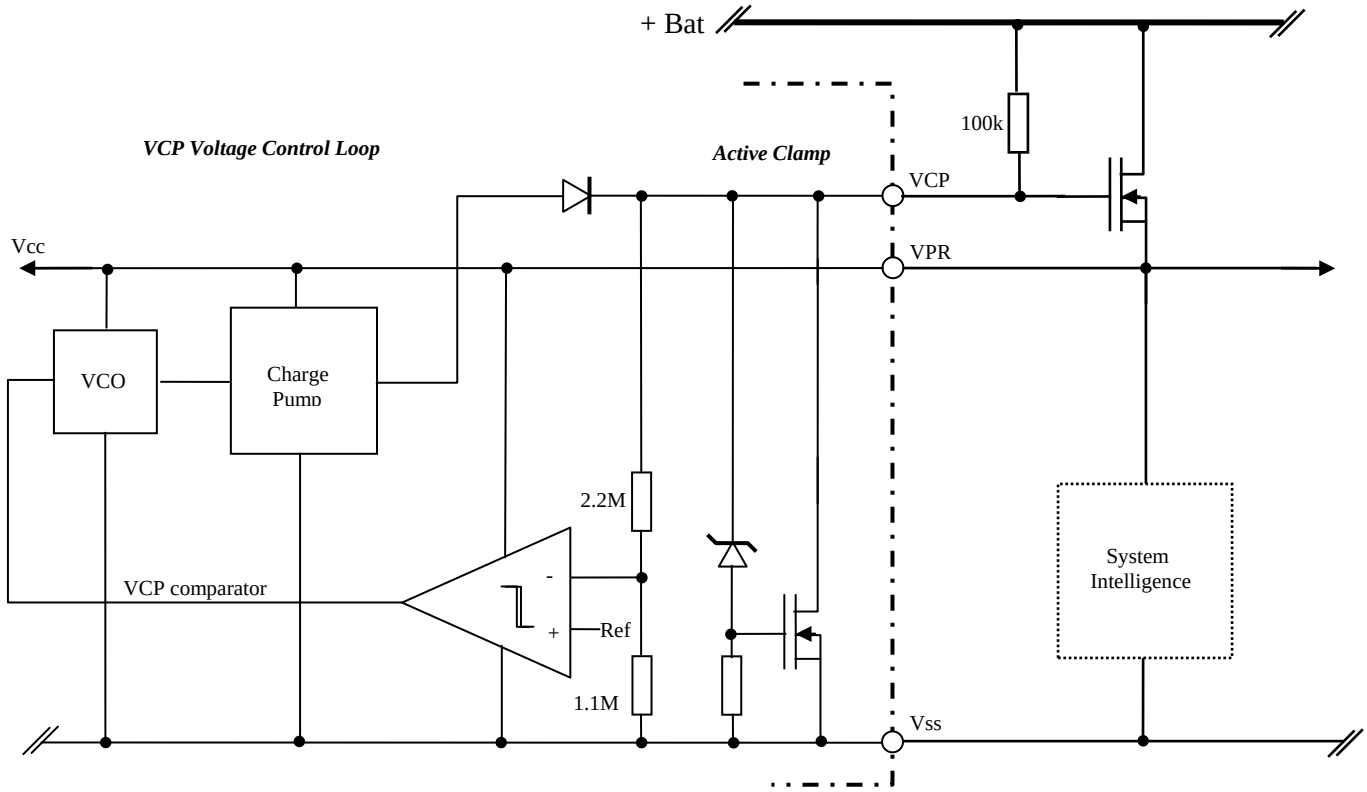


Figure 8: Pre-regulator Block Diagram

During the power-up sequence, the gate is biased thanks to the 100k resistor connected to its drain. When Vbat exceeds 4V, the charge pump output is already close to the MOSFET gate threshold. At 6V, VCP is typically higher than 9V (see VCP values – page 5 – Static Electrical Characteristics). So, during Vbat ramp-up, the MOSFET is first biased by the resistor until the charge pump overcomes the gate voltage and turns it fully on. As Vbat keeps increasing, the MOSFET remains fully on until the voltage closed loop enters the linear mode to control and stabilize VCP at 15V.

Pre-regulator MOSFET drive

The stabilized VPR voltage supplies the I.C and the bootstrap diodes thus the MOSFET power dissipation is quite low. It can also supply the system components. In that case, the power MOSFET dissipation has to be evaluated carefully and the implementation of an extra heat-sink considered. In some applications, it may be necessary to know at what exact voltage the charge pump overcomes the resistive bias of the pre-regulator MOSFET. This voltage depends on the total MOSEFT drain current (Iqpr + system consumption). For example, the system intelligence may include a regulator whose voltage drop influences the minimum operation voltage. If we consider the voltage drop of a 5V regulator at 0.8V, what is the status of the pre-regulator MOSFET when Vbat passes 5,8V (already fully on or still in the source follower mode)?

Figure #9 summarizes the procedure to evaluate the exact Vbat voltage at which the pre-regulator MOSFET is turned fully on by the charge pump. It is a 4 steps procedure where ‘’ I load ‘’ represents the quiescent current of the I.C plus the system consumption (in the voltage range considered). Looking to the MOSFET characteristic at the specific ‘’ I load ‘’ drain current point gives the corresponding Vgs value. The MOSFET will be fully on when the VCP pin exceeds this Vgs value. The charge pump characterization is then used to determine the exact VPR voltage at which the quantity ‘’VCP-VPR’’ exactly equals the identified Vgs. Finally, from the VPR value, the corresponding VCP voltage

is extracted again from the charge pump characterization. At this point of operation, the VCP voltage equals the Vbat potential at which the MOSFET becomes fully on (no voltage drop across the biasing resistor in this mode).

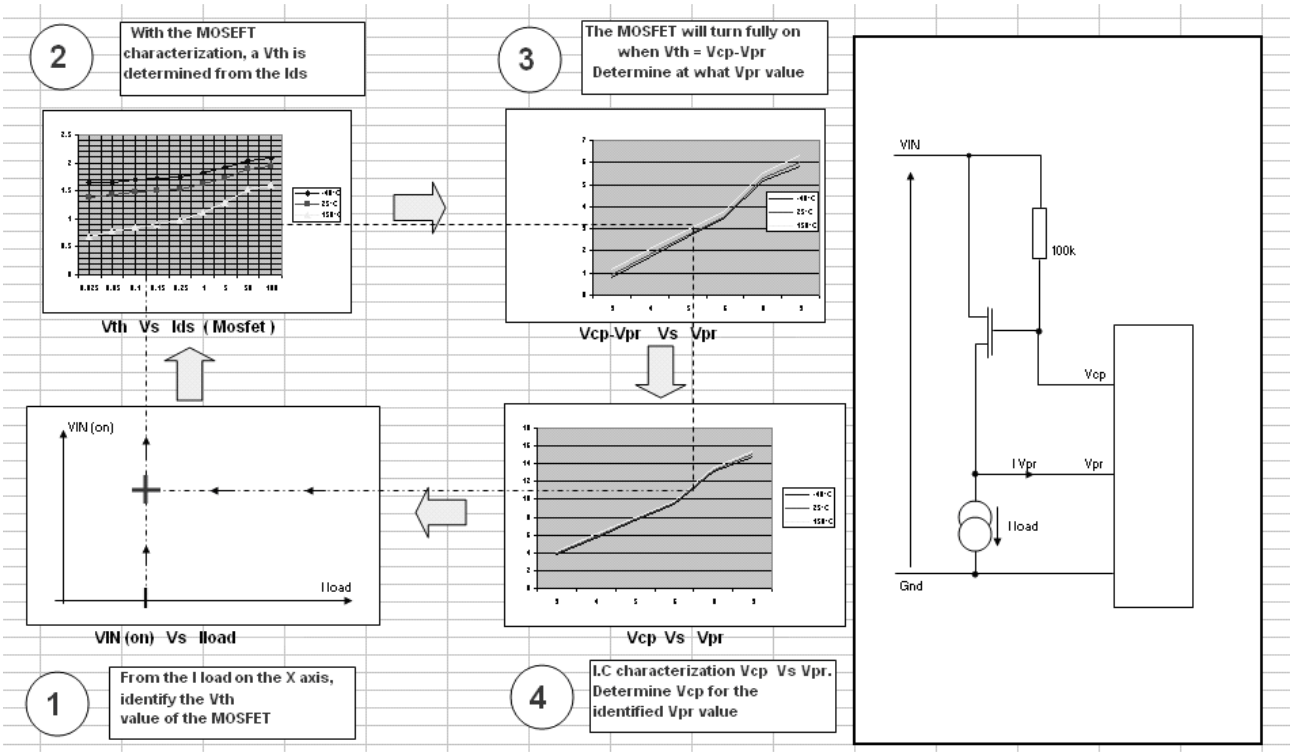


Figure 9: The 4 Step Procedure

PCB recommendations

The PCB is designed in order to minimize the gate drive wires, make the power topology up to 15A continuous capable and have the shunt interface as short as possible. Also, ground star connection is located at the bottom of the shunt.

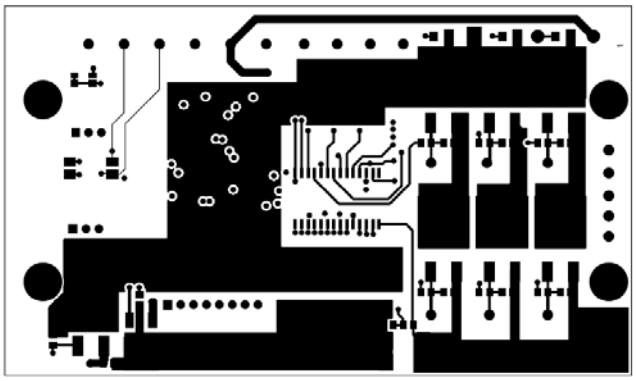


Figure 10: Component Face Layout

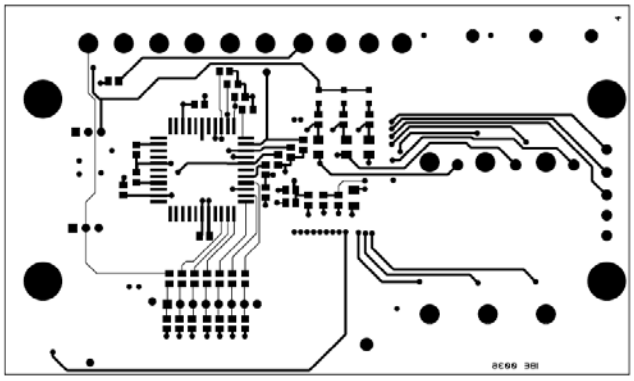


Figure 11: Solder Face Layout

The following schematic is an example of the AUIRS20302S application. It is a 100W-24V BLDC motor drive for an actuator. The power MOSFETs and the pre-regulator are designed in order to pass the 60V truck load dump condition. The system intelligence is powered via a 5V regulator connected to the VPR pin.

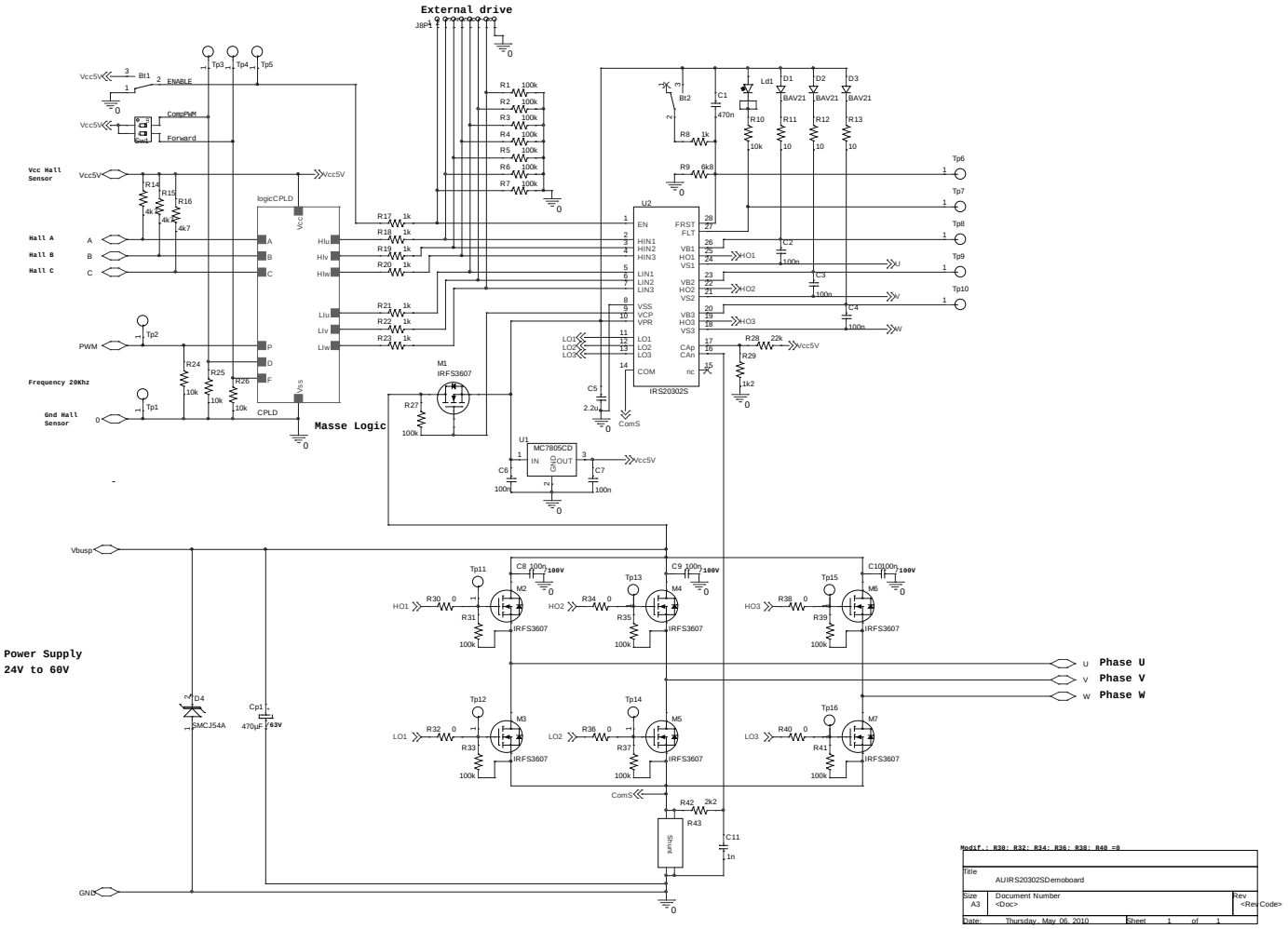


Figure 12: 100W – 24V BLDC Application Schematic

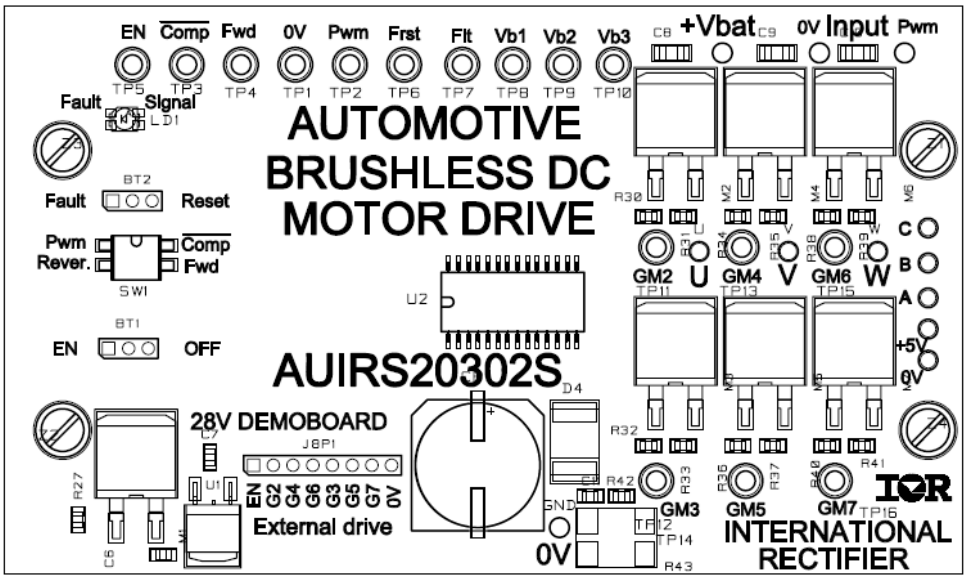


Figure 13: Component Implementation

Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS20302S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) with supply voltage of 15V in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

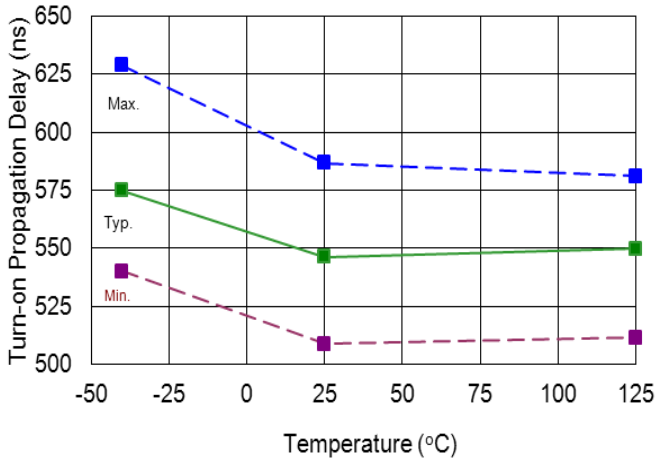


Figure 14. Turn-On Propagation Delay vs. Temperature

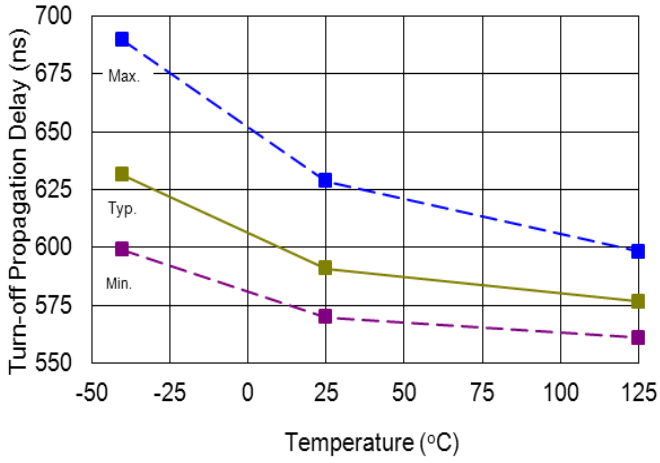


Figure 15. Turn-Off Propagation Delay vs. Temperature

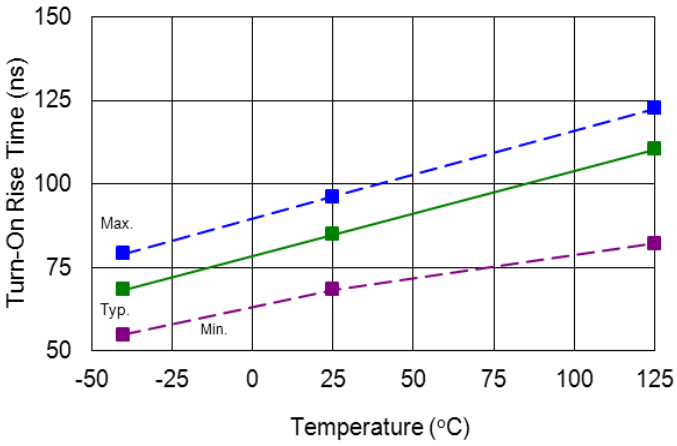


Figure 16. Turn-On Rise Time vs. Temperature

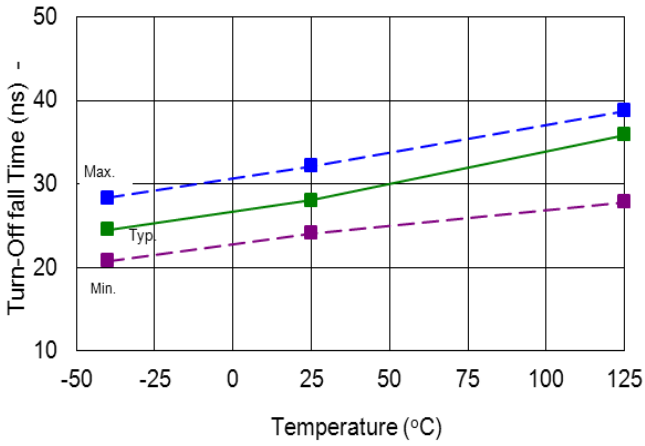


Figure 17. Turn-Off Fall Time vs. Temperature

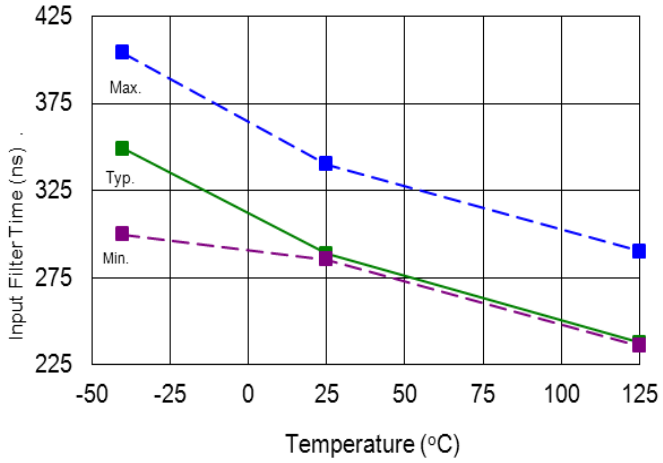


Figure 18. Input Filter Time vs. Temperature

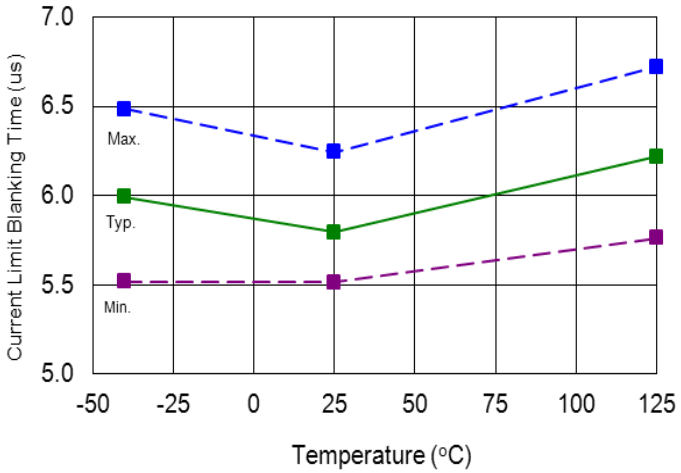


Figure 19. Current Limit Blanking Time vs. Temperature

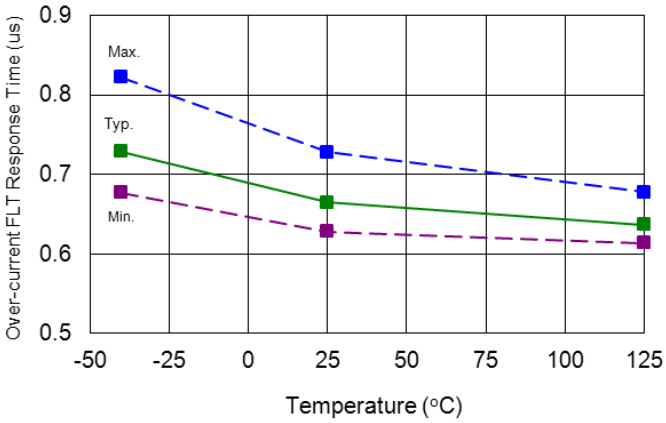


Figure 20. Over Current Response Time vs. Temperature

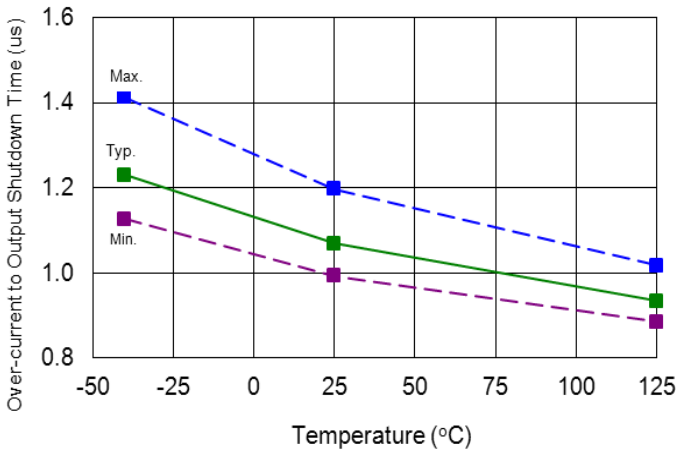


Figure 21. Over Current Shutdown Time vs. Temperature

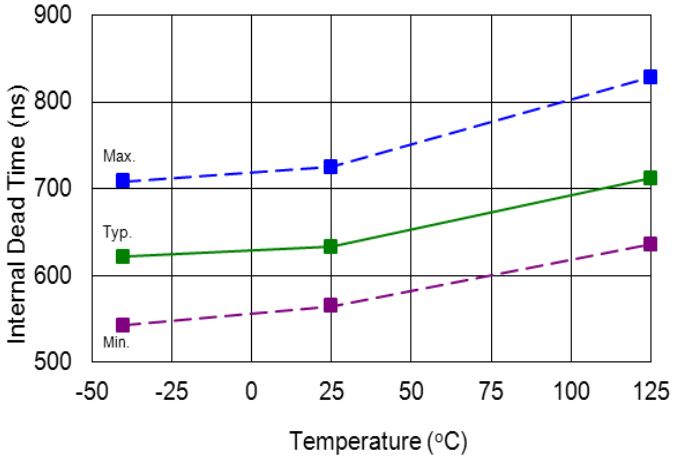


Figure 22. Dead Time vs. Temperature

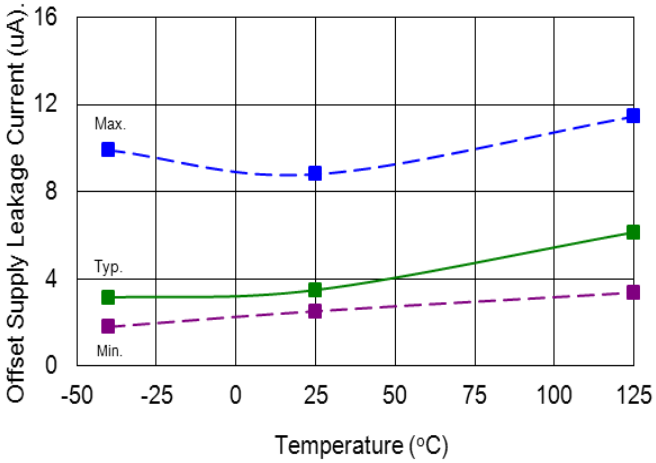


Figure 23. Offset Leakage Current vs. Temperature

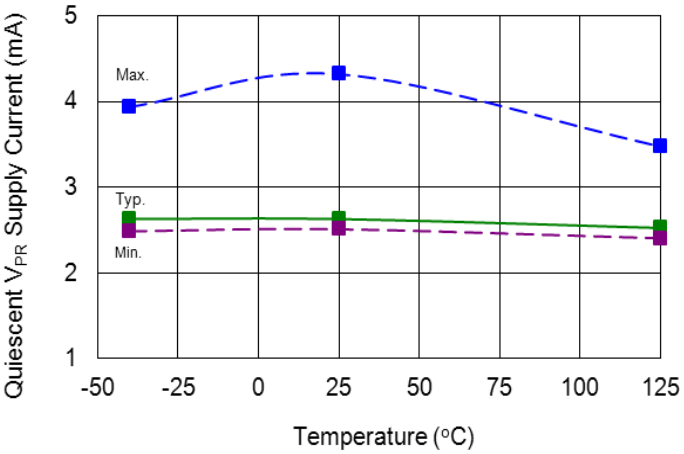


Figure 24. Quiescent VPR Current vs. Temperature

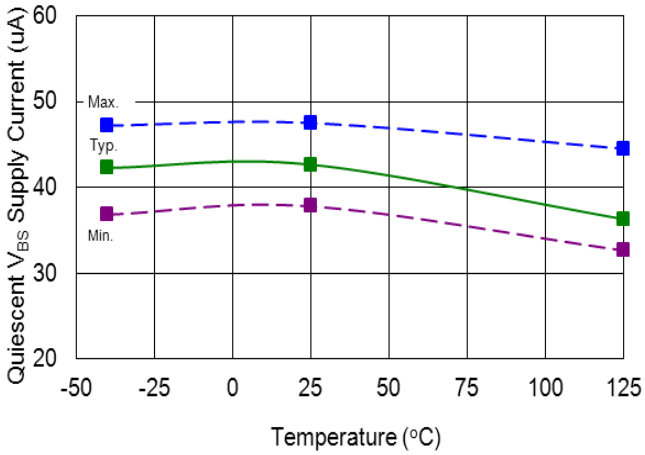
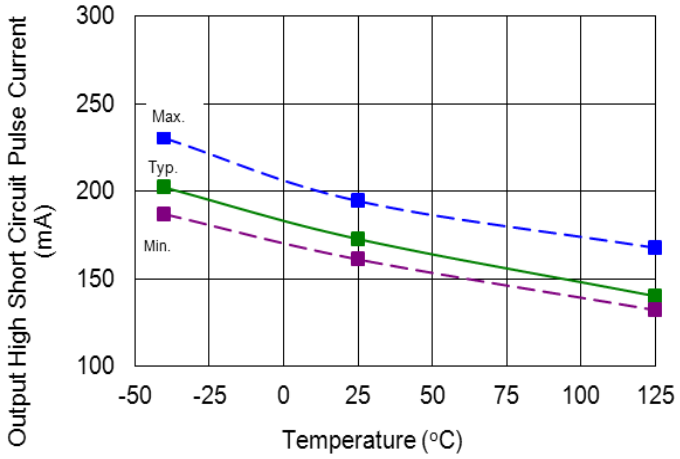


Figure 25. Quiescent VBS Current vs. Temperature



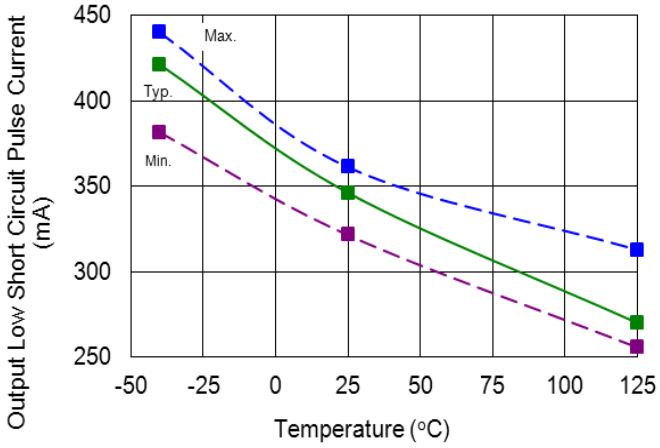


Figure 26. Output High Pulse Current vs. Temperature

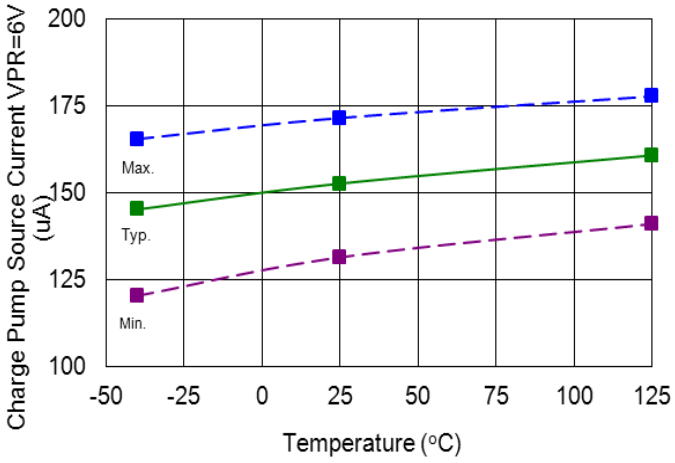


Figure 28. Charge Pump Source Current vs. Temperature VPR = 6V

Figure 27. Output Low Pulse Current vs. Temperature

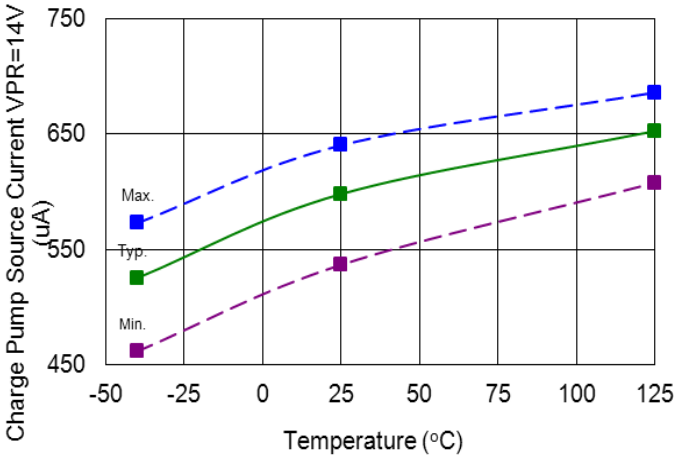


Figure 29. Charge Pump Source Current vs. Temperature VPR = 14V

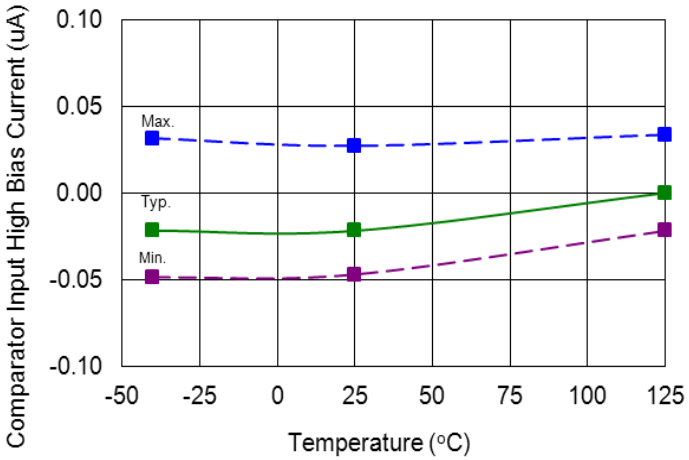


Figure 30. Comparator Input High Current vs. Temperature

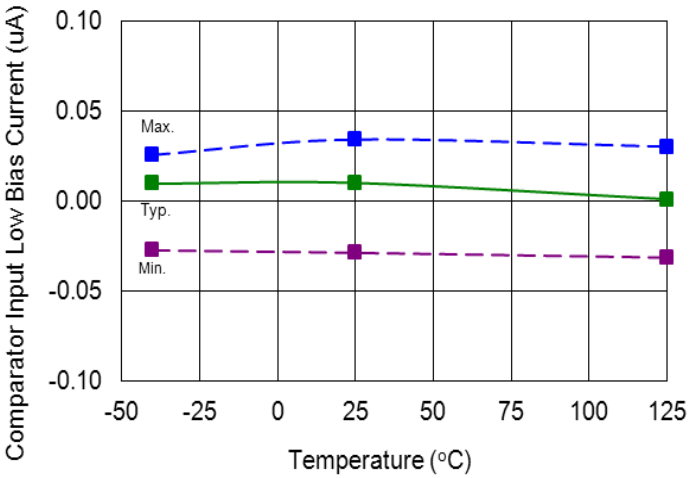


Figure 31. Comparator Input Low Current vs. Temperature

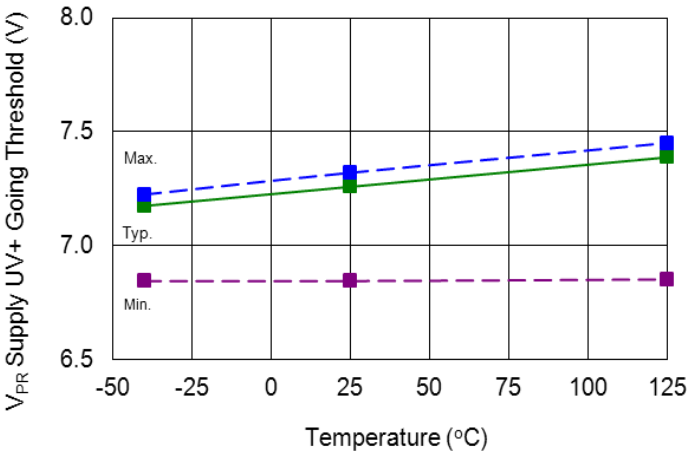


Figure 32. VPR UV+ Going Threshold vs. Temperature

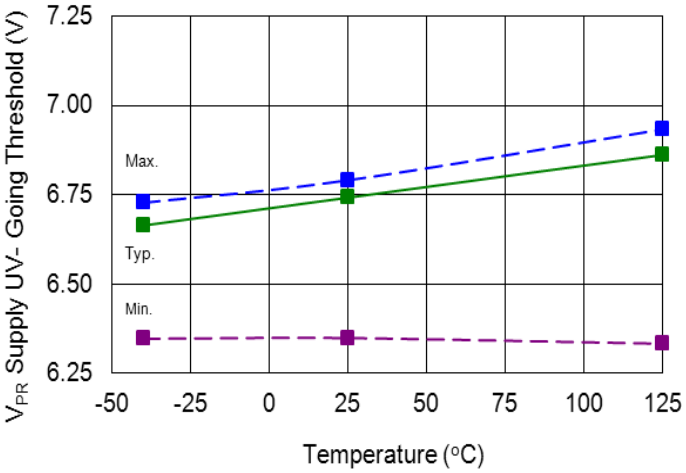


Figure 33. VPR UV- Going Threshold vs. Temperature

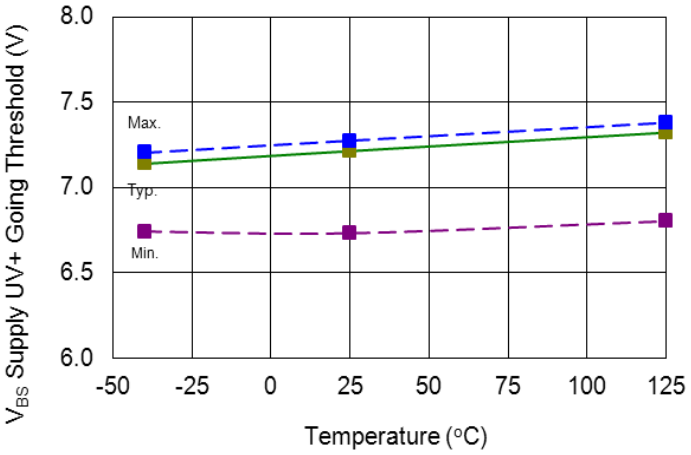


Figure 34. VBS UV+ Going Threshold vs. Temperature

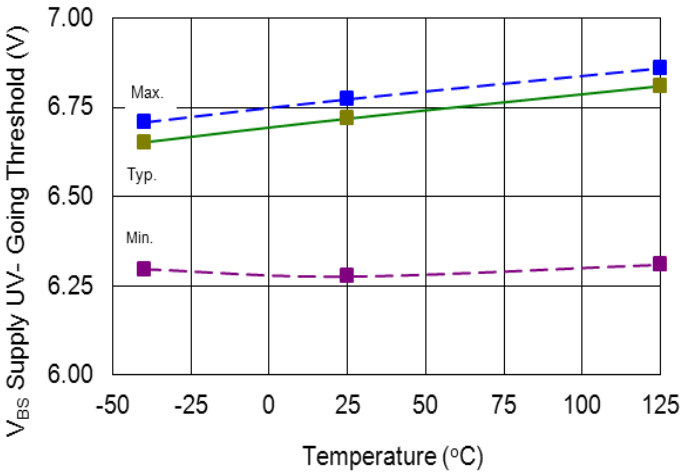
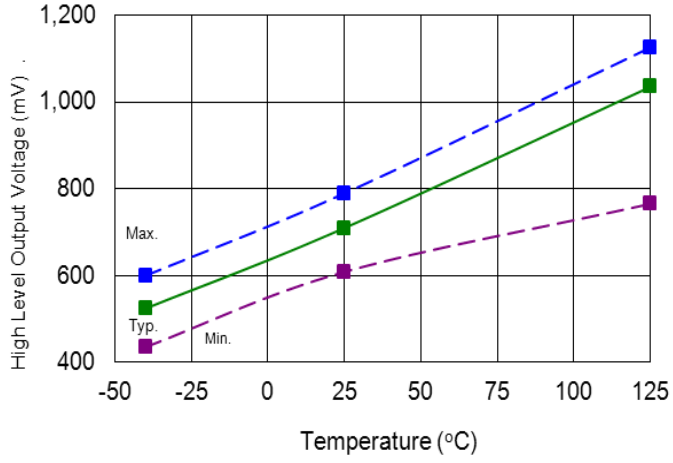


Figure 35. VBS UV- Going Threshold vs. Temperature



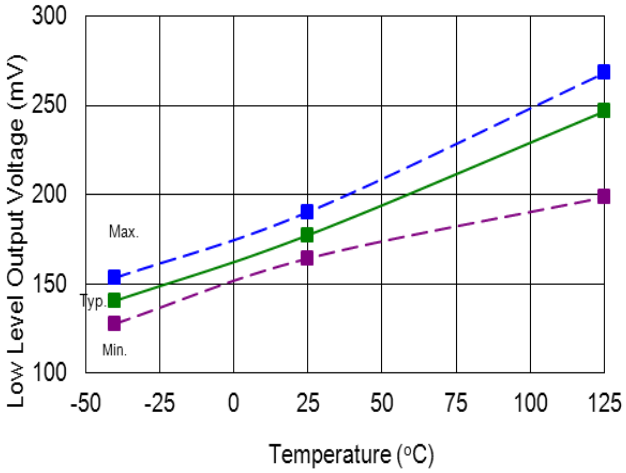


Figure 36. High Level Output Voltage vs. Temperature
Io = 20mA

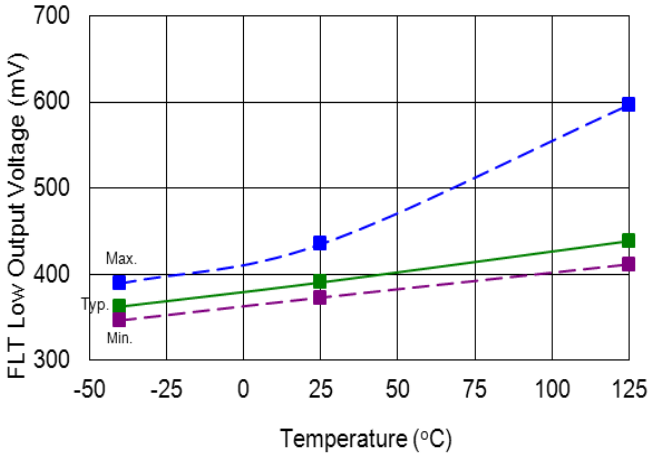


Figure 37. Low Level Output Voltage vs. Temperature
Io = 20mA

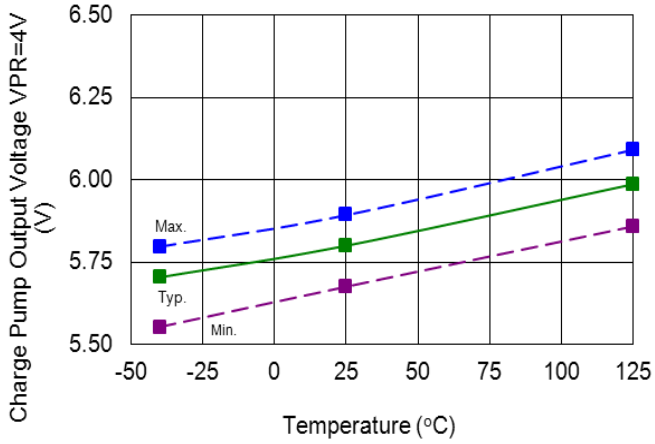
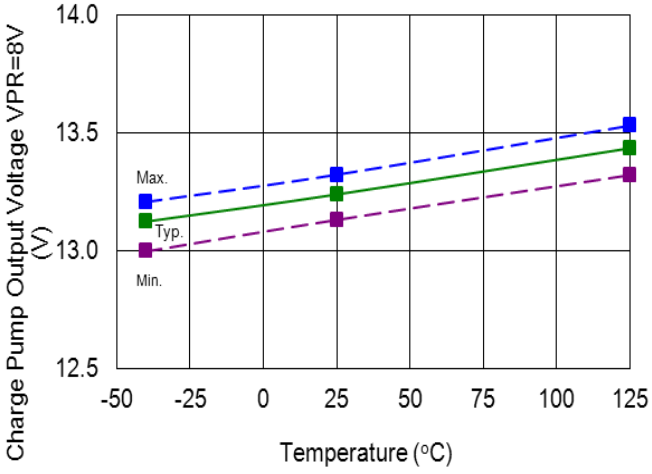


Figure 38. FLT Low Output Voltage vs. Temperature

Figure 39. Charge Pump Output Voltage vs. Temperature
VPR = 4V



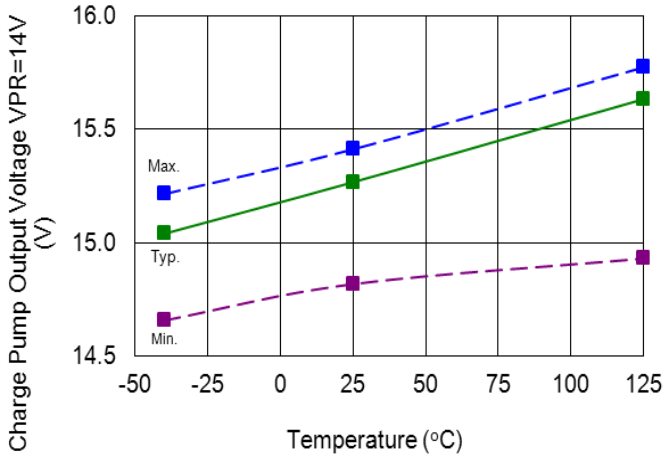
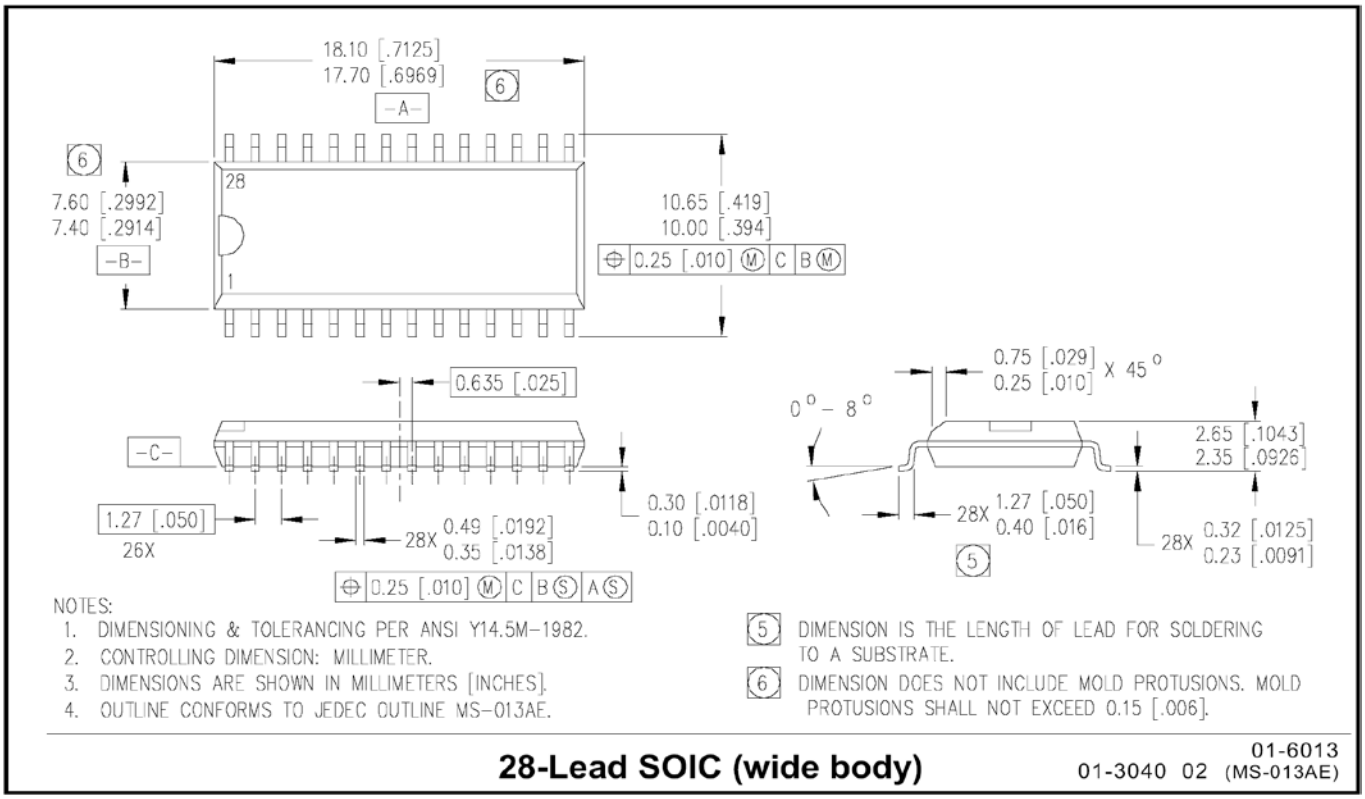


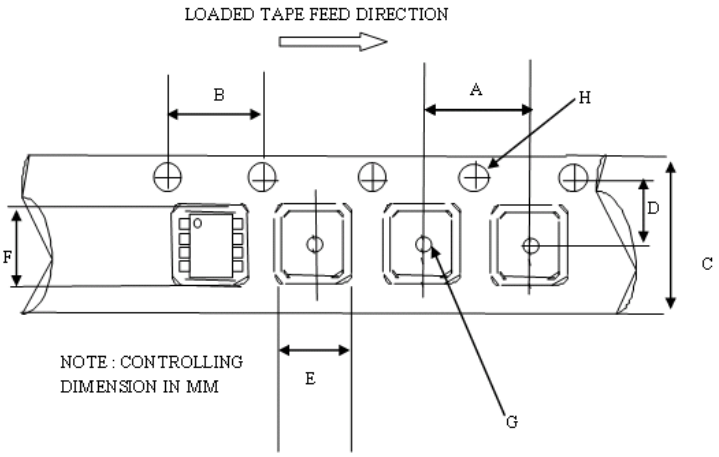
Figure 40. Charge Pump Output Voltage vs. Temperature
VPR = 8V

Figure 41. Charge Pump Output Voltage vs. Temperature
VPR = 14V

Package Details:

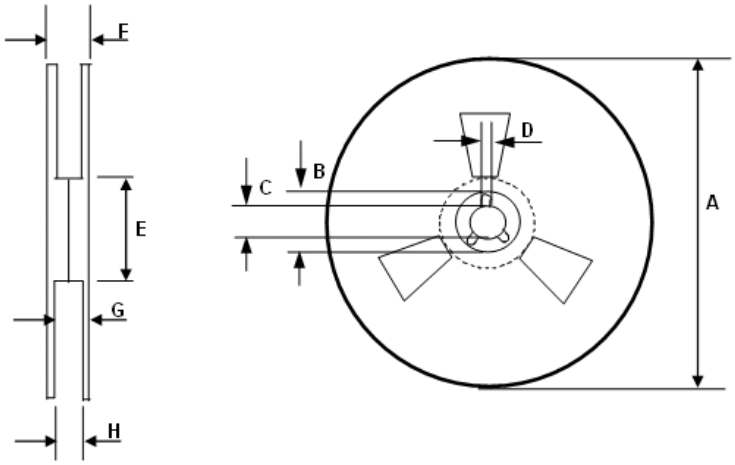


Tape and Reel Information



CARRIER TAPE DIMENSION FOR 28SOICW

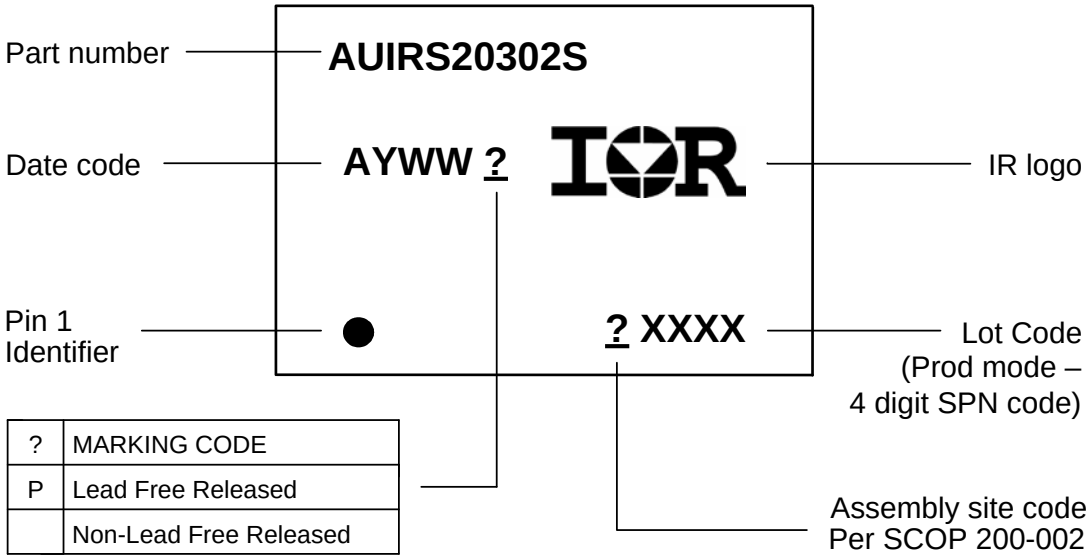
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	18.20	18.40	0.716	0.724
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 28SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS20302S	SOIC28W	Tube/Bulk	25	AUIRS20302S
		Tape and Reel	1000	AUIRS20302STR

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Revision History

Date	Comment
Nov 20th, 2010	DR2 format and revision (Preliminary)
March 14th 2011	Note 2 at page 5 modified ("UVPR is latched") and moved under st el char table.
August 31, 2011	Added AU qualified, Leadfree, RoSH; revised Qualification level table; added tri-temp graphs; modified part marking graph; revise Notice page to the latest version.
Sep 13th, 2011	Abs Max Rat: COM limits set to -5V..5V; Max Oper Junc temp=150^C; static El Char: Voffset min=-33mV. Fig4 and Fig5 and Fig6 change.
Sep 14th, 2011	Added AU qualified, leadfree RoSH; removed preliminary; revised DT condition VPR=15V
May 2nd, 2014	Update ESD protection scheme on page 9, pins CAn and CAp

