

DIP-GAM

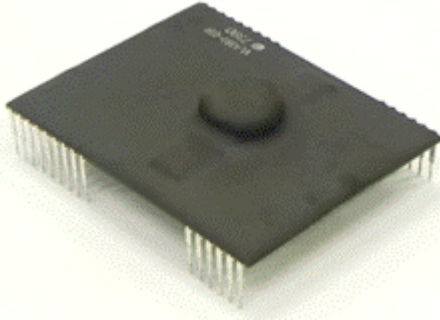
PRELIMINARY

<Dual-In-Line Package Gate Amp Module>

VLA591-01R

DRIVER FOR IGBT MODULES

VLA591-01R



FEATURES

- Low height, DIP structure
- Dual gate drive circuits
- Built in high isolation voltage digital isolators
- Built in isolated DC-DC converter for gate drive
- Built in short circuit protection with soft gate shut down
- Adjustable fall time on activity of short circuit protection
- Output peak gate current is +/-20A(max)
- Isolation voltage is 4000Vrms (for 1 minute)
- CMOS compatible input interface (Input high active type)
- Low voltage lock out for gate power supply(VCC)

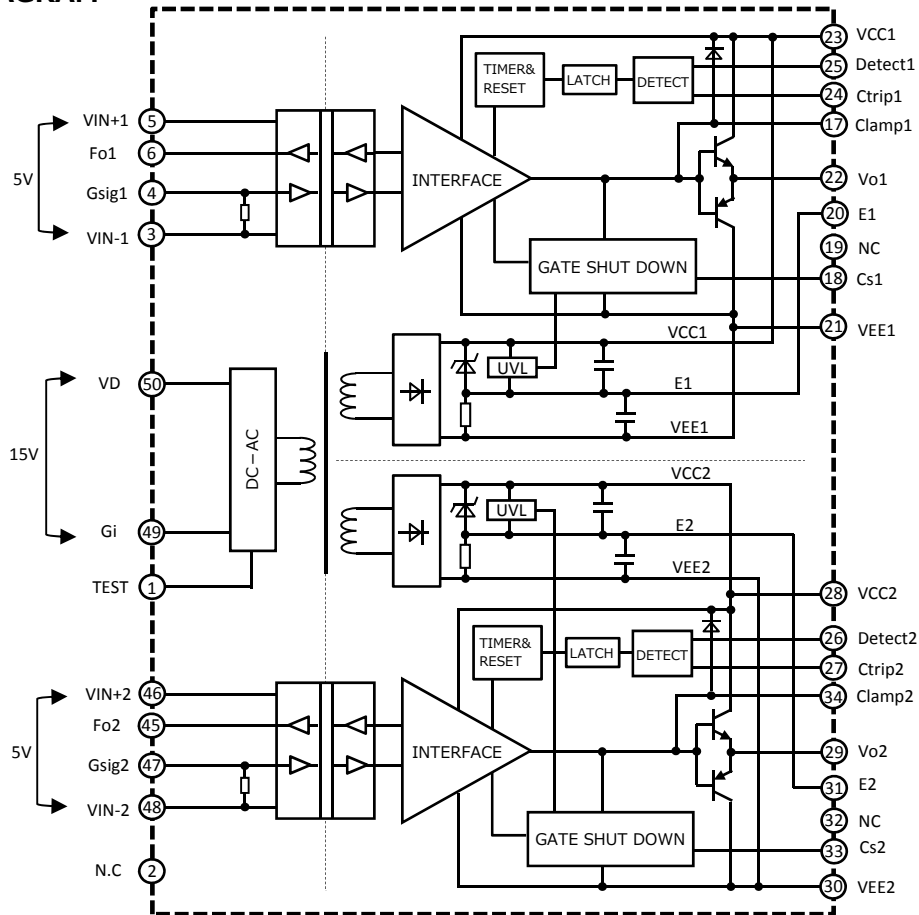
TARGETED IGBT MODULES

- $V_{CES} = 600V$ series up to 600A class
- $V_{CES} = 1200V$ series up to 1400A class
- $V_{CES} = 1700V$ series up to 1400A class

APPLICATIONS

To drive IGBT modules for inverter or AC servo system application

BLOCK DIAGRAM



* 1pin: Test pin (Not to be connected electrically to other line)

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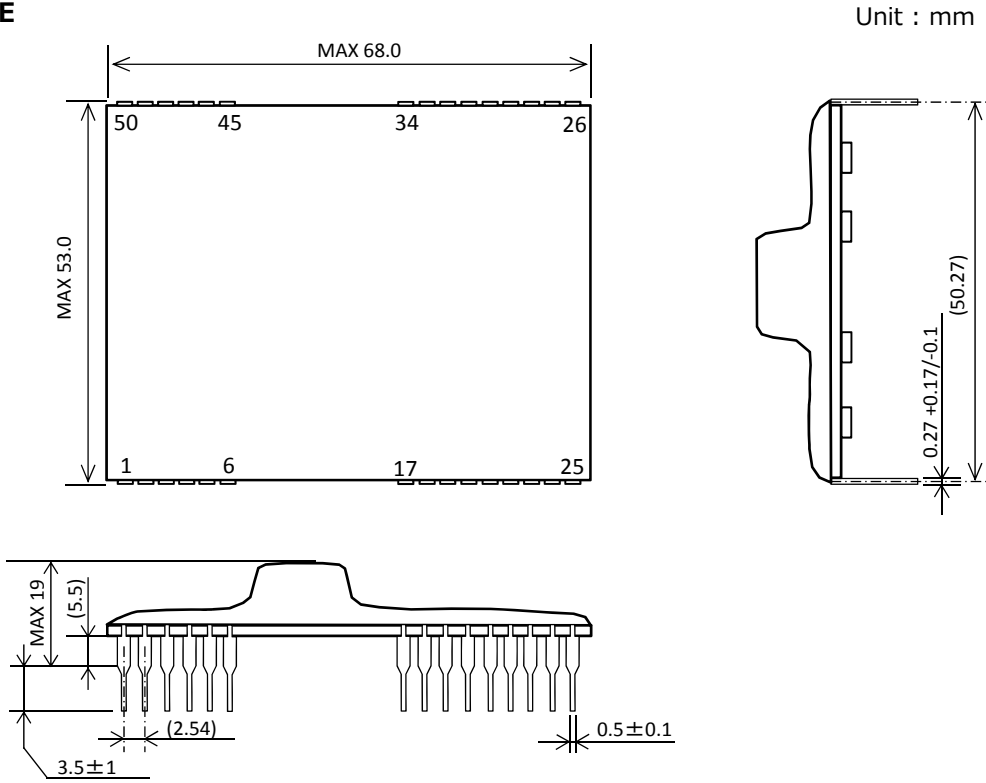
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<Dual-In-Line Package Gate Amp Module>

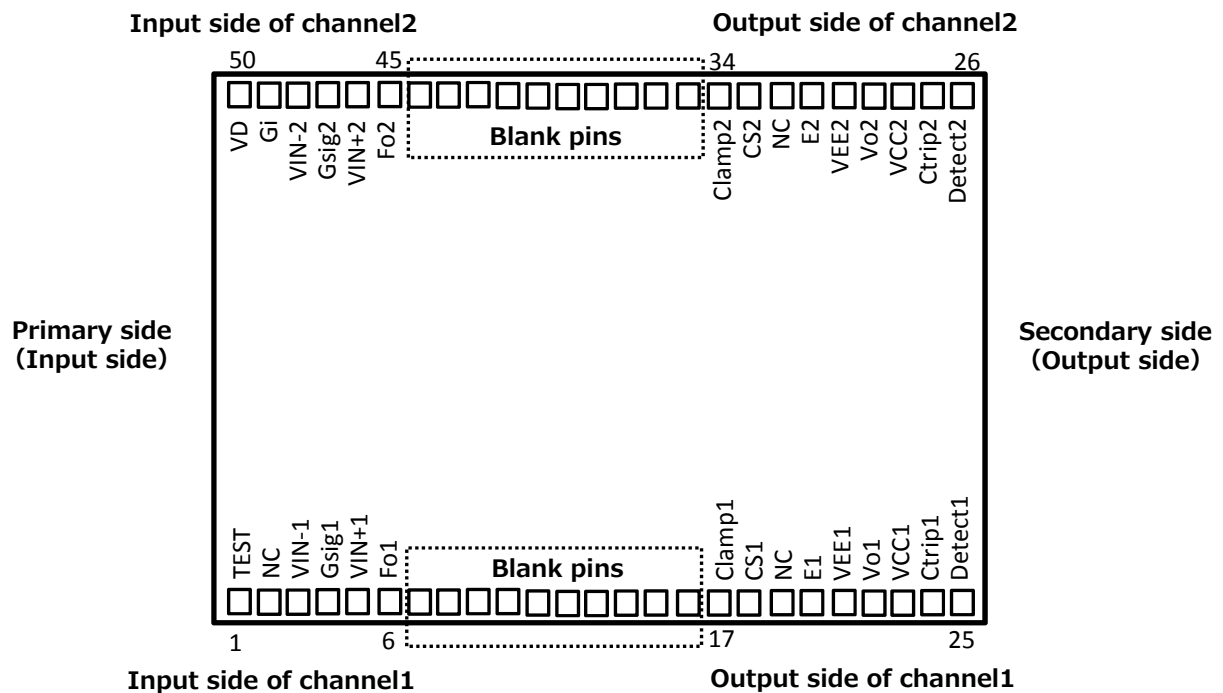
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OUTLINE



PIN ASSIGNMENT



DIP-GAM**PRELIMINARY****VLA591-01R**

DRIVER FOR IGBT MODULES

MAXIMUM RATINGS (Unless otherwise noted, Ta=25 °C)

| Symbol | Item | Conditions | Ratings | Unit |
|--------|---|---|------------|------|
| VD | Supply voltage | Between VD and Gi | 16.5 | V |
| VIN | Supply voltage for gate signal | Between VIN+ and VIN- | 6 | V |
| V_Gsig | Gate signal voltage | Between Gsig and VIN- | VIN+0.5 *1 | V |
| IOHP | Output peak current | Pulse width 3us | -20 | A |
| IOLP | | | 20 | A |
| Viso1 | Isolation voltage between primary and secondary | Sine wave voltage, 60Hz, 1minute | 4000 | Vrms |
| Viso2 | Isolation voltage between each output | Sine wave voltage, 60Hz, 1minute | 4000 | Vrms |
| Tc | Case temperature | Surface temperature of the exterior resin | 110 | °C |
| Topr | Operating temperature | No condensation allowable | -40 ~ 85 | °C |
| Tstg | Storage temperature | No condensation allowable | -40 ~ 90 | °C |
| IFo | Fault output current | Applied Fo pin | +/-10 | mA |
| VR_Det | Input voltage at Detect pin | Applied Detect pin | 80 | V |
| Idrive | Gate drive current | Gate average current (Total of 2 drive circuits) *Keep case temperature less than 110 °C | 200 | mA |

*1 Maximum voltage must not exceed 6V.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta=25°C, VD=15V, VIN=5V, RG=1.5Ω)

| Symbol | Item | Conditions | Limits | | | Unit |
|-----------|--|---|--------|------|------|------|
| | | | Min | Typ | Max | |
| VD | Supply voltage | Recommended range | 14.5 | 15 | 15.5 | V |
| VIN | Supply voltage for gate signal | Recommended range | 4.75 | 5 | 5.25 | V |
| V_Gsig | Gate signal voltage | Recommended range | 3.5 | - | VIN | V |
| f | Switching frequency | Recommended range Keep total gate average current less than 200mA | - | - | 50 | kHz |
| RG | Gate resistance | Recommended range | 0.5 | - | - | Ω |
| IFo | Fault output current | Recommended range | -4 | - | 4 | mA |
| VCC | VCC voltage | - | - | 16.4 | - | V |
| VEE | VEE voltage | - | - | -9 | - | V |
| η | Gate supply efficiency | 2 circuits total load current between VCC and VEE is 200mA | 62 | 70 | - | % |
| VOH | "H" output voltage | Input "H" (High active) | 13.5 | 15.2 | 16.5 | V |
| VOL | "L" output voltage | Input "L" (High active) | -6 | -8 | -11 | V |
| tPLH | "L-H" propagation time | RG=1.5Ω, f=10kHz, C_load:0.33uF | - | 0.29 | - | us |
| tr | "L-H" rise time | RG=1.5Ω, f=10kHz, C_load:0.33uF | - | 0.52 | 0.65 | us |
| tPHL | "H-L" propagation time | RG=1.5Ω, f=10kHz, C_load:0.33uF | - | 0.15 | - | us |
| tf | "H-L" fall time | RG=1.5Ω, f=10kHz, C_load:0.33uF | - | 0.12 | 0.25 | us |
| ttimer | Timer | Between start and cancel of protection (Under input signal is off state) | 1 | - | 2 | ms |
| VFoL | Fo "L" output voltage | Pull up resistor 4.7kΩ to 5V (1mA sink) | - | 0.1 | 0.2 | V |
| ttrip1 | Masked time detect short circuit1 | Detect pin:over than15V, Ctrip pin:open | - | 2.9 | - | us |
| ttrip2 | Masked time detect short circuit2 *2 | Detect pin:over than15V, Between Ctrip and E pin:capacitor 47pF | - | 3.7 | - | us |
| VSC | SC detect voltage | Collector voltage of IGBT | 15 | - | - | V |
| UVLO+_VCC | Under voltage lock out (Operation start) | VCC voltage | - | 12.6 | - | V |
| UVLO-_VCC | Under voltage lock out (Operation stop) | VCC voltage | - | 11.7 | - | V |

*2 Length of wiring of capacitor masked time detect short-circuit is within 5cm from E and Ctrip pins coming and going

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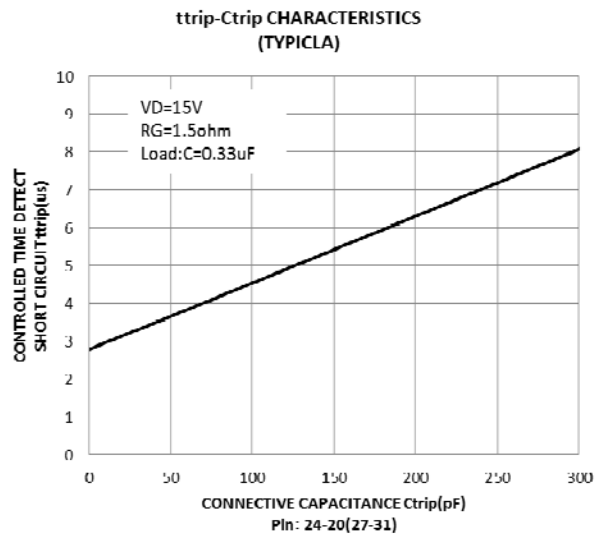
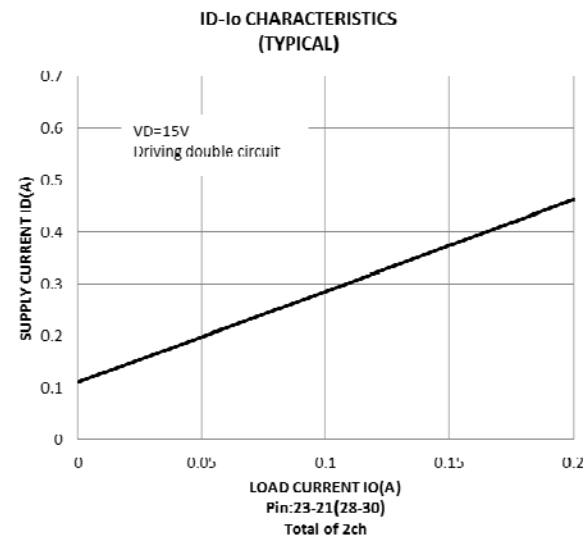
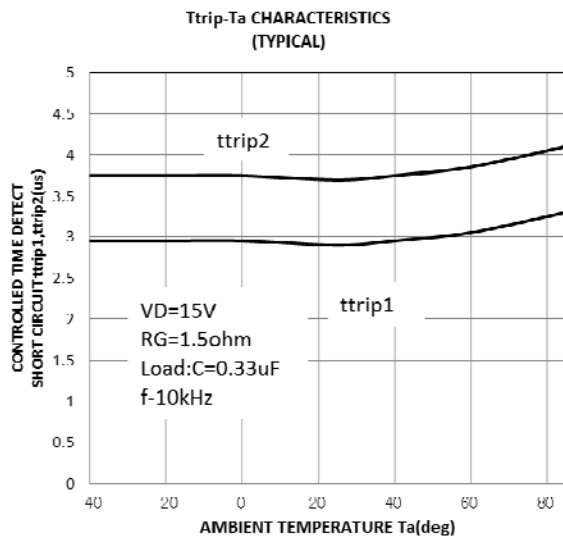
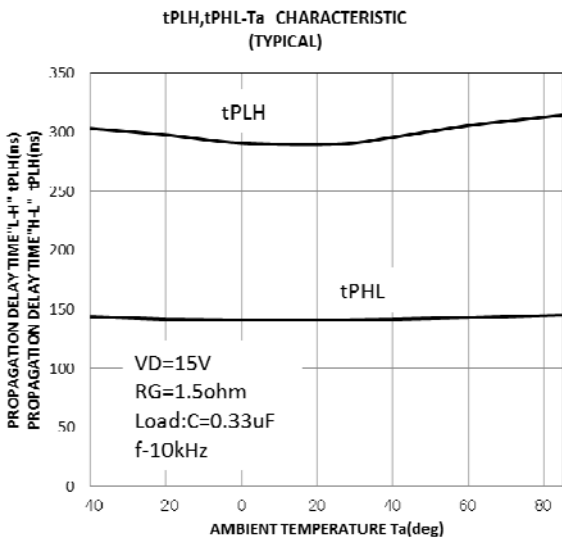
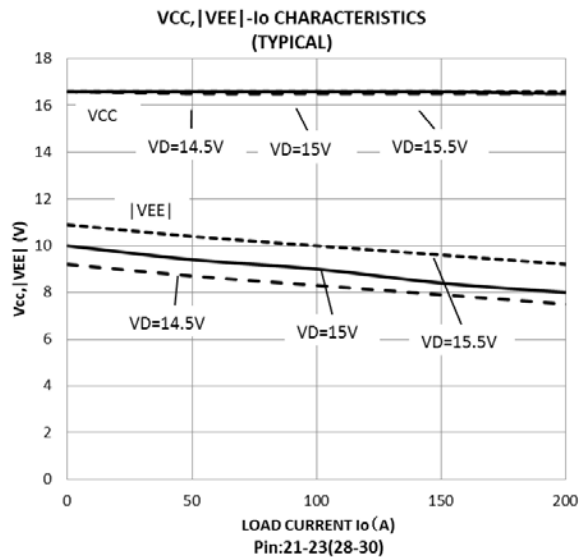
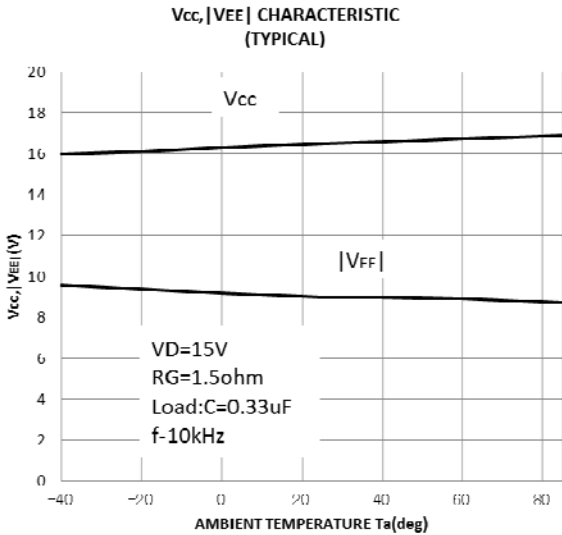
VLA591-01R

DRIVER FOR IGBT MODULES

PERFORMANCE CURVES

(Unless otherwise noted, Ta=25deg, VD=15V, RG=1.5 ohm, driving only single circuit)

(ID: Input current for power supply, Idrive: gate average current, Io: DC load)



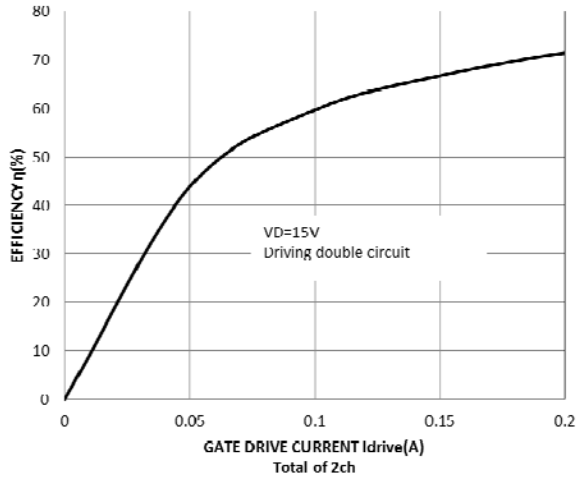
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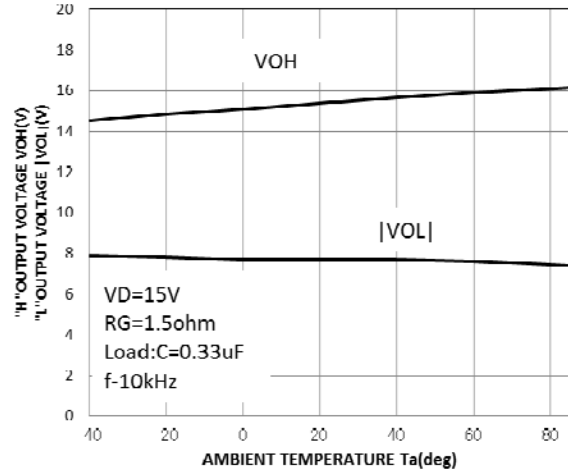
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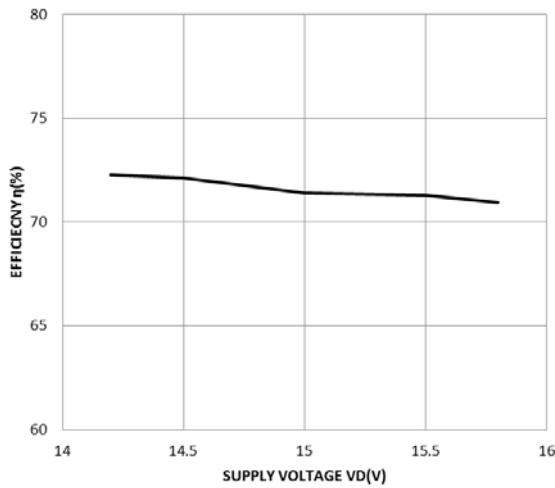
η -I_{drive} CHARACTERISTICS
(TYPICAL)



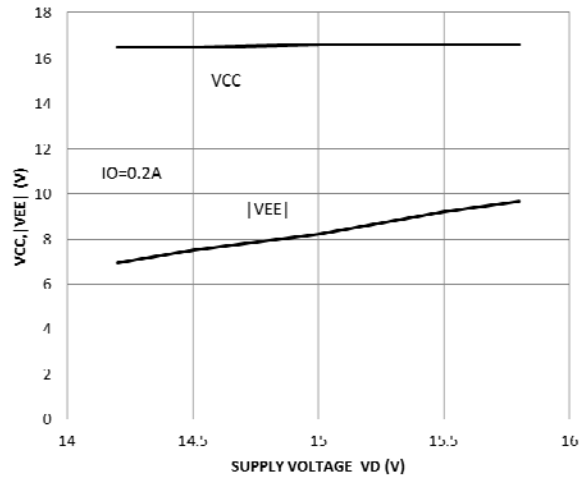
VOH, |VOL| -Ta CHARACTERISTICS
(TYPICAL)



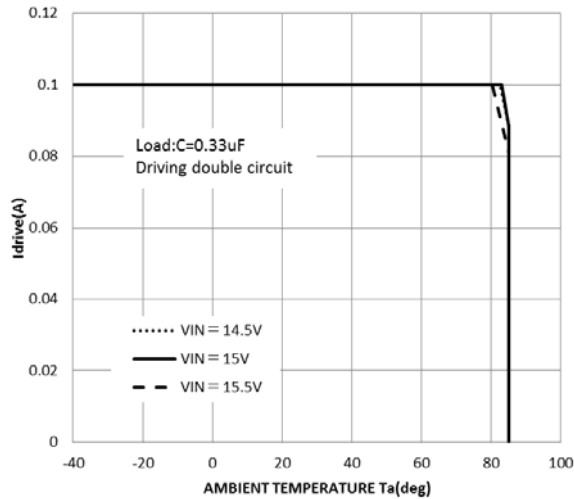
η -VD CHARACTERISTICS
(TYPICAL)



VCC, |VEE| -VD CHARACTERISTICS
(TYPICAL)



DERATING CHARACTERISTICS



DIP-GAM

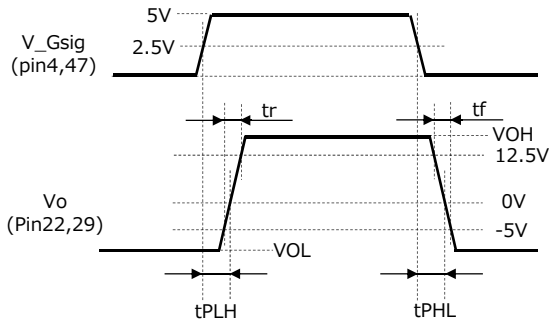
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DRIVER FOR IGBT MODULES

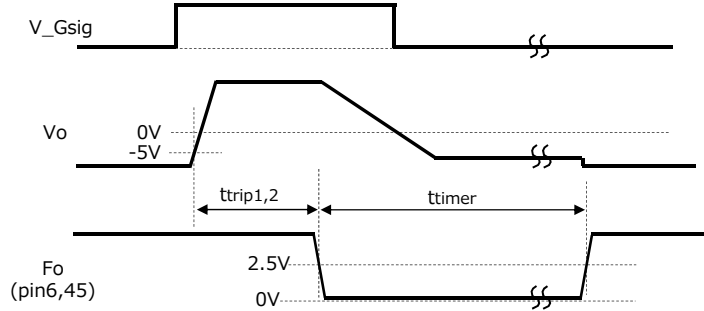
DEFINITION OF CHARACTERISTICS

SWITCHING OPERATION

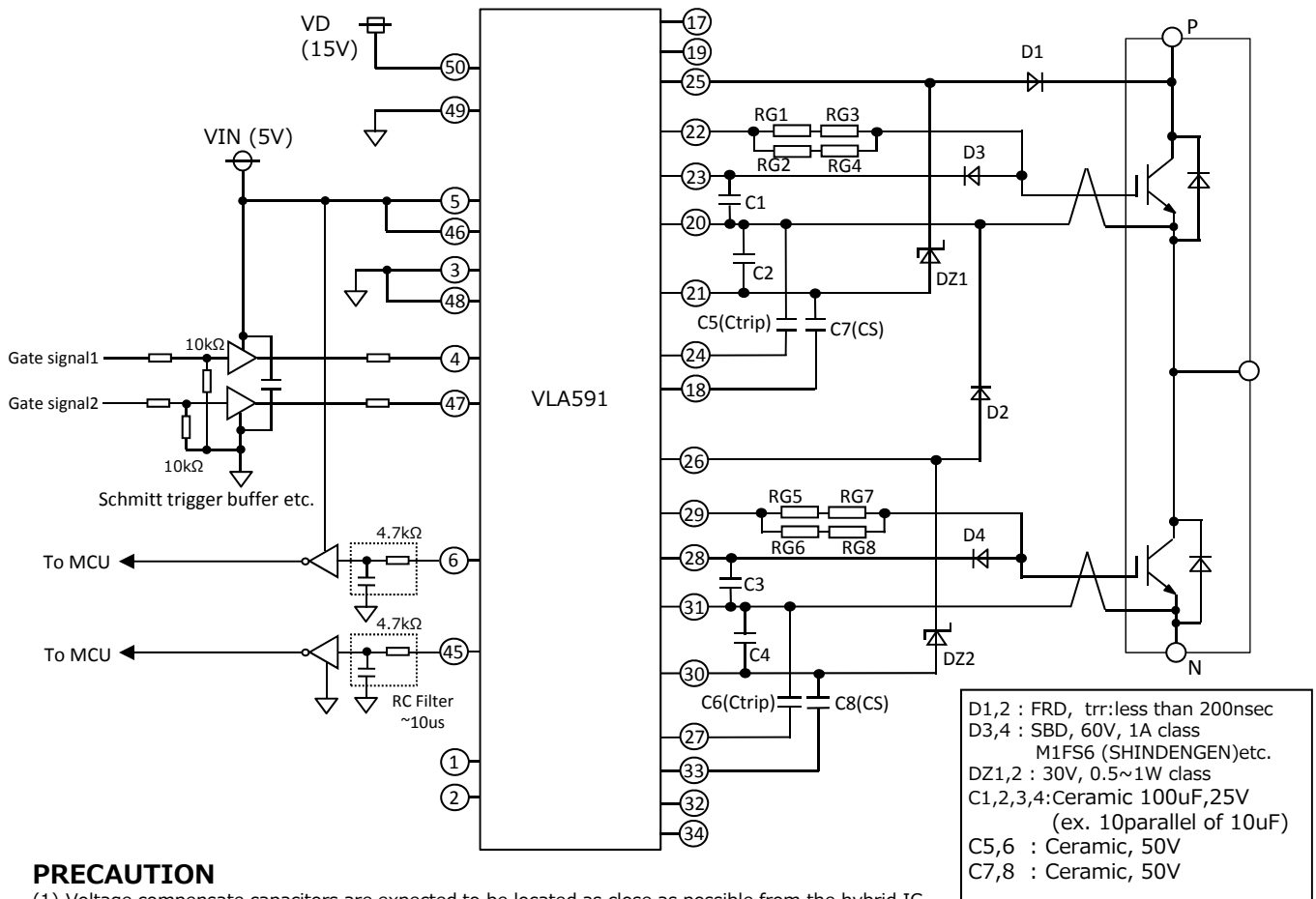


*RG=1.5Ω, C_load:0.33uF, f=10kHz, ON Duty=50%

OPERATION OF SHORT CIRCUIT PROTECTION



APPLICATION EXAMPLE



PRECAUTION

- (1) Voltage compensate capacitors are expected to be located as close as possible from the hybrid IC.
- (2) D1,2 require approximately the same voltage of IGBT modules.
- (3) If reverse recovery time of D1 (2) is long, pin25 (26) is applied high voltage. In that case, counterplan for protection which insert zener diode between pin 25 and 21 (pin 26 and 30) is necessary like above diagram.
- (4) In case pin 24 or 27 are operating, the Ctrip is expected to be wired as close as possible from pin. (Less than 5cm coming and going) In case of not using, please keep pin 24 or 27 open.
- (5) Minimize the area of closed circuit of gate circuit and input gate signal circuit so as not to be affected by induction noise.
- (6) When the built in short-circuit protection circuit need not be used, please connect resistance of 4.7k(1/4W) between pin 25 and 20 (pin 26 and 31). At that time, D1 (D2) and Dz1 (DZ2) are not require.
- (7) Pin1 is Test pin. Please not to be connected electrically to other line.
- (8) Please keep pin17 and 34 open ordinarily. These pins are exclusive to our specific product.
- (9) Please keep total gate average current less than maximum rating.
- (10) About the IC which drives gate signal on input side, it is not recommended to use the one whose output is open collector or open drain type.

DIP-GAM

PRELIMINARY

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DRIVER FOR IGBT MODULES

OPERATION OF PROTECTION CIRCUIT

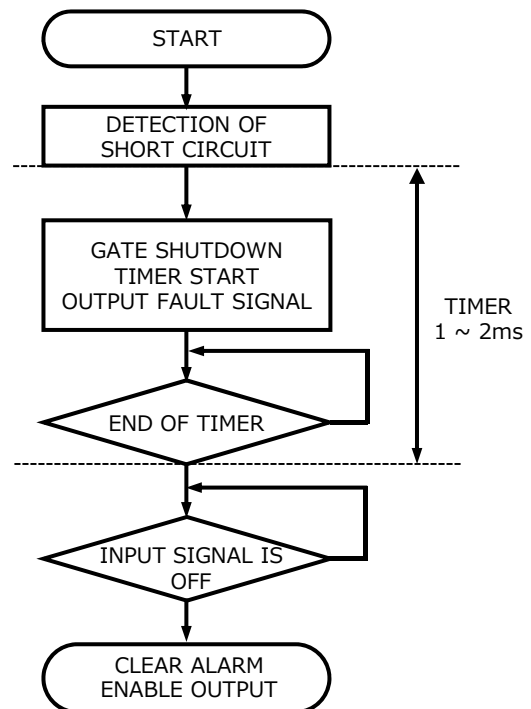
- (1) In case the gate voltage is "H" and the collector voltage is high, this hybrid IC will recognize the circuit as short circuit and immediately reduce the gate voltage. Besides, put out error signal ("L") which inform that protection circuit is operating at the same time from pin 6 or 45.
- (2) The protection circuit reset and resort to ordinary condition if input signal is "OFF" when the premised 1~2msec passed. ("OFF" period needs 10us or more)
- (3) When the output rises, the masked time detect short circuit (ttrip) is set up so that on-time of IGBT can be secured properly.
It is possible to adjust that time by connecting the capacitor (Ctrip) between pin24 and 20 (27 and 31).
- (4) When the short circuit protection works, the soft gate shut down circuit works to suppress collector surge voltage of IGBT. Furthermore, when it is necessary to be more soft, by adding a capacitor between Cs and VEE terminals, it is possible to make gate shut down speed more slow.

LATCH & TIMER RESET SYSTEM IN SHORT-CIRCUIT PROTECTION CIRCUIT

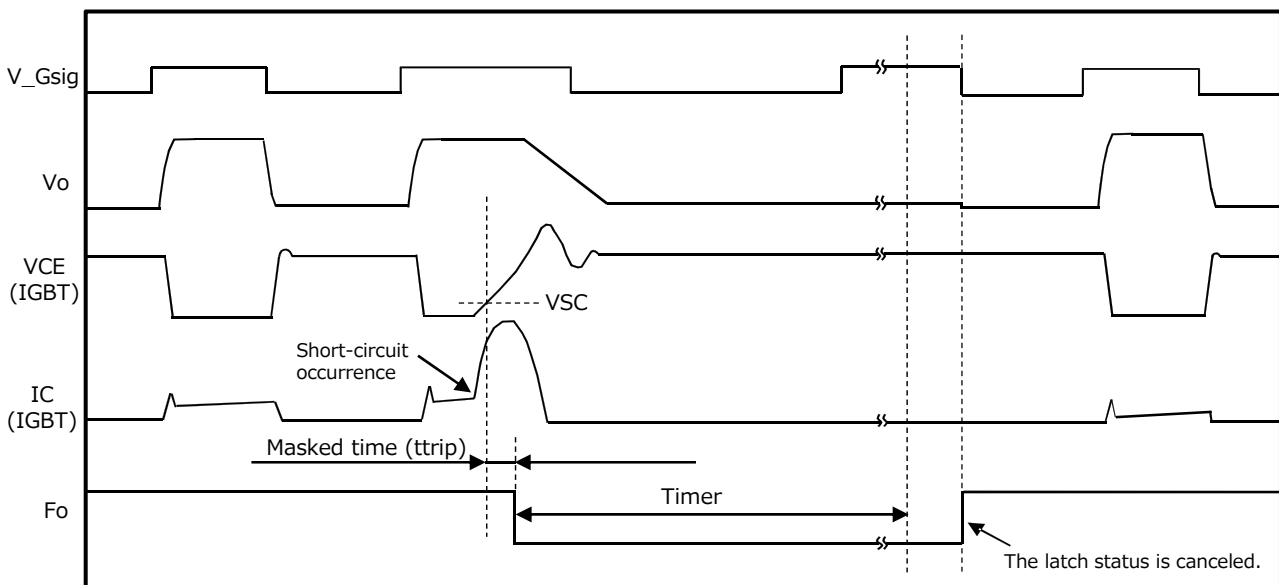
Once the short-circuit protection circuit starts, it shuts down the gate output and keeps alarm output, causing the latch status. This status is canceled if the input signal is OFF when specific time elapses after the activation of the short-circuit protection circuit. Then, gate output depending on input signals becomes possible. If the input signal is ON when specific time elapses, the latch status is not canceled: it is canceled when the signal becomes OFF.

As mentioned above, on the latch & timer reset system, the latch status is resulted after activation of the protection circuit and shutdown of the gate output. Therefore, during this period, gate output is not made no matter how much input signals are received. For this reason, it is possible to safely stop the entire equipment by sending error signals to the microcomputer during this period to stop all gate signals.

OPERATION FLOW ON DETECTING SHORT CIRCUIT



TIMING CHART



FOR SAFETY USING

Great detail and careful attention are given to the production activity of Hics, such as the development, the quality of production, and in it's reliability. However the reliability of Hics depends not only on their own factors but also in their condition of usage. When handling Hics, please note the following cautions.

| CAUTIONS | |
|------------------|---|
| Packing | The materials used in packing Hics can only withstand normal external conditions. When exposed to outside shocks, rain and certain environmental contaminators, the packing materials will deteriorates. Please take care in handling. |
| Carrying | <ol style="list-style-type: none"> 1) Don't stack boxes too high. Avoid placing heavy materials on boxes. 2) Boxes must be positioned correctly during transportation to avoid breakage. 3) Don't throw or drop boxes. 4) Keep boxes dry. Avoid rain or snow. 5) Minimal vibration and shock during transportation is desirable. |
| Storage | <p>When storing Hics, please observe the following notices or possible deterioration of their electrical characteristics, risk of solder ability, and external damage may occur.</p> <ol style="list-style-type: none"> 1) Devices must be stored where fluctuation of temperature and humidity is minimal, and must not be exposed to direct sunlight. Store at the normal temperature of 5 to 30 degrees Celsius with humidity at 40 to 60%. 2) Avoid locations where corrosive gasses are generated or where much dust accumulates. 3) Storage cases must be static proof. 4) Avoid putting weight on boxes. |
| Extended storage | When extended storage is necessary, Hics must be kept non-processed. When using Hics which have been stored for more than one year or under severe conditions, be sure to check that the exterior is free from flaw and other damages. |
| Maximum ratings | To prevent any electrical damages, use Hics within the maximum ratings. The temperature, current, voltage, etc. must not exceed these conditions. |
| Polarity | To protect Hics from destruction and deterioration due to wrong insertion, make sure of polarity in inserting leads into the board holes, conforming to the external view for the terminal arrangement. |

Keep safety first in your circuit designs!

·ISAHAYA Electronics Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (1) placement of substitutive, auxiliary circuits, (2) use of non-flammable material or (3) prevention against any malfunction or mishap.

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