Click here for production status of specific part numbers.

MAX17491

Single-Phase Synchronous MOSFET Driver

General Description

The MAX17491 is a single-phase synchronous noninverting MOSFET driver. The MAX17491 is intended to work with controller ICs like the MAX8736, MAX8786, or MAX17030 in multiphase notebook CPU core regulators.

The regulators can either step down directly from the battery voltage to create the core voltage or step down from the main system supply. The single-stage conversion method allows the highest possible efficiency, while the 2-stage conversion at higher switching frequency provides the minimum possible physical size.

The low-side driver is optimized to drive 3nF capacitive loads with 4ns/8ns typical fall/rise times, and the high-side driver with 8ns/10ns typical fall/rise times. Adaptive dead-time control prevents shoot-through currents and maximizes converter efficiency.

The MAX17491 features improved zero crossing and UVLO performance over the MAX8791/MAX8791B.

The MAX17491 is available in a small, lead-free, 8-pin, 3mm x 3mm TQFN package.

Applications

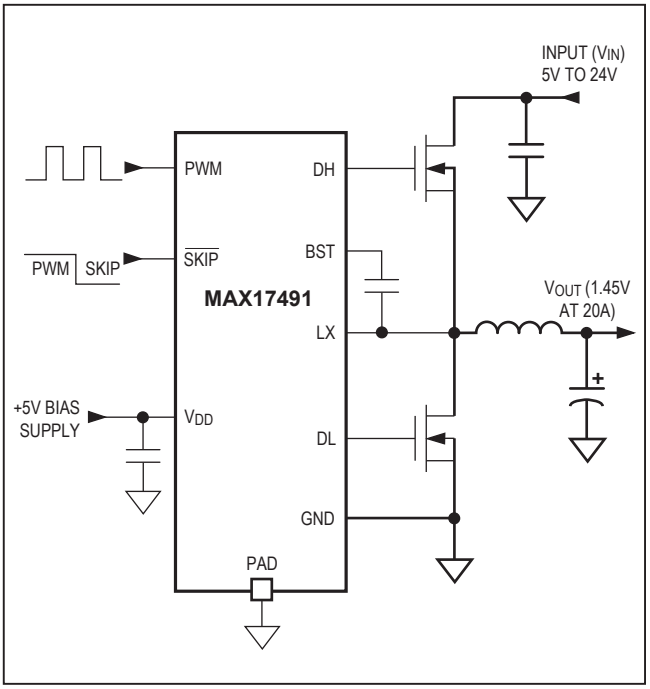
- Notebooks/Desktops/Servers
- CPU Core Power Supplies
- Multiphase Step-Down Converters

Ordering Information appears at end of data sheet.

Features

- Single-Phase Synchronous MOSFET Driver
- 0.5Ω Low-Side On-Resistance
- 0.7Ω High-Side On-Resistance
- 10ns Minimum Guaranteed Dead Time
- Integrated Boost “Diode”
- 2V to 24V Input Voltage Range
- Selectable Pulse-Skipping Mode
- Low-Profile, 3mm x 3mm, TQFN Package

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
$\overline{SKIP}$ to GND .....-0.3V to +6V
PWM to GND.....-0.3V to +6V
DL to GND.....-0.3V to (V_{DD} + 0.3V)
BST to GND .....-0.3V to +36V
DH to LX.....-0.3V to (V_{BST} + 0.3V)
BST to V_{DD} .....-0.3V to +30V
BST to LX.....-0.3V to +6V

Continuous Power Dissipation
8-Pin 3mm x 3mm TQFN
(derate 14.4mW/°C above +70°C) 1150mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 TQFN-EP

Package Code	TQ833+1
Outline Number	21-0136
Land Pattern Number	90-0066
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	69.54°C/W*
Junction to Case (θ_{JC})	17.96°C/W

**Based on JEDEC51-7*

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Circuit of Figure 1, V_{DD} = $V_{\overline{SKIP}}$ = 5V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{DD}		4.20		5.50	V
V_{DD} Undervoltage-Lockout Threshold	$V_{UVLO(VDD)}$	Rising edge, PWM disabled below this level		3.7	4.05	V
		Falling edge, PWM disabled below this level	3.30	3.40	3.75	
Quiescent Supply Current (V_{DD})	I_{DD}	PWM = open; after the shutdown hold time has expired		0.08	0.20	mA
		$\overline{SKIP}$ = GND, PWM = GND, LX = GND (after zero crossing); this state should be equivalent to low-power standby if LX = GND		0.15	0.30	
		$\overline{SKIP}$ = GND or V_{DD}, PWM = V_{DD}, V_{BST} = 5V		0.35	0.70	
DRIVERS						
PWM Pulse Width	$t_{ON(MIN)}$	Minimum on-time		50		ns
	$t_{OFF(MIN)}$	Minimum off-time; required to allow the zero-crossing comparator time to settle to the proper state		300		
DL Propagation Delay	t_{PWM-DL}	PWM high-to-DL low		15		ns

Electrical Characteristics (continued)

(Circuit of Figure 1, V_{DD} = $V_{\overline{SKIP}}$ = 5V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

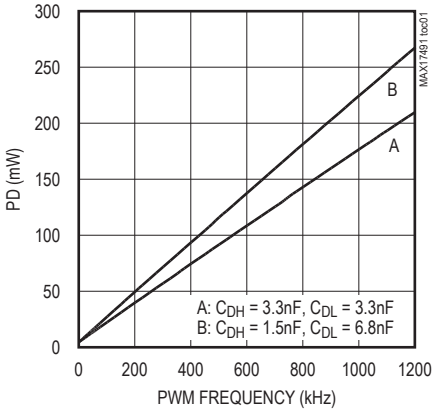
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DH Propagation Delay	t_{PWM-DH}	PWM low-to-DH low			17		ns
DL-to-DH Dead Time	t_{DL-DH}	DL falling to DH rising	T_A = 0°C to +85°C	10			ns
			T_A = -40°C to +105°C	10			
DH-to-DL Dead Time	t_{DH-DL}	DH falling to DL rising	T_A = 0°C to +85°C	10			ns
			T_A = -40°C to +105°C	10			
DL Transition Time	t_{F_DL}	Falling, 3.0nF load			10		ns
	t_{R_DL}	Rising, 3.0nF load			12		
DH Transition Time	t_{F_DH}	Falling, 3.0nF load			8		ns
	t_{R_DH}	Rising, 3.0nF load			10		
DH Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V	DH, high state (pullup)		0.9	2.5	Ω
			DH, low state (pulldown)		0.7	2.1	
DL Driver On-Resistance	$R_{ON(DL)}$	DL, high state (pullup)			0.7	1.6	Ω
		DL, low state (pulldown)			0.3	0.9	
DH Driver Source Current	I_{DH_SOURCE}	DH forced to 2.5V, BST - LX forced to 5V			2.2		A
DH Driver Sink Current	I_{DH_SINK}	DH forced to 2.5V, BST - LX forced to 5V			2.7		A
DL Driver Source Current	I_{DL_SOURCE}	DL forced to 2.5V			2.7		A
DL Driver Sink Current	I_{DL_SINK}	DL forced to 2.5V			8		A
Zero-Crossing Threshold	V_{ZX}	GND - LX, $\overline{SKIP}$ = GND			1.5		mV
Boost On-Resistance	$R_{ON(BST)}$	V_{DD} = 5V, DH = LX = GND (pulldown state), I_{BST} = 10mA			5	8	Ω
PWM Input Levels		High (DH = high, DL = low)		V_{DD} - 0.4			V
		Midlevel		$V_{DD}/2$ - 0.4		$V_{DD}/2$ + 0.4	
		Low (DH = low, DL = high)				0.4	
PWM Input Current	I_{PWM}	Sink; PWM forced to V_{DD}		-370	-200	-110	µA
		Source; PWM forced to GND		110	200	370	
Midlevel Shutdown Hold Time	t_{MID}			120	300	600	ns
$\overline{SKIP}$ Input Threshold		Rising edge			1.7	2.4	V
		Falling edge		0.8	1.5		
$\overline{SKIP}$ Input Current	I_{SKIP}	Sink; $\overline{SKIP}$ forced to 0.8V to V_{DD}, T_A = +25°C		-4	-2	-0.5	µA
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 20°C			+160		°C

Note 1: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed through correlation using statistical-quality-control (SQC) methods.

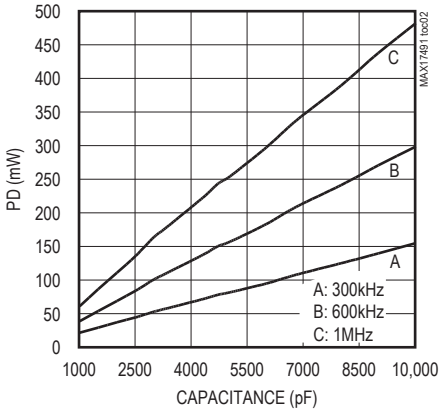
Typical Operating Characteristics

(Circuit of Figure 1, V_{DD} = 5V, C_{DH} = 3nF, C_{DL} = 3nF, T_A = +25°C, unless otherwise noted.)

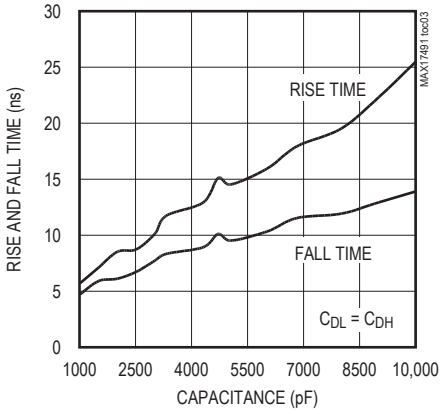
PACKAGE-POWER DISSIPATION vs. PWM FREQUENCY



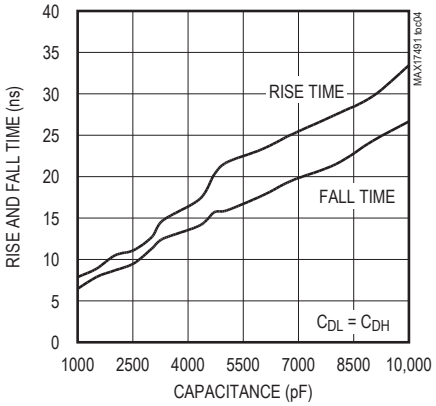
PACKAGE-POWER DISSIPATION vs. CAPACITIVE LOAD ON DH AND DL



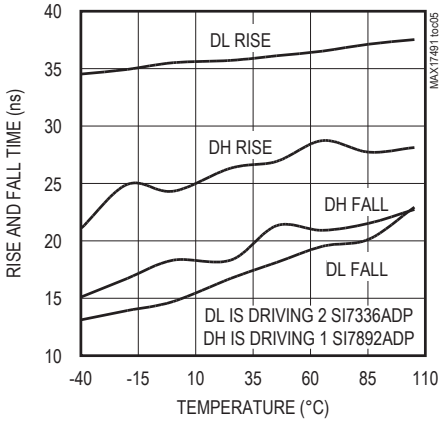
DL RISE AND FALL TIMES vs. CAPACITIVE LOAD



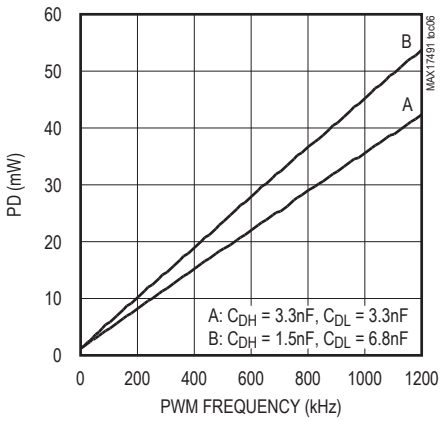
DH RISE AND FALL TIMES vs. CAPACITIVE LOAD



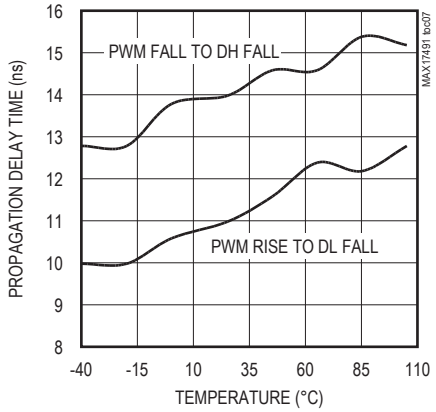
DH AND DL RISE AND FALL TIMES vs. TEMPERATURE



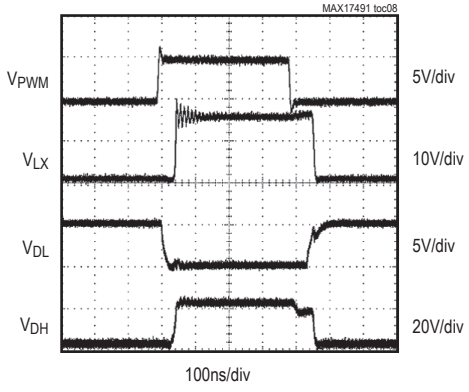
PACKAGE-POWER DISSIPATION vs. PWM FREQUENCY



PROPAGATION DELAY TIME vs. TEMPERATURE



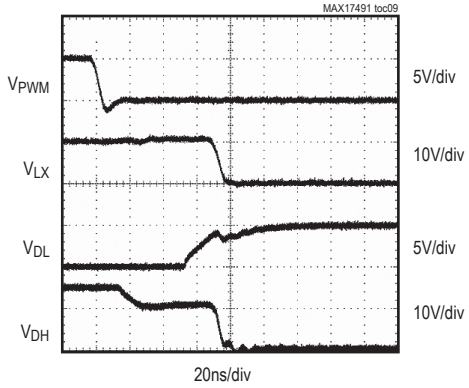
TYPICAL APPLICATION CIRCUIT SWITCHING WAVEFORMS



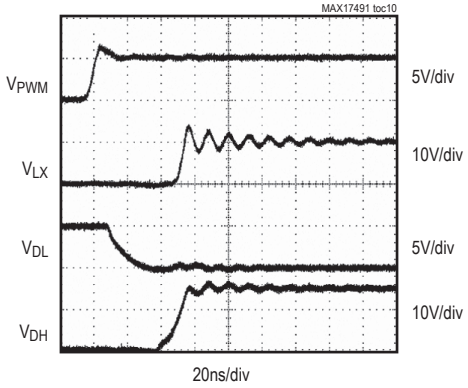
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DD} = 5V, C_{DH} = 3nF, C_{DL} = 3nF, T_A = +25°C, unless otherwise noted.)

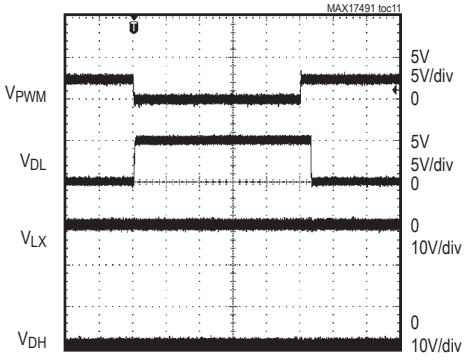
DH FALL AND DL RISE WAVEFORMS



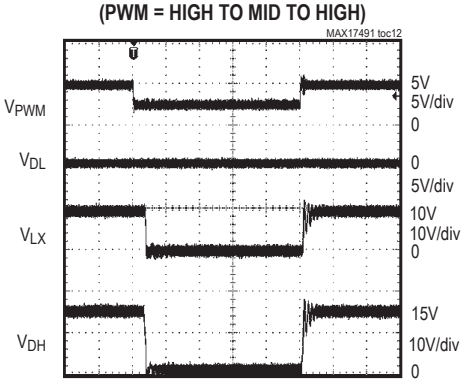
DH RISE AND DL FALL WAVEFORMS



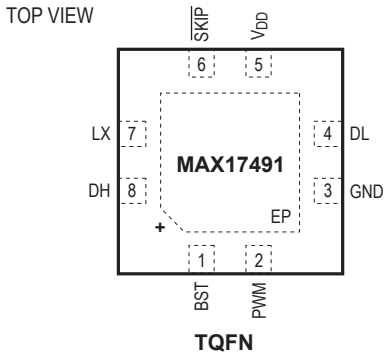
SWITCHING WAVEFORMS (PWM = MID TO LOW TO MID)



SWITCHING WAVEFORMS (PWM = HIGH TO MID TO HIGH)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	BST	Boost Flying-Capacitor Connection. Gate-drive power supply for DH high-side gate driver. Connect a 0.1µF or 0.22µF capacitor between BST and LX.
2	PWM	PWM Input. Noninverting DH control input from the controller IC: Logic-high: DH = high (BST), DL = low (PGND). Midlevel: After the midlevel hold time expires, the controller enters standby mode. DH and DL pulled low. Logic-low: DH = low (LX), DL = high (V_{DD}) when $\overline{SKIP}$ = high. Internal pullup and pulldown resistors create the midlevel and prevent the controller from triggering an on-time if this input is left unconnected (not soldered properly) or driven by a high impedance.
3	GND	Power Ground for the DL Gate Drivers and Analog Ground. Connect exposed pad to GND.
4	DL	PWM Low-Side Gate-Driver Output. Swings between GND and V_{DD}. DL forced high in shutdown.
5	V_{DD}	Supply Voltage Input for the DL Gate Drivers. Connect to 4.2V to 5.5V supply and bypass to GND with a 1µF ceramic capacitor.
6	$\overline{SKIP}$	Active-Low Pulse-Skipping Mode. Enable pulse-skipping mode (zero-crossing comparator enabled) when the driver is operating in SKIP mode: $\overline{SKIP}$ = V_{DD} PWM mode $\overline{SKIP}$ = GND skip mode An internal pulldown current pulls the controller into the low-power pulse-skipping state if this input is left unconnected (not soldered properly) or driven by a high impedance.
7	LX	Switching Node and Inductor Connection. Low-power supply for the DH high-side gate driver. LX connects to the skip-mode zero-crossing comparator.
8	DH	External High-Side n-Channel MOSFET Gate-Driver Output. Swings between LX and BST.
—	EP	Exposed Pad. Connect to ground through multiple vias to reduce the thermal impedance.

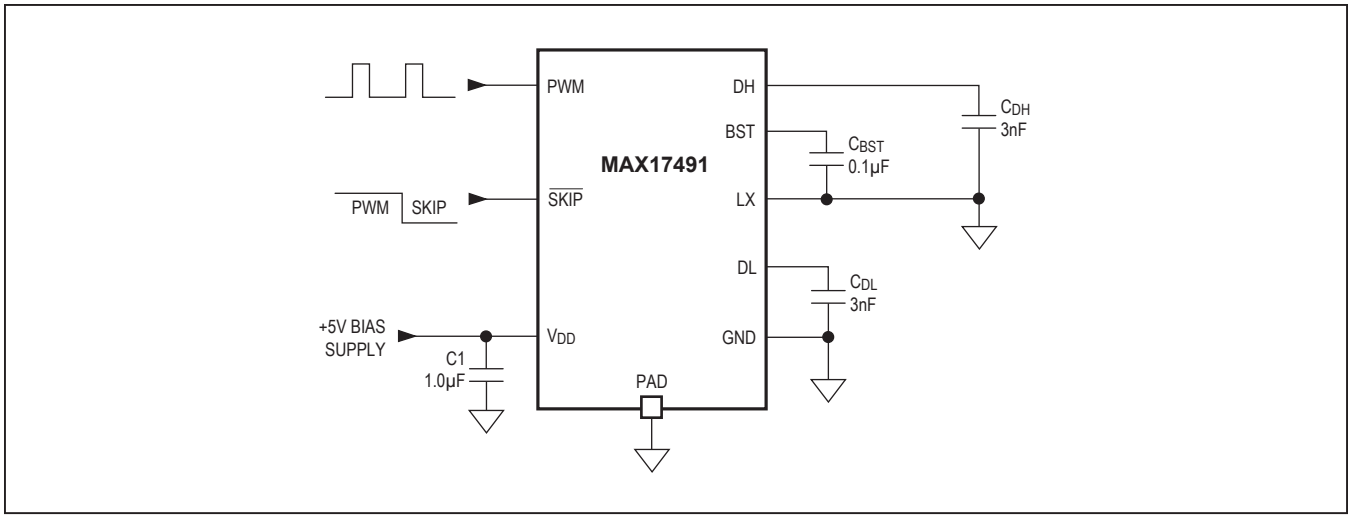


Figure 1. Test Circuit

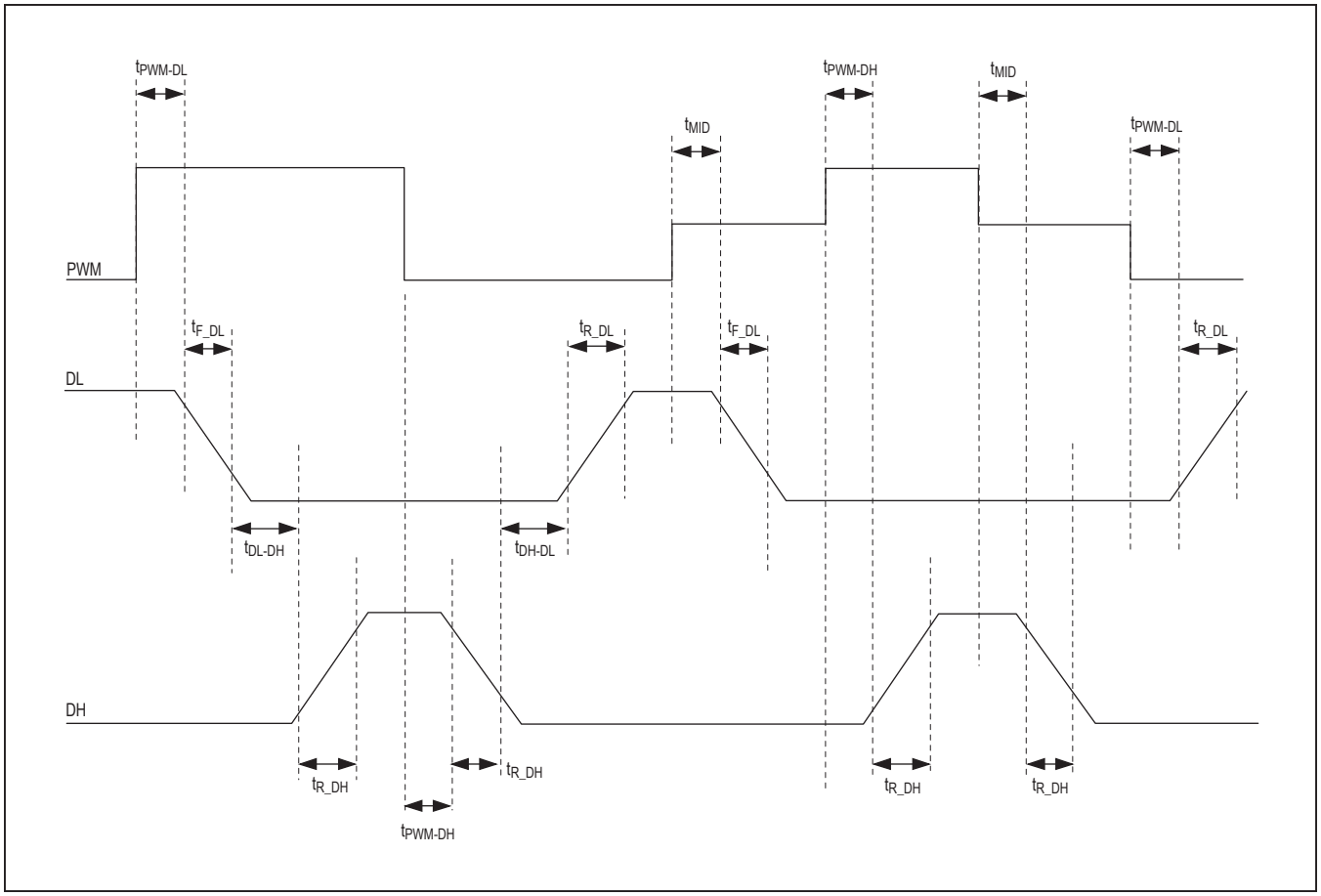


Figure 2. Timing Diagram

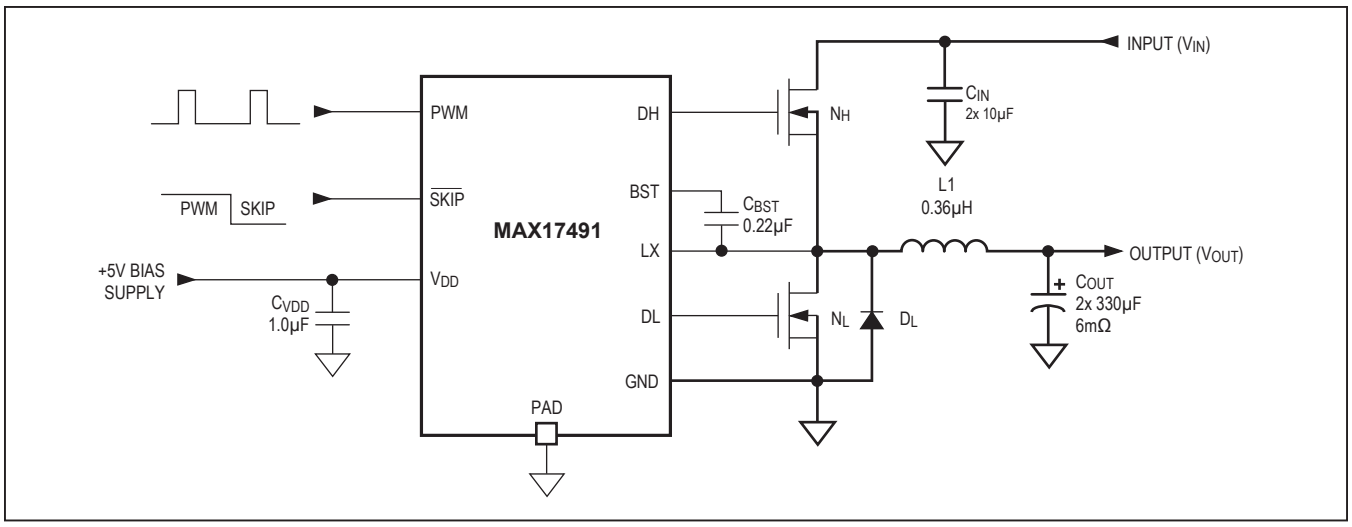


Figure 3. Typical MOSFET-Driver Application Circuit

Table 1. Typical Components

DESIGNATION	QTY	COMPONENT SUPPLIERS
N_H	1 per phase	Siliconix Si4860DY
N_L	1–2 per phase	Siliconix Si4336DY
BST Capacitor (C_{BST})	1 per phase	0.1µF or 0.22µF ceramic capacitor
Schottky Diode	Optional	3A, 40V Schottky diode
Inductor (L1)	1 per phase	0.36µH, 26A, 0.9mΩ power inductor
Output Capacitors (C_{OUT})	1–2 per phase	330µF, 6mΩ per phase
Input Capacitors (C_{IN})	1–2 per phase	10µF, 25V X5R ceramic capacitors

Detailed Description

The MAX17491 single-phase gate driver, along with the MAX8736, MAX8786, or MAX17030 multiphase controllers, provide flexible multiphase CPU core-voltage supplies. The low driver resistance allows up to 7A output peak current. Each MOSFET driver in the MAX17491 can drive 3nF capacitive loads with only 9ns propagation delay and 4ns/8ns (typ) fall/rise times, allowing operation up to 3MHz per phase. Larger capacitive loads are allowable but result in longer propagation and transition times. Adaptive dead-time control prevents shoot-through currents and maximizes converter efficiency while allowing operation with a variety of MOSFETs and PWM controllers. An input undervoltage-lockout (UVLO) circuit allows proper power-on sequencing.

PWM Input

The drivers for the MAX17491 are disabled—DH and DL pulled low—if the PWM input remains in the midlevel window for at least 300ns (typ). Once the PWM signal is driven high or low, the MAX17491 immediately exits the low-current shutdown state and resumes active operation. Outside the shutdown state, the drivers are enabled based on the rising and falling thresholds specified in the *Electrical Characteristics*.

MOSFET Gate Drivers (DH, DL)

The high-side driver (DH) has a 0.9Ω sourcing resistance and 0.7Ω sinking resistance, resulting in 2.2A peak sourcing current and 2.7A peak sinking current with a 5V supply voltage. The low-side driver (DL) has a typical 0.7Ω sourcing resistance and 0.3Ω sinking resistance, yielding 2.7A peak sourcing current and 8A peak sinking current. This reduces switching losses, making the MAX17491 ideal for both high-frequency and high-output-current applications.

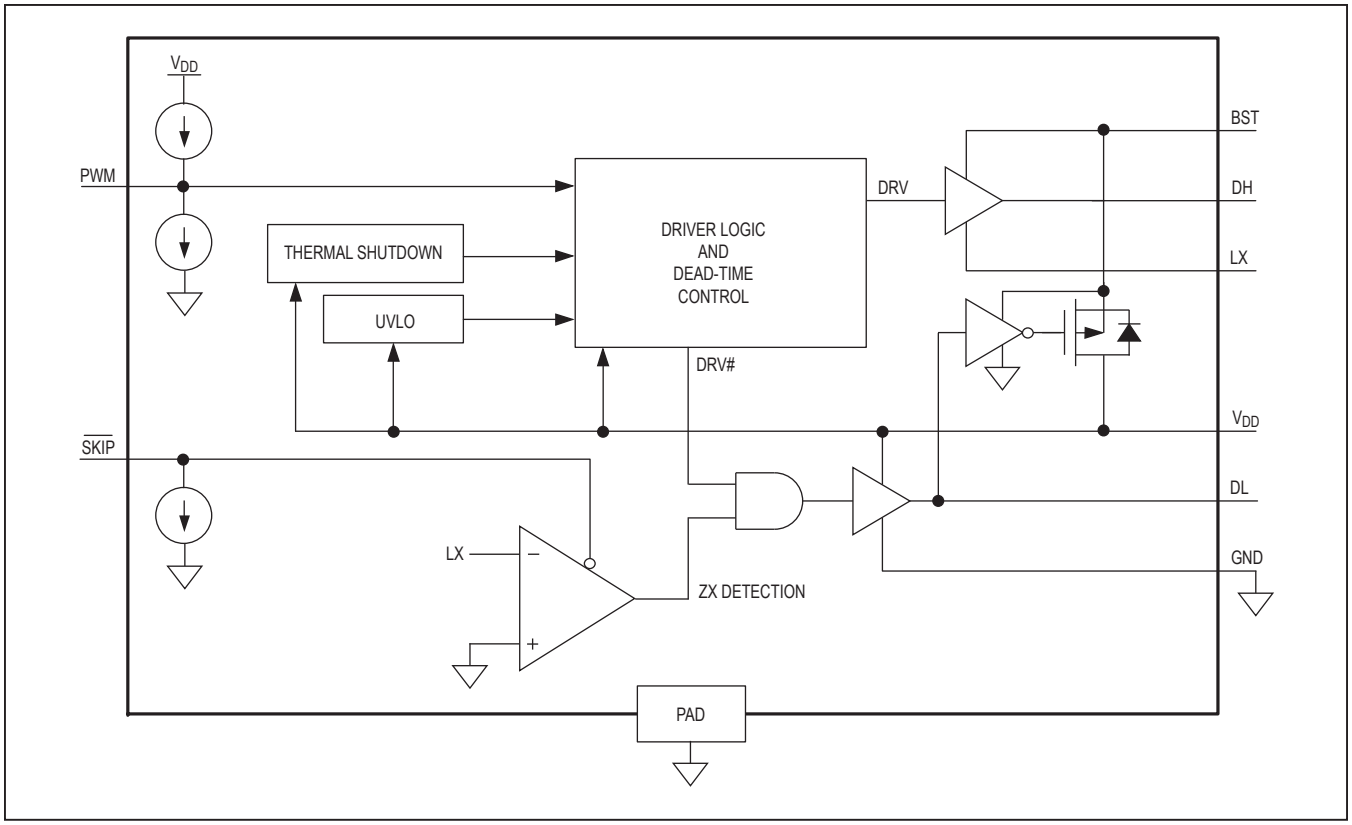


Figure 4. Overview Block Diagram

Adaptive Shoot-Through Protection

The DH and DL drivers are optimized for driving moderately sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. Two adaptive dead-time circuits monitor the DH and DL outputs and prevent the opposite-side FET from turning on until the other is fully off. The MAX17491 constantly monitors the low-side driver output (DL) voltage, and only allows the high-side driver to turn on only when DL drops below the adaptive threshold. Similarly, the controller monitors the high-side driver output (DH) and prevents the low side from turning on until DH falls below the adaptive threshold before allowing DL to turn on.

The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17491 interprets the MOSFET gates as off while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

Internal Boost Switch

The MAX17491 uses a bootstrap circuit to generate the necessary drive voltage to fully enhance the high-side n-channel MOSFET. The internal p-channel MOSFET creates an ideal diode, providing a low voltage drop between V_{DD} and BST.

The selected high-side MOSFET determines appropriate boost capacitance values (C_{BST} in Figure 1), according to the following equation:

$$C_{BST} = Q_{GATE} / \Delta V_{BST}$$

where Q_{GATE} is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver. Choose ΔV_{BST} = 0.1V to 0.2V when determining C_{BST}. The boost flying capacitor should be a low equivalent-series resistance (ESR) ceramic capacitor.

5V Bias Supply (V_{DD})

V_{DD} provides the supply voltage for the internal logic circuits. Bypass V_{DD} with a 1µF or larger ceramic capacitor to GND to limit noise to the internal circuitry. Connect these bypass capacitors as close as possible to the IC.

Input Undervoltage Lockout

When V_{DD} is below the UVLO threshold, DH and DL are held low. Once V_{DD} is above the UVLO threshold and while PWM is low, DL is driven high and DH is driven low. This prevents the output of the converter from rising before a valid PWM signal is applied.

Low-Power Pulse Skipping

The MAX17491 enters into low-power pulse-skipping mode when $\overline{SKIP}$ is pulled low. In skip mode, an inherent automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. A zero-crossing comparator truncates the low-side switch on-time at the inductor current's zero crossing. The comparator senses the voltage across LX and GND. Once V_{LX} - V_{GND} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics*), the comparator forces DL low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value. For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The switching waveforms can appear noisy and asynchronous when light loading activates the pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency.

Applications Information

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention. The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but increasing C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ but reducing C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses. Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D2PAK), and is reasonably priced. Ensure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD(N_H\ RESISTIVE) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

where η_{TOTAL} is the total number of phases. Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package-power dissipation often limits how small the MOSFETs can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics.

The following switching-loss calculation provides only a very rough estimate and is no substitute for prototype evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(N_H\ SWITCHING) = \left(\frac{V_{IN(MAX)} I_{LOAD} f_{SW}}{n_{TOTAL}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN}{}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the high-side MOSFET, and I_{GATE} is the peak gate-drive source/sink current (5A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied due to the squared term in the switching-loss equation above. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at the maximum input voltage:

$$PD(N_L\ RESISTIVE) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy load conditions that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. The MOSFETs must have a good-sized heatsink to handle the overload power dissipation. The heatsink can be a large copper field on the PCB or an externally mounted device.

An optional Schottky diode only conducts during the dead time when both the high-side and low-side MOSFETs are off. Choose a Schottky diode with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time, and a peak current rating higher than the peak inductor current. The Schottky diode must be rated to handle the average power dissipation per switching cycle. This diode is optional and can be removed if efficiency is not critical.

IC Power Dissipation and Thermal Considerations

Power dissipation in the IC package comes mainly from driving the MOSFETs. Therefore, it is a function of both switching frequency and the total gate charge of the selected MOSFETs. The total power dissipation when both drivers are switching is given by:

$$PD(IC) = I_{BIAS} \times 5V$$

where I_{BIAS} is the bias current of the 5V supply calculated in the *5V Bias Supply (V_{DD})* section. The rise in die temperature due to self-heating is given by the following formula:

$$\Delta T_J = \theta_{JA} \times PD(IC)$$

where PD(IC) is the power dissipated by the device, and θ_{JA} is the package's thermal resistance. The typical thermal resistance is 69.54°C/W for the 3mm x 3mm TQFN package.

Avoiding dV/dt Turning on the Low-Side MOSFET

At high input voltages, fast turn-on of the high-side MOSFET can momentarily turn on the low-side MOSFET due to the high dV/dt appearing at the drain of the low-side MOSFET. The high dV/dt causes a current flow through the Miller capacitance (C_{RSS}) and the input capacitance (C_{ISS}) of the low-side MOSFET. Improper selection of the low-side MOSFET that results in a high ratio of C_{RSS}/C_{ISS} makes the problem more severe. To avoid this problem, minimize the ratio of C_{RSS}/C_{ISS} when selecting the low-side MOSFET. Adding a 1Ω to 4.7Ω resistor between BST and C_{BST} can slow the high-side MOSFET turn-on. Similarly, adding a small capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods work at the expense of increased switching losses.

Layout Guidelines

The MAX17491 MOSFET driver sources and sinks large currents to drive MOSFETs at high switching speeds. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PCB layout guidelines are recommended when designing with the MAX17491:

1) Place all decoupling capacitors as close as possible to their respective IC pins.
2) Minimize the length of the high-current loop from the input capacitor, the upper switching MOSFET, and the low-side MOSFET back to the input-capacitor negative terminal.
3) Provide enough copper area at and around the switching MOSFETs and inductors to aid in thermal dissipation.
4) Connect GND of the MAX17491 as close as possible to the source of the low-side MOSFETs.

A sample layout is available in the MAX17030 evaluation kit.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17491GTA+	-40°C to +105°C	8 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—
1	1/20	Updated the Package thermal resistance values.	2, 11

