

## Description

The DGD21064M is a high-voltage / high-speed gate driver capable of driving N-Channel MOSFETs and IGBTs in a half bridge configuration. High-voltage processing techniques enable the DGD21064M's high-side to switch to 600V in a bootstrap operation.

The DGD21064M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The DGD21064M is available in a SO-14 package and operates over an extended -40°C to +125°C temperature range.

## Features

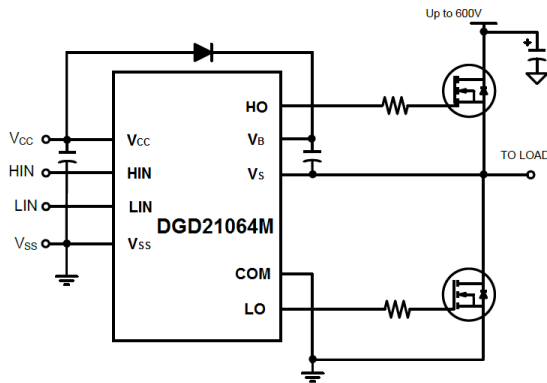
- Floating High-Side Driver in Bootstrap Operation to 600V
- Drives Two N-Channel MOSFETs or IGBTs in Half Bridge Configuration
- Outputs Tolerant to Negative Transients
- Wide Logic and Low-Side Gate Driver Supply Voltage: 10V to 20V
- Wide Logic Supply Voltage Offset Voltage: -5V to 5V
- Logic Input (HIN and LIN) 3.3V Capability
- Schmitt Triggered Logic Inputs with Internal Pull Down
- Undervoltage Lockout for High and Low Side Drivers
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Applications

- DC-DC Converters
- DC-AC Inverters
- AC-DC Power Supplies
- Motor Controls
- Class D Power Amplifiers

## Mechanical Data

- Case: SO-14 (Type TH)
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208
- Weight: 0.142 grams (Approximate)



Typical Configuration



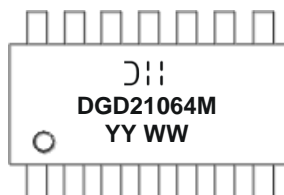
SO-14  
Top View

## Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Quantity Per Reel
DGD21064MS14-13	DGD21064M	13	16	2,500

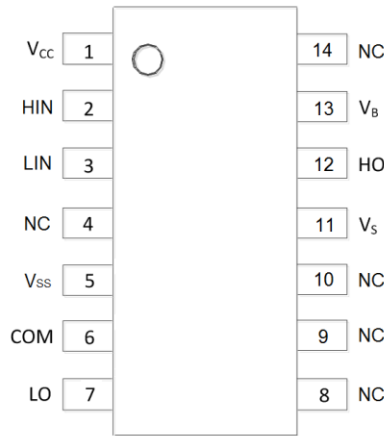
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



= Manufacturer's Marking  
 DGD21064M = Product Type Marking Code  
 YY = Year (ex: 19 = 2019)  
 WW = Week (01 to 53)

**Pin Diagrams**

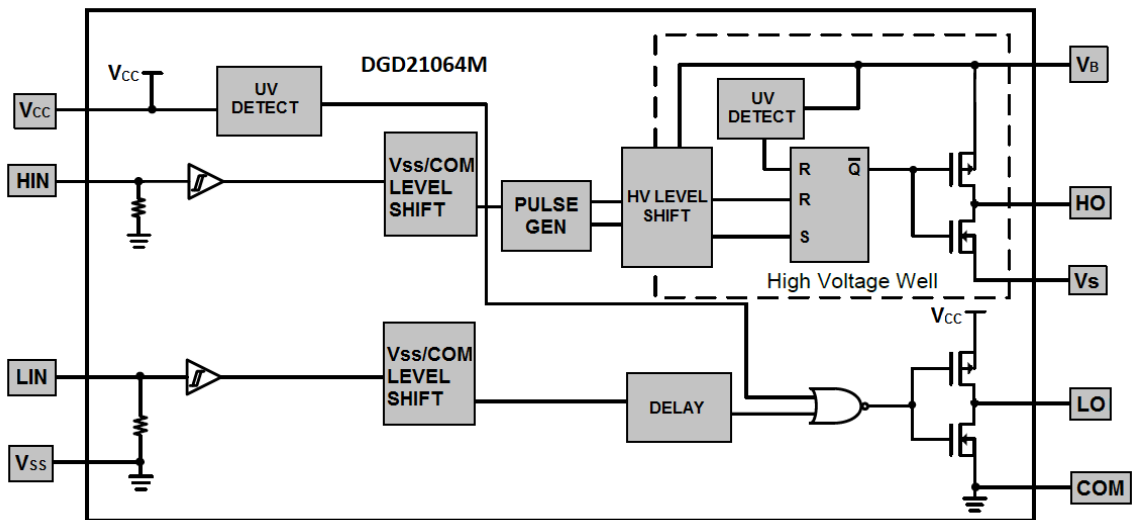


Top View: SO-14

**Pin Descriptions**

Pin Number	Pin Name	Function
1	V <sub>CC</sub>	Low-Side and Logic Fixed Supply
2	HIN	Logic Input for High-Side Gate Driver Output, in Phase with HO (Referenced to V <sub>SS</sub> )
3	LIN	Logic Input for Low-Side Gate Driver Output, in Phase with LO (Referenced to V <sub>SS</sub> )
4, 8, 9, 10, 14	NC	No Connection (No Internal Connection)
5	V <sub>SS</sub>	Logic Ground
6	COM	Low-Side Return
7	LO	Low-Side Gate Drive Output
11	V <sub>S</sub>	High-Side Floating Supply Return
12	HO	High-Side Gate Drive Output
13	V <sub>B</sub>	High-Side Floating Supply

**Functional Block Diagram**



**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Supply Voltage	V <sub>B</sub>	-0.3 to +624	V
High-Side Floating Supply Offset Voltage	V <sub>S</sub>	V <sub>B</sub> -24 to V <sub>B</sub> +0.3	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3 to V <sub>B</sub> +0.3	V
Offset Supply Voltage Transient	dV <sub>S</sub> / dt	50	V/ns
Low-Side and Logic Fixed Supply Voltage	V <sub>CC</sub>	-0.3 to +24	V
Low-Side Output Voltage	V <sub>LO</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Logic Supply Offset Voltage	V <sub>SS</sub>	V <sub>SS</sub> -24 to V <sub>CC</sub> +0.3	V
Logic Input Voltage (HIN and LIN)	V <sub>IN</sub>	V <sub>SS</sub> -0.3 to V <sub>CC</sub> +0.3	V

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P <sub>D</sub>	1.0	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	120	°C/W
Operating Temperature	T <sub>J</sub>	+150	°C
Lead Temperature (Soldering, 10s)	T <sub>L</sub>	+300	
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply Absolute Voltage	V <sub>B</sub>	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
High-Side Floating Supply Offset Voltage	V <sub>S</sub>	(Note 6)	600	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub>	V <sub>B</sub>	V
Low-Side Fixed Supply Voltage	V <sub>CC</sub>	10	20	V
Low-Side Output Voltage	V <sub>LO</sub>	COM	V <sub>CC</sub>	V
Logic Input Voltage (HIN and LIN)	V <sub>IN</sub>	V <sub>SS</sub>	5	V
Logic Ground	V <sub>SS</sub>	-5	5	V
Ambient Temperature	T <sub>A</sub>	-40	+125	°C

Note: 6. Logic operation for V<sub>S</sub> of -5V to +600V.

**DC Electrical Characteristics** ( $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $V_{SS}$  = COM, @ $T_A$  = +25°C, unless otherwise specified.) (Note 7)

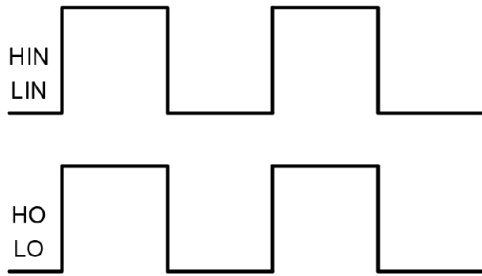
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" Input Voltage (Note 8)	$V_{IH}$	2.5	—	—	V	$V_{CC}$ = 10V to 20V
Logic "0" Input Voltage (Note 8)	$V_{IL}$	—	—	0.6	V	$V_{CC}$ = 10V to 20V
High Level Output Voltage, $V_{BIAS} - V_O$	$V_{OH}$	—	0.05	0.2	V	$I_O$ = 2mA
Low Level Output Voltage, $V_O$	$V_{OL}$	—	0.02	0.1	V	$I_O$ = 2mA
Offset Supply Leakage Current	$I_{LK}$	—	—	50	$\mu$ A	$V_B = V_S = 600V$
Quiescent $V_{BS}$ Supply Current	$I_{BSQ}$	20	75	130	$\mu$ A	$V_{IN}$ = 0V or 5V
Quiescent $V_{CC}$ Supply Current	$I_{CCQ}$	60	120	180	$\mu$ A	$V_{IN}$ = 0V or 5V
Logic "1" Input Bias Current	$I_{IN+}$	—	5.0	20	$\mu$ A	$V_{IN}$ = 5V
Logic "0" Input Bias Current	$I_{IN-}$	—	—	5.0	$\mu$ A	$V_{IN}$ = 0V
$V_{BS}$ Supply Undervoltage Positive Going Threshold	$V_{BSUV+}$	8.0	8.9	9.8	V	—
$V_{BS}$ Supply Undervoltage Negative Going Threshold	$V_{BSUV-}$	7.4	8.2	9.0	V	—
$V_{CC}$ Supply Undervoltage Positive Going Threshold	$V_{CCUV+}$	8.0	8.9	9.8	V	—
$V_{CC}$ Supply Undervoltage Negative Going Threshold	$V_{CCUV-}$	7.4	8.2	9.0	V	—
Hysteresis	$V_{CCUVH}$	0.3	0.7	—	V	—
	$V_{BSUVH}$	0.3	0.7	—	V	—
Output High Short Circuit Pulsed Current	$I_{O+}$	130	290	—	mA	$V_O$ = 0V, $PW \leq 10\mu s$
Output Low Short Circuit Pulsed Current	$I_{O-}$	270	600	—	mA	$V_O$ = 15V, $PW \leq 10\mu s$

- Notes:
- The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to COM and are applicable to the two logic pins: HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output pins: HO and LO.
  - For optimal operation, it is recommended that the input pulses (HIN and LIN) should have a minimum amplitude of 2.5V with a minimum pulse width of 440ns.

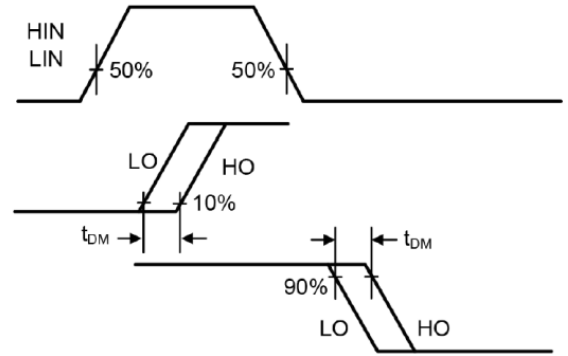
**AC Electrical Characteristics** ( $V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000pF,  $V_{SS}$  = COM, @ $T_A$  = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Propagation Delay	$t_{ON}$	—	220	300	ns	$V_S$ = 0V
Turn-Off Propagation Delay	$t_{OFF}$	—	200	280	ns	$V_S$ = 0V or 600V
Delay Matching	$t_{DM}$	—	—	30	ns	—
Turn-On Rise Time	$t_R$	—	100	220	ns	$V_S$ = 0V
Turn-Off Fall Time	$t_F$	—	35	80	ns	$V_S$ = 0V

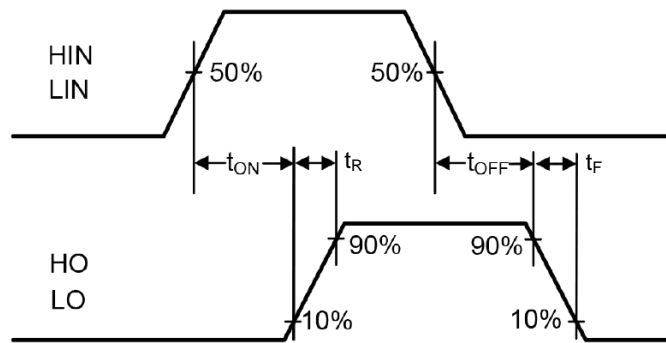
**Timing Waveforms**



**Figure 1.** Input / Output Timing Diagram

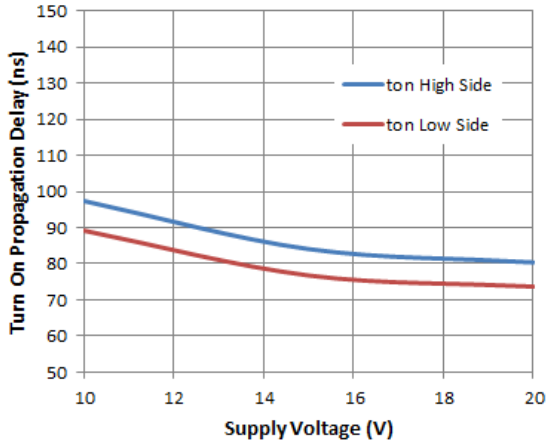


**Figure 2.** Delay Matching Waveform Definitions

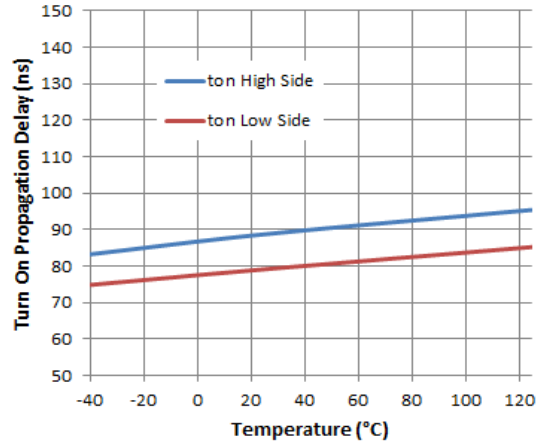


**Figure 3.** Switching Time Waveform Definitions

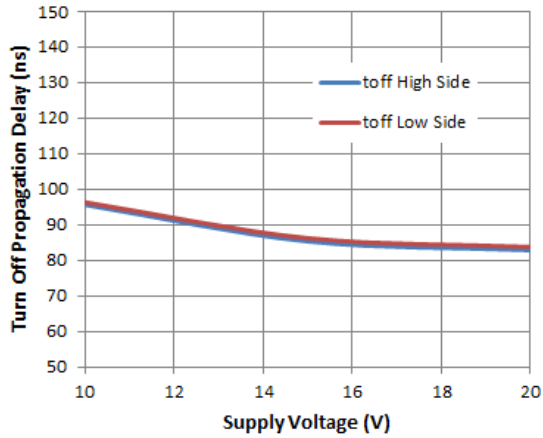
**Typical Performance Characteristics** ( $V_{CC}=15V$ , @ $T_A = +25^\circ C$ , unless otherwise specified.)



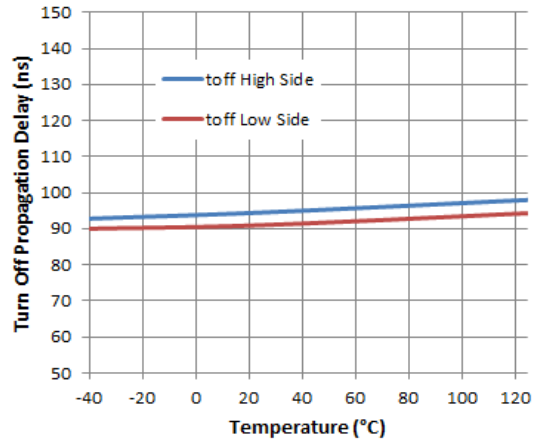
**Figure 4.** Turn-on Propagation Delay vs. Supply Voltage



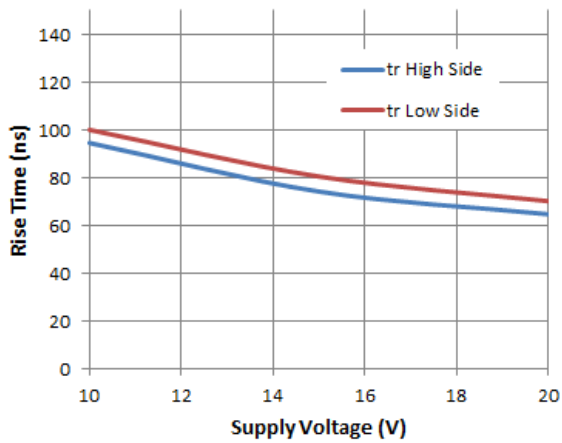
**Figure 5.** Turn-on Propagation Delay vs. Temperature



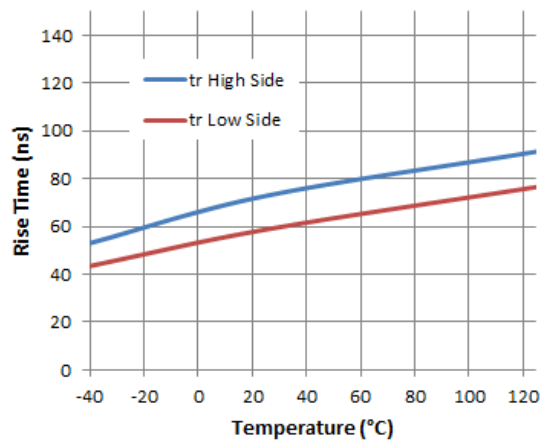
**Figure 6.** Turn-off Propagation Delay vs. Supply Voltage



**Figure 7.** Turn-off Propagation Delay vs. Temperature

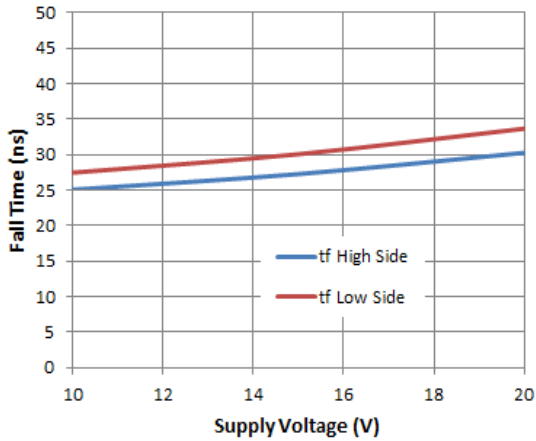


**Figure 8.** Rise Time vs. Supply Voltage

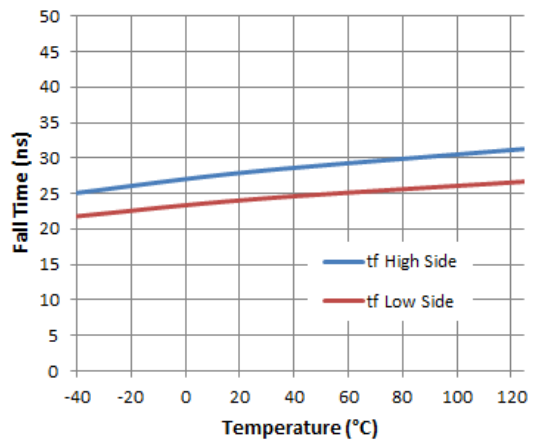


**Figure 9.** Rise Time vs. Temperature

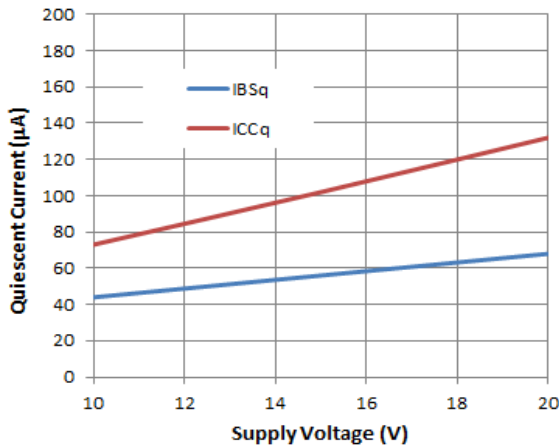
**Typical Performance Characteristics** (continued)



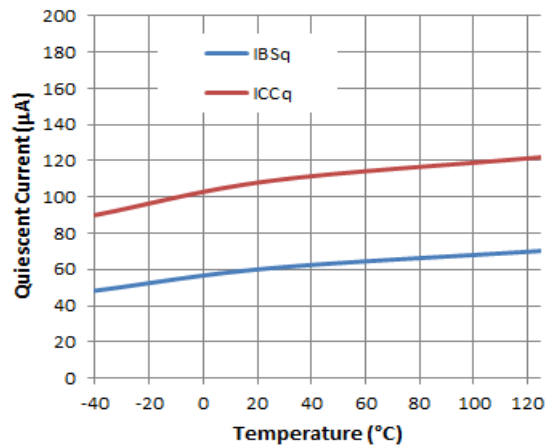
**Figure 10.** Fall Time vs. Supply Voltage



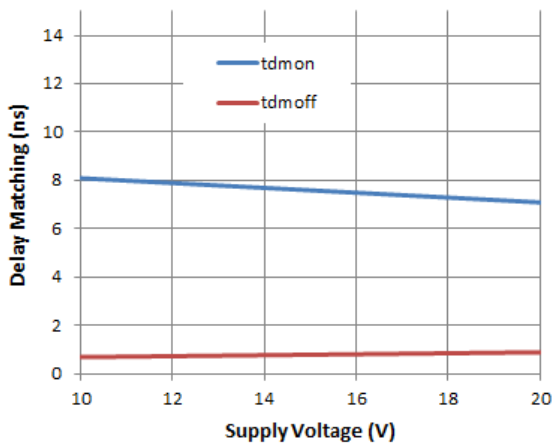
**Figure 11.** Fall Time vs. Temperature



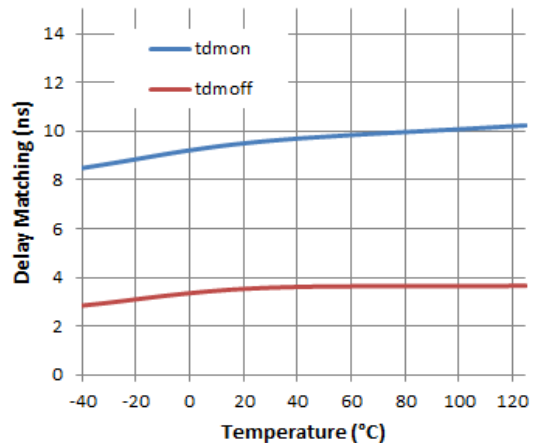
**Figure 12.** Quiescent Current vs. Supply Voltage



**Figure 13.** Quiescent Current vs. Temperature

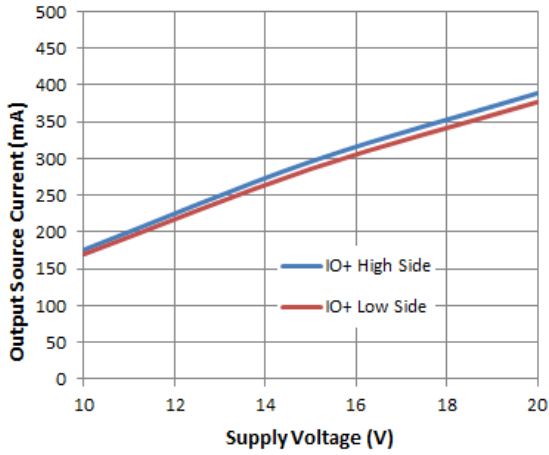


**Figure 14.** Delay Matching vs. Supply Voltage

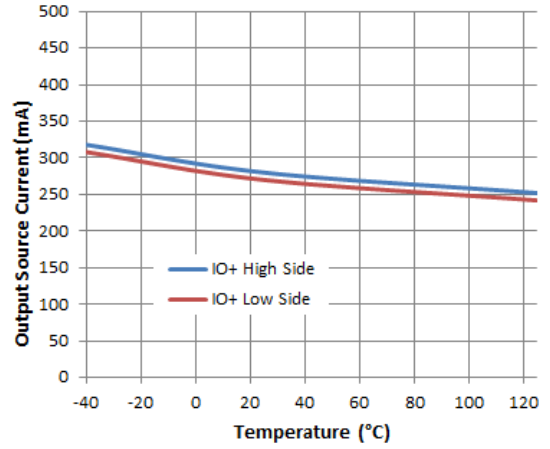


**Figure 15.** Delay Matching vs. Temperature

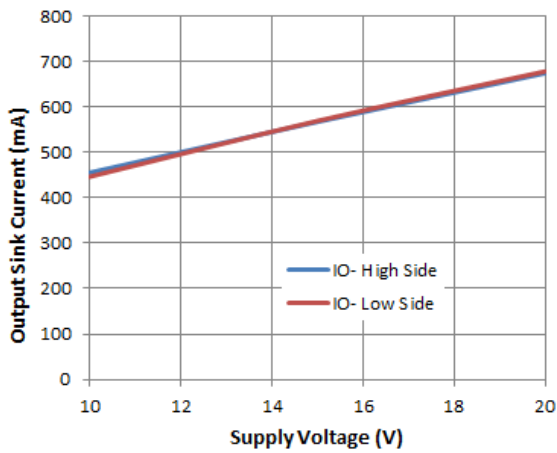
**Typical Performance Characteristics** (continued)



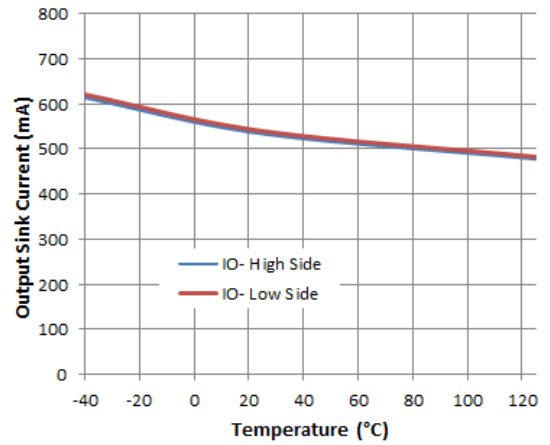
**Figure 16.** Output Source Current vs. Supply Voltage



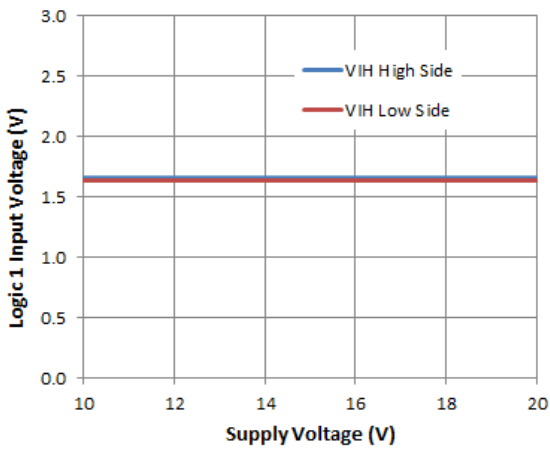
**Figure 17.** Output Source Current vs. Temperature



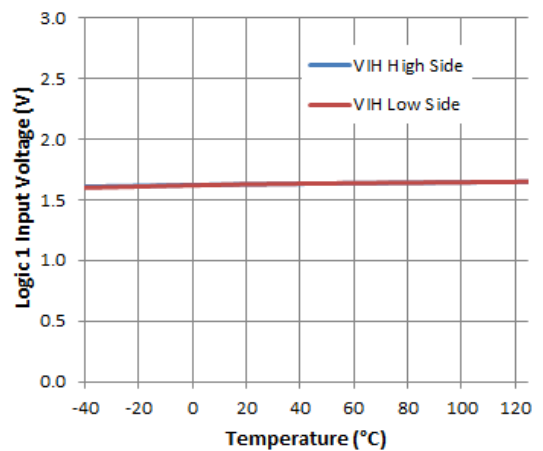
**Figure 18.** Output Sink Current vs. Supply Voltage



**Figure 19.** Output Sink Current vs. Temperature



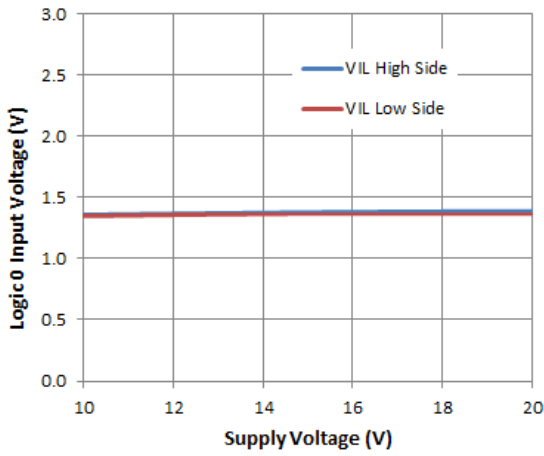
**Figure 20.** Logic 1 Input Voltage vs. Supply Voltage



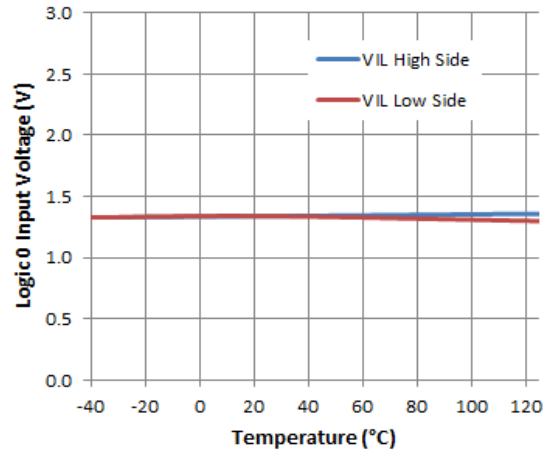
**Figure 21.** Logic 1 Input Voltage vs. Temperature



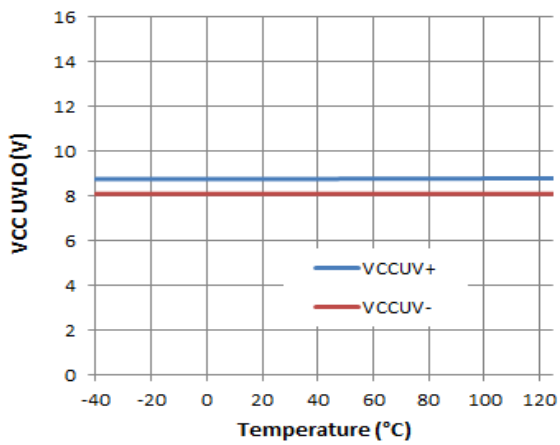
**Typical Performance Characteristics** (continued)



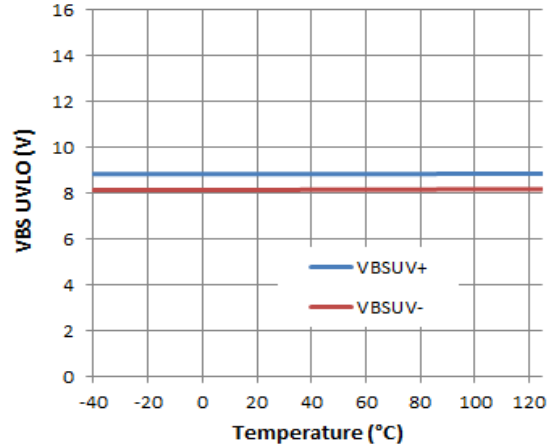
**Figure 22.** Logic 0 Input Voltage vs. Supply Voltage



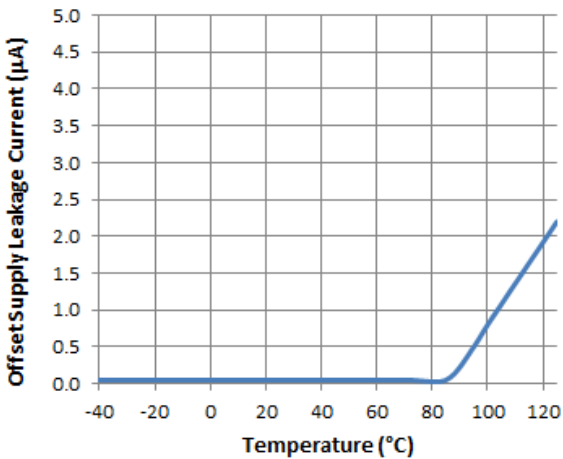
**Figure 23.** Logic 0 Input Voltage vs. Temperature



**Figure 24.** VCC UVLO vs. Temperature



**Figure 25.** VBS UVLO vs. Temperature

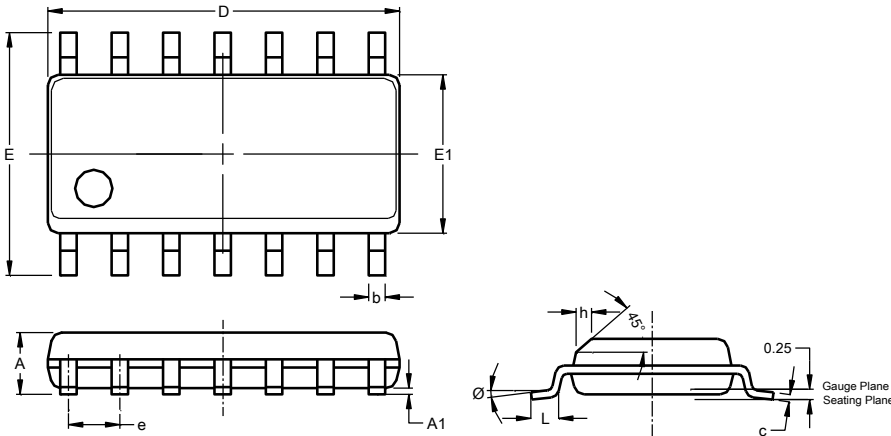


**Figure 26.** Offset Supply Leakage Current vs. Temperature

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-14 (Type TH)**

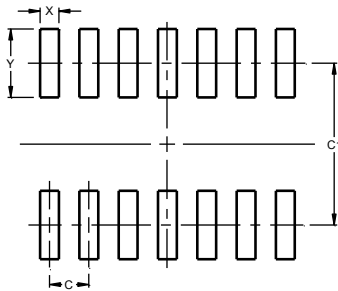


SO-14 (Type TH)			
Dim	Min	Max	Typ
A	1.55	1.73	--
A1	0.10	0.25	--
b	0.35	0.51	--
c	0.190	0.248	--
D	8.56	8.74	8.61
E	5.84	6.20	6.00
E1	3.81	3.99	3.94
e	--	--	1.27
h	--	--	0.33
L	0.41	0.89	--
Ø	0°	8°	--
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-14 (Type TH)**



Dimensions	Value (in mm)
C	1.27
C1	5.20
X	0.60
Y	2.20

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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