

General Description

The MIC4100/1 are high frequency, 100V Half Bridge MOSFET driver ICs featuring fast 30ns propagation delay times. The low-side and high-side gate drivers are independently controlled and matched to within 3ns typical. The MIC4100 has CMOS input thresholds, and the MIC4101 has TTL input thresholds. The MIC4100/1 include a high voltage internal diode that charges the high-side gate drive bootstrap capacitor.

A robust, high-speed, and low power level shifter provides clean level transitions to the high side output. The robust operation of the MIC4100/1 ensures the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high speed voltage transitions. Under-voltage protection is provided on both the low-side and high-side drivers.

The MIC4100 is available in the SOIC-8L package with a junction operating range from -40°C to $+125^{\circ}\text{C}$.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

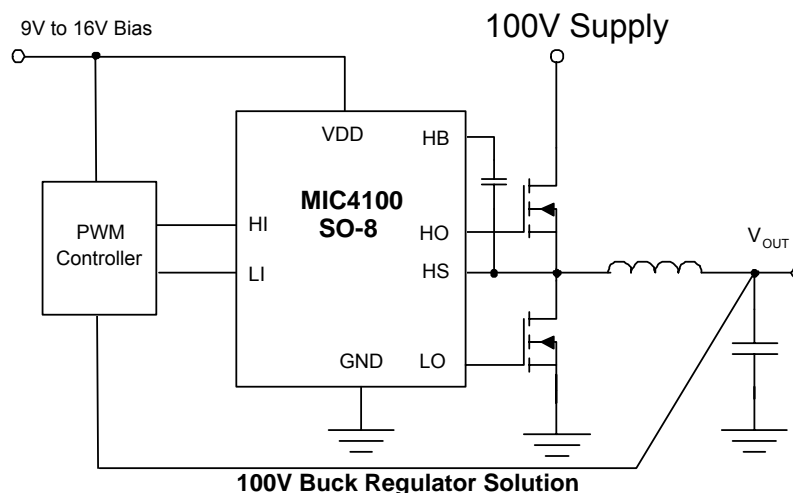
Features

- Bootstrap supply max voltage to 118V DC
- Supply voltage up to 16V
- Drives high- and low-side N-Channel MOSFETs with independent inputs
- CMOS input thresholds (MIC4100)
- TTL input thresholds (MIC4101)
- On-chip bootstrap diode
- Fast 30ns propagation times
- Drives 1000pF load with 10ns rise and fall times
- Low power consumption
- Supply under-voltage protection
- 3Ω pull up, 3Ω pull down output resistance
- Space saving SOIC-8L package
- -40°C to $+125^{\circ}\text{C}$ junction temperature range

Applications

- High voltage buck converters
- Push-pull converters
- Full- and half-bridge converters
- Active clamp forward converters

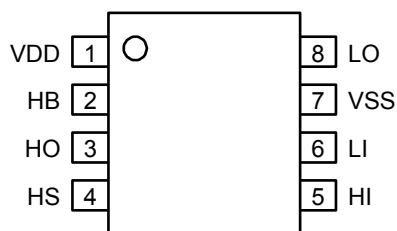
Typical Application



Ordering Information

Part Number				
Standard	Pb-Free	Input	Junction Temp. Range	Package
MIC4100BM	MIC4100YM	CMOS	-40° to +125°C	SOIC-8L
MIC4101BM	MIC4101YM	TTL	-40° to +125°C	SOIC-8L

Pin Configuration



SOIC-8L (M)

Pin Description

Pin Number	Pin Name	Pin Function
1	VDD	Positive Supply to lower gate drivers. Decouple this pin to VSS (Pin 7). Bootstrap diode connected to HB (pin 2).
2	HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
3	HO	High-Side Output. Connect to gate of High-Side power MOSFET.
4	HS	High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	High-Side input.
6	LI	Low-Side input.
7	VSS	Chip negative supply, generally will be ground.
8	LO	Low-Side Output. Connect to gate of Low-Side power MOSFET.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{DD} , $V_{HB} - V_{HS}$)	-0.3V to 18V
Input Voltages (V_{LI} , V_{HI})	-0.3V to $V_{DD} + 0.3V$
Voltage on LO (V_{LO})	-0.3V to $V_{DD} + 0.3V$
Voltage on HO (V_{HO})	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
Voltage on HS (continuous)	-1V to 110V
Voltage on HB	118V
Average Current in VDD to HB Diode	100mA
Junction Temperature (T_J)	-55°C to +150°C
Storage Temperature (T_s)	-60°C to +150°C
EDS Rating ⁽³⁾	Note 3

Operating Ratings⁽²⁾

Supply Voltage (V_{DD})	+9V to +16V
Voltage on HS	-1V to 100V
Voltage on HS (repetitive transient)	-5V to 105V
HS Slew Rate	50V/ns
Voltage on HB	$V_{HS} + 8V$ to $V_{HS} + 16V$ and $V_{DD} - 1V$ to $V_{DD} + 100V$
Junction Temperature (T_J)	-40°C to +125°C
Junction Thermal Resistance	
SOIC-8L (θ_{JA})	140°C/W

Electrical Characteristics⁽⁴⁾

$V_{DD} = V_{HB} = 12V$; $V_{SS} = V_{HS} = 0V$; No load on LO or HO; $T_A = 25^\circ C$; unless noted. **Bold** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
V_{DD} Quiescent Current	I_{DD}	LI = HI = 0V		40	150 200	μA
V_{DD} Operating Current	I_{DDO}	f = 500kHz		2.5	3.4	mA
Total HB Quiescent Current	I_{HB}	LI = HI = 0V		25	150 200	μA
Total HB Operating Current	I_{HBO}	f = 500kHz		1.4	2.5 3	mA
HB to V_{SS} Current, Quiescent	I_{HBS}	$V_{HS} = V_{HB} = 110V$		0.05	1	μA
HB to V_{SS} Current, Operating	I_{HBSO}	f = 500kHz		10		μA
Input Pins: MIC4100 (CMOS Input)						
Low Level Input Voltage Threshold	V_{IL}		4 3	5.3		V
High Level Input Voltage Threshold	V_{IH}			5.7	7 8	V
Input Voltage Hysteresis	V_{IHYS}			0.4		V
Input Pulldown Resistance	R_I		100	200	500	$K\Omega$
Input Pins: MIC4101 (TTL)						
Low Level Input Voltage Threshold	V_{IL}		0.8	1.5		V
High Level Input Voltage Threshold	V_{IH}			1.5	2.2	V
Input Pulldown Resistance	R_I		100	200	500	$K\Omega$

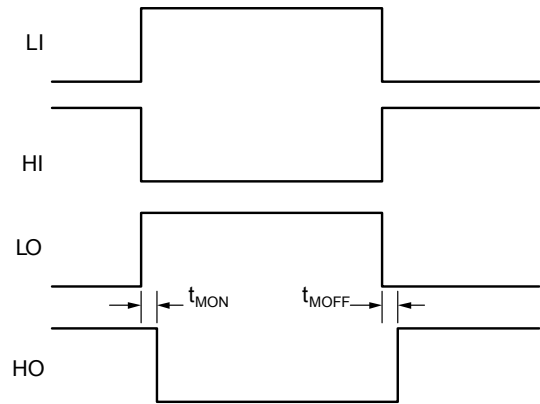
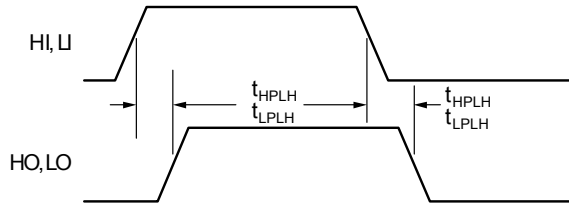
Parameter	Symbol	Condition	Min	Typ	Max	Units
Under Voltage Protection						
V _{DD} Rising Threshold	V _{DDR}		6.5	7.4	8.0	V
V _{DD} Threshold Hysteresis	V _{DDH}			0.5		V
HB Rising Threshold	V _{HBR}		6.0	7.0	8.0	V
HB Threshold Hysteresis	V _{HBH}			0.4		V
Bootstrap Diode						
Low-Current Forward Voltage	V _{DL}	I _{VDD-HB} = 100μA		0.4	0.55 0.70	V
High-Current Forward Voltage	V _{DH}	I _{VDD-HB} = 100mA		0.7	0.8 1.0	V
Dynamic Resistance	R _D	I _{VDD-HB} = 100mA		1.0	1.5 2.0	Ω
LO Gate Driver						
Low Level Output Voltage	V _{OLL}	I _{LO} = 100mA		0.22	0.3 0.4	V
High Level Output Voltage	V _{OHL}	I _{LO} = -100mA, V _{OHL} = V _{DD} - V _{LO}		0.25	0.3 0.45	V
Peak Sink Current	I _{OHL}	V _{LO} = 0V		2		A
Peak Source Current	I _{OLL}	V _{LO} = 12V		2		A
HO Gate Driver						
Low Level Output Voltage	V _{OLH}	I _{HO} = 100mA		0.22	0.3 0.4	V
High Level Output Voltage	V _{OHH}	I _{HO} = -100mA, V _{OHH} = V _{HB} - V _{HO}		0.25	0.3 0.45	V
Peak Sink Current	I _{OHH}	V _{HO} = 0V		2		A
Peak Source Current	I _{OLH}	V _{HO} = 12V		2		A

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Specifications						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}	(MIC4100)		27	45	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}	(MIC4100)		27	45	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}	(MIC4100)		27	45	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}	(MIC4100)		27	45	ns
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}	(MIC4101)		31	55	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}	(MIC4101)		31	55	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}	(MIC4101)		31	55	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}	(MIC4101)		31	55	ns
Delay Matching: Lower Turn-On and Upper Turn-Off	t_{MON}			3	8 10	ns
Delay Matching: Lower Turn-Off and Upper Turn-On	t_{MOFF}			3	8 10	ns
Either Output Rise/Fall Time	t_{RC}, t_{FC}	$C_L = 1000\text{pF}$		10		ns
Either Output Rise/Fall Time (3V to 9V)	t_R, t_F	$C_L = 0.1\mu\text{F}$		0.4	0.6 0.8	μs
Minimum Input Pulse Width that Changes the Output	t_{PW}	Note 6			50	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}			10		ns

Notes:

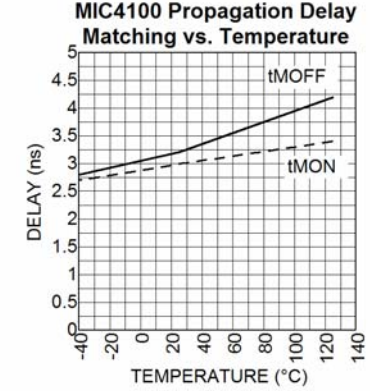
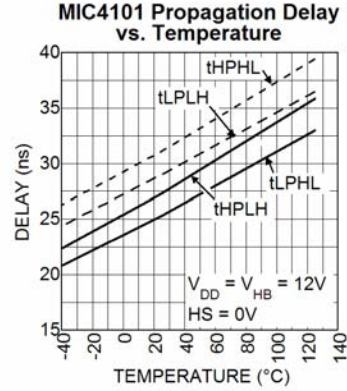
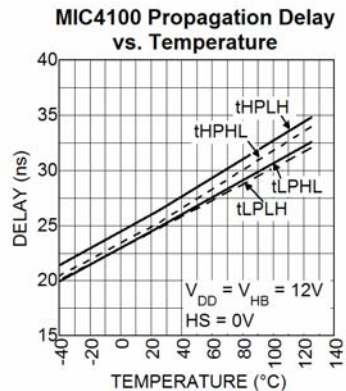
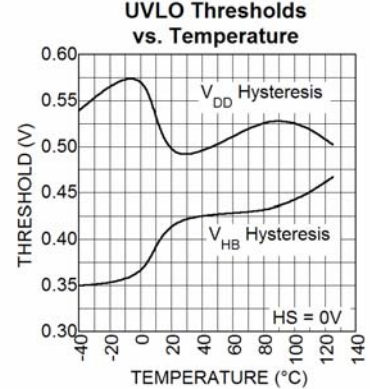
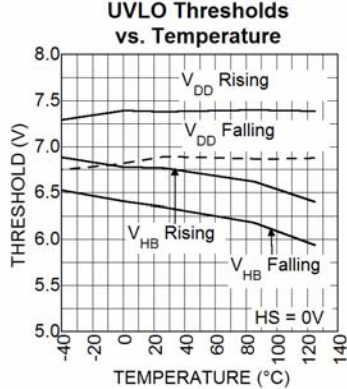
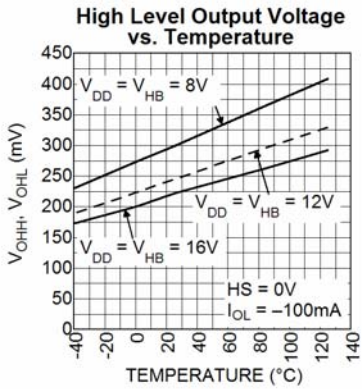
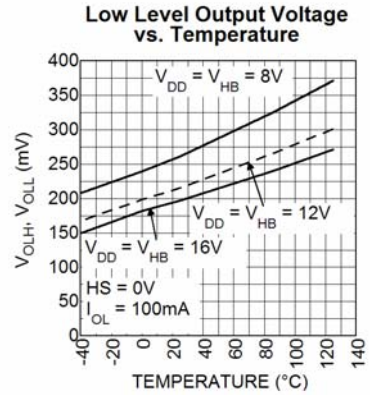
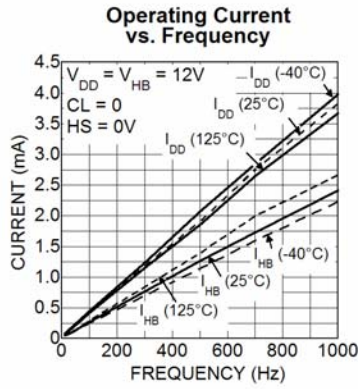
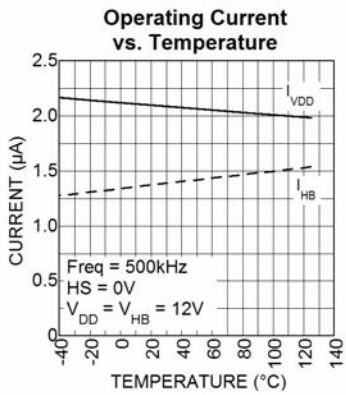
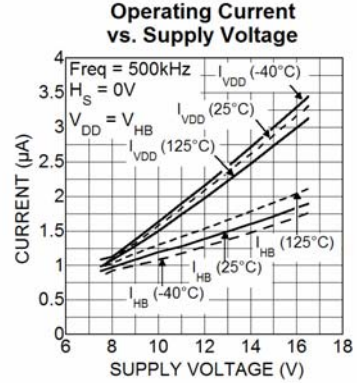
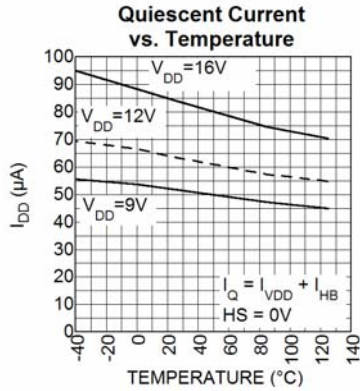
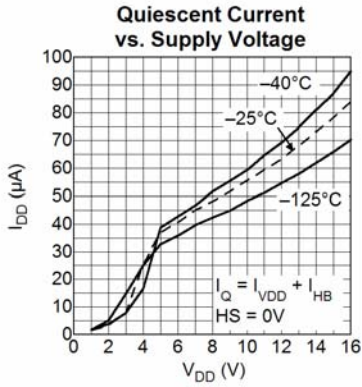
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k Ω in series with 100pF.
4. Specification for packaged product only.
5. All voltages relative to pin7, V_{SS} unless otherwise specified
6. Guaranteed by design. Not production tested.

Timing Diagrams

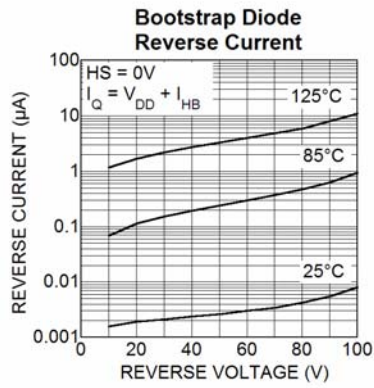
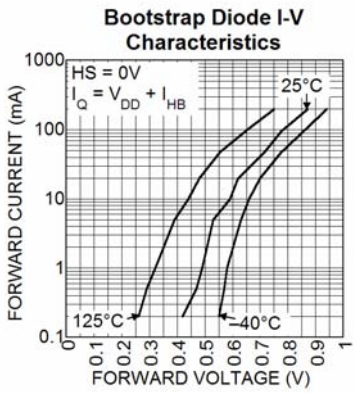
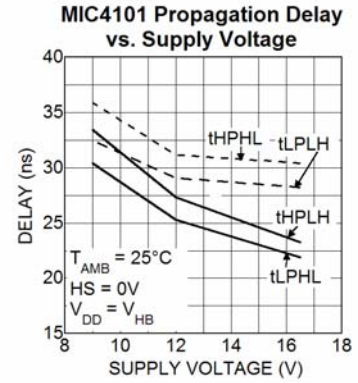
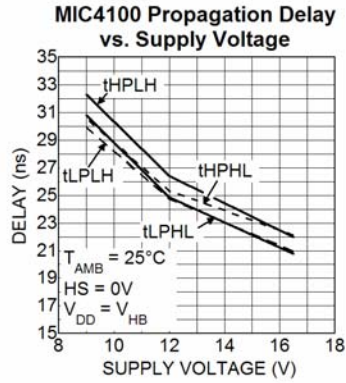
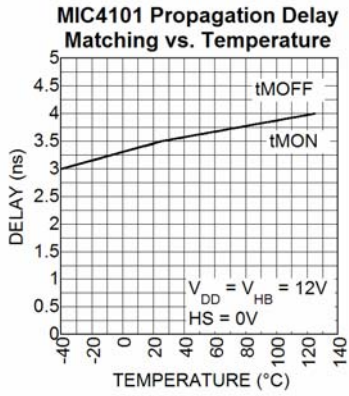


Note: All propagation delays are measured from the 50% voltage level.

Typical Characteristics



Typical Characteristics (cont.)



Functional Diagram

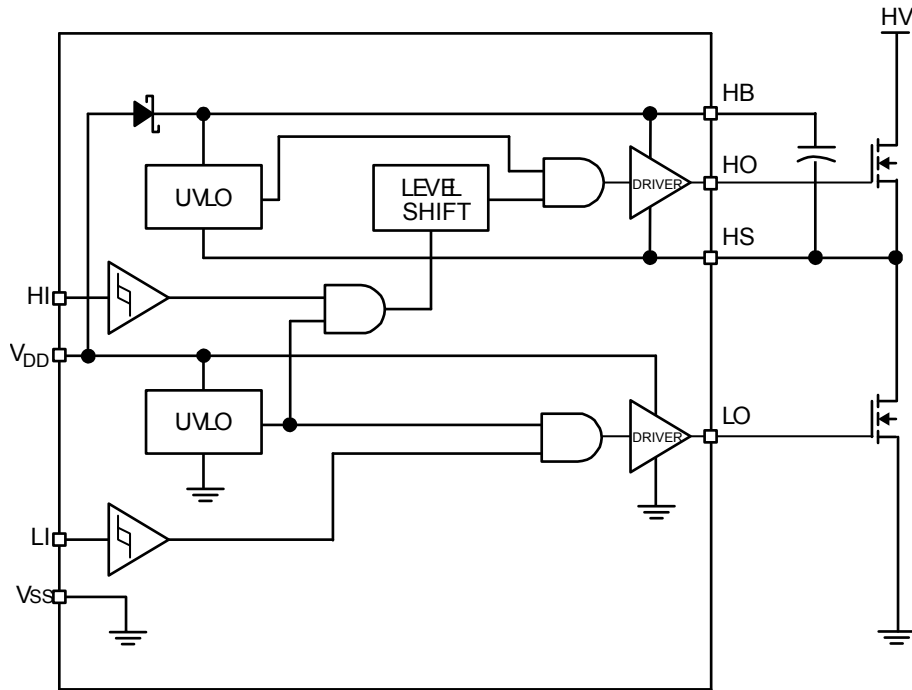


Figure 1. MIC4100 Functional Block Diagram

Functional Description

The MIC4100 is a high voltage, non-inverting, dual MOSFET driver that is designed to independently drive both high-side and low-side N-Channel MOSFETs. The block diagram of the MIC4100 is shown in Figure 1.

Both drivers contain an input buffer with hysteresis, a UVLO circuit and an output buffer. The high-side output buffer includes a high speed level-shifting circuit that is referenced to the HS pin. An internal diode is used as part of a bootstrap circuit to provide the drive voltage for the high-side output.

Startup and UVLO

The UVLO circuit forces the driver output low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

Input Stage

The MIC4100 and MIC4101 have different input stages, which lets these parts cover a wide range of driver applications. Both the HI and LI pins are referenced to the VSS pin. The voltage state of the input signal does not change the quiescent current draw of the driver.

The MIC4100 has a high impedance, CMOS compatible input range and is recommended for applications where the input signal is noisy or where the input signal swings the full range of voltage (from Vdd to Gnd). There is typically 400mV of hysteresis on the input pins throughout the VDD range. The hysteresis improves noise immunity and prevents input signals with slow rise times from falsely triggering the output. The threshold voltage of the MIC4100 varies proportionally with the VDD supply voltage.

The amplitude of the input signal affects the VDD supply current. Vin voltages that are a diode drop less than the VDD supply voltage will cause an increase in the VDD pin current. The graph in Figure 2 shows the typical dependence between I_{VDD} and Vin for Vdd=12V.

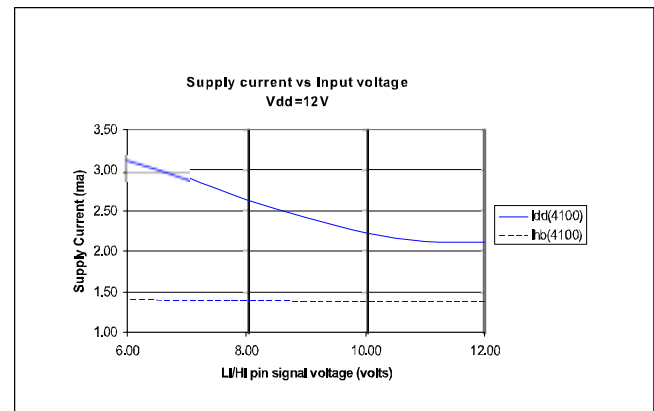


Figure 2

The MIC4101 has a TTL compatible input range and is recommended for use with inputs signals whose amplitude is less than the supply voltage. The threshold level is independent of the VDD supply voltage and there is no dependence between I_{VDD} and the input signal amplitude with the MIC4101. This feature makes the MIC4101 an excellent level translator that will drive high threshold MOSFETs from a low voltage PWM IC.

Low-Side Driver

A block diagram of the low-side driver is shown in Figure 3. The low-side driver is designed to drive a ground (Vss pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low $R_{ds(on)}$ from the external MOSFET.

A high level applied to LI pin causes the upper driver fet to turn on and Vdd voltage is applied to the gate of the external MOSFET. A low level on the LI pin turns off the upper driver and turns on the low side driver to ground the gate of the external MOSFET.

Application Information

Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the C_B capacitor times the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

$$I_{F(AVE)} = Q_{gate} \times f_s$$

where: Q_{gate} = Total Gate Charge at V_{HB}

f_s = gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals:

$$P_{diode_{fwd}} = I_{F(AVE)} \times V_F$$

where: V_F = Diode forward voltage drop

The value of V_F should be taken at the peak current through the diode, however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used and will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 11uA at a reverse voltage of 100V and 125C. Power dissipation due to reverse leakage is typically much less than 1mW and can be ignored.

Reverse recovery time is the time required for the injected minority carriers to be swept away from the depletion region during turn-off of the diode. Power dissipation due to reverse recovery can be calculated by computing the average reverse current due to reverse recovery charge times the reverse voltage across the diode. The average reverse current and power dissipation due to reverse recovery can be estimated by:

$$I_{RR(AVE)} = 0.5 \times I_{RRM} \times t_{rr} \times f_s$$

$$P_{diode_{RR}} = I_{RR(AVE)} \times V_{REV}$$

where: I_{RRM} = Peak Reverse Recovery Current

t_{rr} = Reverse Recovery Time

The total diode power dissipation is:

$$P_{diode_{total}} = P_{diode_{fwd}} + P_{diode_{RR}}$$

An optional external bootstrap diode may be used instead of the internal diode (Figure 6). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the V_{DD} supply voltage. A 100V Schottky diode will work for most 72V input telecom applications. The above equations can be used to calculate power dissipation in the external diode, however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

$$P_{diode_{REV}} = I_R \times V_{REV} \times (1 - D)$$

where: I_R = Reverse current flow at V_{REV} and T_J

V_{REV} = Diode Reverse Voltage

D = Duty Cycle = t_{ON} / f_s

f_s = switching frequency of the power supply

The on-time is the time the high-side switch is conducting. In most power supply topologies, the diode is reverse biased during the switching cycle off-time.

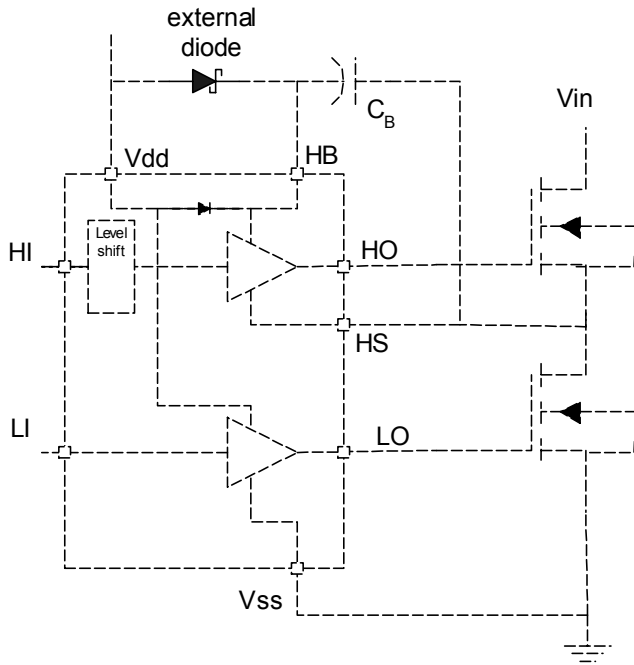


Figure 6

Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 7 shows a simplified equivalent circuit of the MIC4100 driving an external MOSFET.

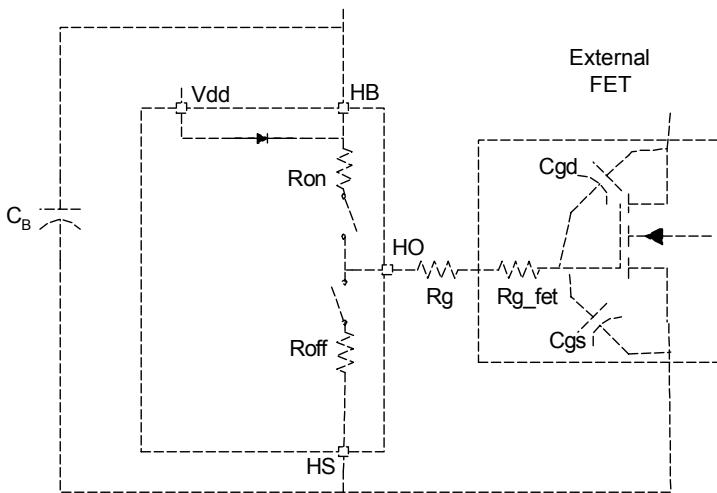


Figure 7

Dissipation during the external MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{gd} and C_{gs}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{on} , R_g and R_{g_fet} . R_{on} is the on resistance of the upper driver MOSFET in the MIC4100. R_g is the series resistor (if any) between the driver IC and the MOSFET. R_{g_fet} is the gate resistance of the MOSFET. R_{g_fet} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{on} and R_{g_fet} .

The effective capacitance of C_{gd} and C_{gs} is difficult to calculate since they vary non-linearly with I_d , V_{gs} , and V_{ds} . Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. V_{gs} . Figure 8 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

$$E = \frac{1}{2} \times C_{iss} \times V_{gs}^2$$

but

$$Q = C \times V$$

so

$$E = 1/2 \times Qg \times V_{gs}$$

where

C_{iss} is the total gate capacitance of the MOSFET

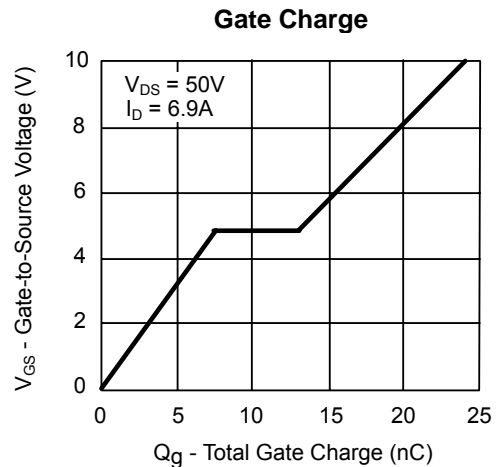


Figure 8

The same energy is dissipated by R_{off} , R_g and R_{g_fet} when the driver IC turns the MOSFET off. Assuming R_{on} is approximately equal to R_{off} , the total energy and power dissipated by the resistive drive elements is:

$$E_{\text{driver}} = Qg \times V_{gs}$$

and

$$P_{\text{driver}} = Qg \times V_{gs} \times fs$$

where

E_{driver} is the energy dissipated per switching cycle

P_{driver} is the power dissipated by switching the MOSFET on and off

Qg is the total gate charge at V_{gs}

V_{gs} is the gate to source voltage on the MOSFET

fs is the switching frequency of the gate drive circuit

The power dissipated inside the MIC4100/1 is equal to the ratio of R_{on} & R_{off} to the external resistive losses in R_g and R_{g_fet} . Letting $R_{on} = R_{off}$, the power dissipated in the MIC4100 due to driving the external MOSFET is:

$$P_{\text{diss_drive}} = P_{\text{driver}} \frac{R_{on}}{R_{on} + R_g + R_{g_fet}}$$

Supply Current Power Dissipation

Power is dissipated in the MIC4100 even if it is there is nothing being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the V_{dd} and V_{hb} voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4100 due to supply current is

$$P_{\text{diss_sup_ply}} = V_{dd} \times I_{dd} + V_{hb} \times I_{hb}$$

Total power dissipation and Thermal Considerations

Total power dissipation in the MIC4100 or MIC4101 is equal to the power dissipation caused by driving the external MOSFETs, the supply current and the internal bootstrap diode.

$$P_{\text{diss_total}} = P_{\text{diss_sup_ply}} + P_{\text{diss_drive}} + P_{\text{diode_total}}$$

The die temperature may be calculated once the total power dissipation is known.

$$T_J = T_A + P_{\text{diss_total}} \times \theta_{JA}$$

where:

T_A is the maximum ambient temperature

T_J is the junction temperature (°C)

$P_{\text{diss_total}}$ is the power dissipation of the MIC4100/1

θ_{JC} is the thermal resistance from junction to ambient air (°C/W)

Propagation Delay and Delay Matching and other Timing Considerations

Propagation delay and signal timing is an important

consideration in a high performance power supply. The MIC4100 is designed not only to minimize propagation delay but to minimize the mismatch in delay between the high-side and low-side drivers.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Many power supply topologies use two switching MOSFETs operating 180° out of phase from each other. These MOSFETs must not be on at the same time or a short circuit will occur, causing high peak currents and higher power dissipation in the MOSFETs. The MIC4100 and MIC4101 output gate drivers are not designed with anti-shoot-through protection circuitry. The output drives signals simply follow the inputs. The power supply design must include timing delays (dead-time) between the input signals to prevent shoot-through. The MIC4100 & MIC4101 drivers specify delay matching between the two drivers to help improve power supply performance by reducing the amount of dead-time required between the input signals.

Care must be taken to insure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low side (V_{dd}) and high side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs as well as minimize the voltage ripple on these pins. The capacitor from HB to HS serves double duty by providing decoupling for the high-side circuitry as well as providing current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. A minimum value of 0.1µf is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic

capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used since even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the V_{DD} and V_{SS} pins. The bypass capacitor (C_B) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section on layout and component placement for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge vs. V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_B \geq \frac{Q_{gate}}{\Delta V_{HB}}$$

where: Q_{gate} = Total Gate Charge at V_{HB}
 ΔV_{HB} = Voltage drop at the HB pin

The decoupling capacitor for the V_{DD} input may be calculated in with the same formula; however, the two capacitors are usually equal in value.

Grounding, Component Placement and Circuit Layout

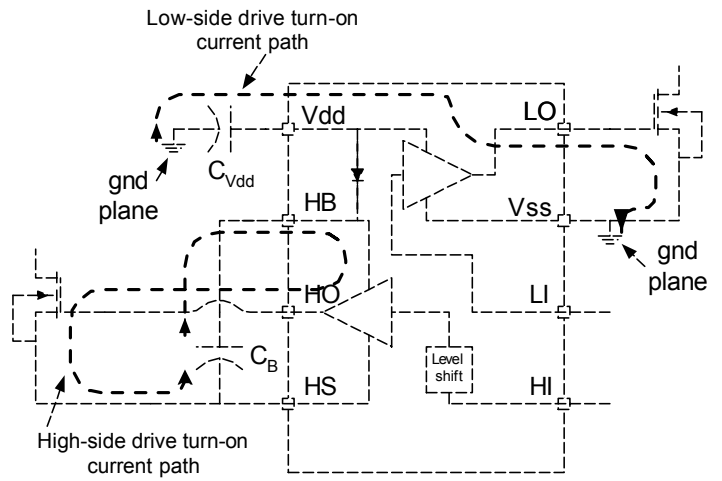
Nanosecond switching speeds and ampere peak currents in and around the MIC4100 and MIC4101 drivers require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing or circuit latch-up.

Figure 9 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate and out the Source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period where it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the HB pin and out the HO pin, into the gate of the high side MOSFET. The return path for the current

is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback which fights the turn-on of the MOSFET.

It is important to note that capacitor C_B must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.



Turn-On Current Paths

Figure 9

Figure 10 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B.

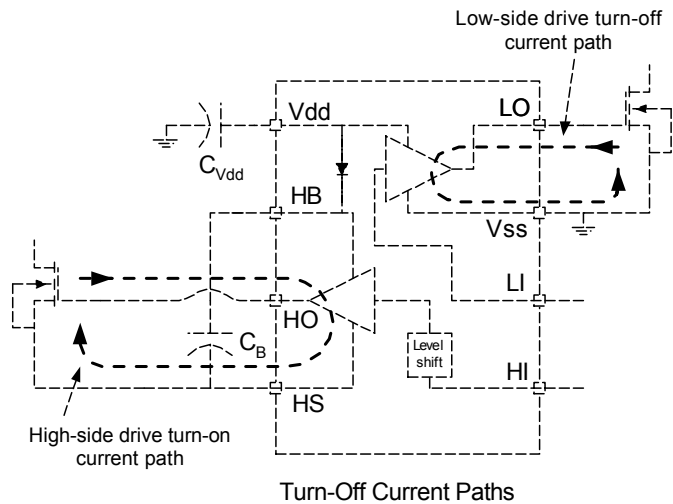


Figure 10

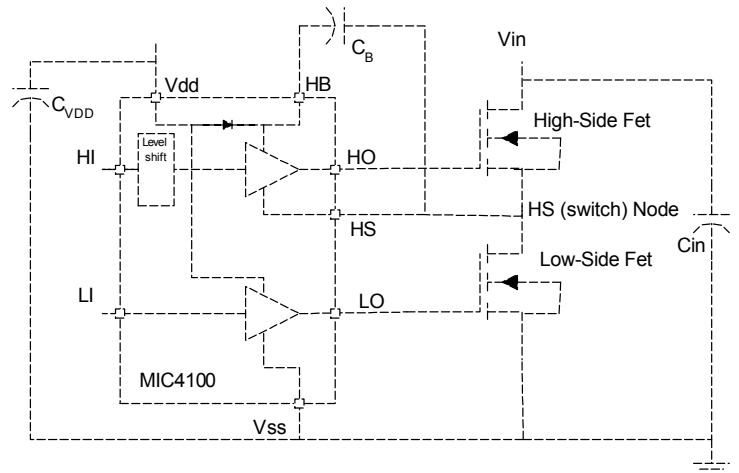


Figure 11

The following circuit guidelines should be adhered to for optimum circuit performance:

1. The Vcc and HB bypass capacitors must be placed close to the supply and ground pins. It is critical that the etch length between the high side decoupling capacitor (C_B) and the HB & HS pins be minimized to reduce lead inductance.
2. A ground plane should be used to minimize parasitic inductance and impedance of the return paths. The MIC4100 is capable of greater than 2A peak currents and any impedance between the MIC4100, the decoupling capacitors and the external MOSFET will degrade the performance of the driver.
3. Trace out the high di/dt and dv/dt paths, as shown in Figures 9 and 10 and minimize etch length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times.

A typical layout of a synchronous Buck converter power stage (Figure 11) is shown in Figure 12.

The circuit is configured as a synchronous buck power stage. The high-side MOSFET drain connects to the input supply voltage (drain) and the source connects to the switching node. The low-side MOSFET drain connects to the switching node and its source is connected to ground. The buck converter output inductor (not shown) would connect to the switching node. The high-side drive trace, HO, is routed on top of its return trace, HS, to minimize loop area and parasitic inductance. The low-side drive

trace LO is routed over the ground plane which minimizes the impedance of that current path. The decoupling capacitors, C_B and C_{VDD} are placed to minimize etch length between the capacitors and their respective pins. This close placement is necessary to efficiently charge capacitor C_B when the HS node is low. All traces are 0.025" wide or greater to reduce impedance. C_{in} is used to decouple the high current path through the MOSFETs.

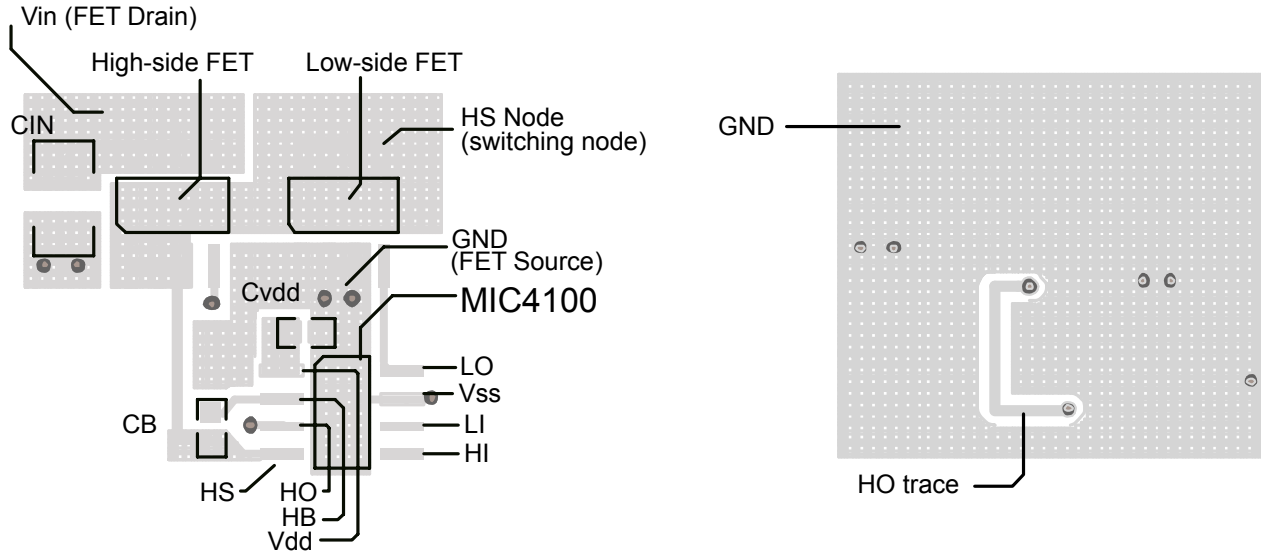
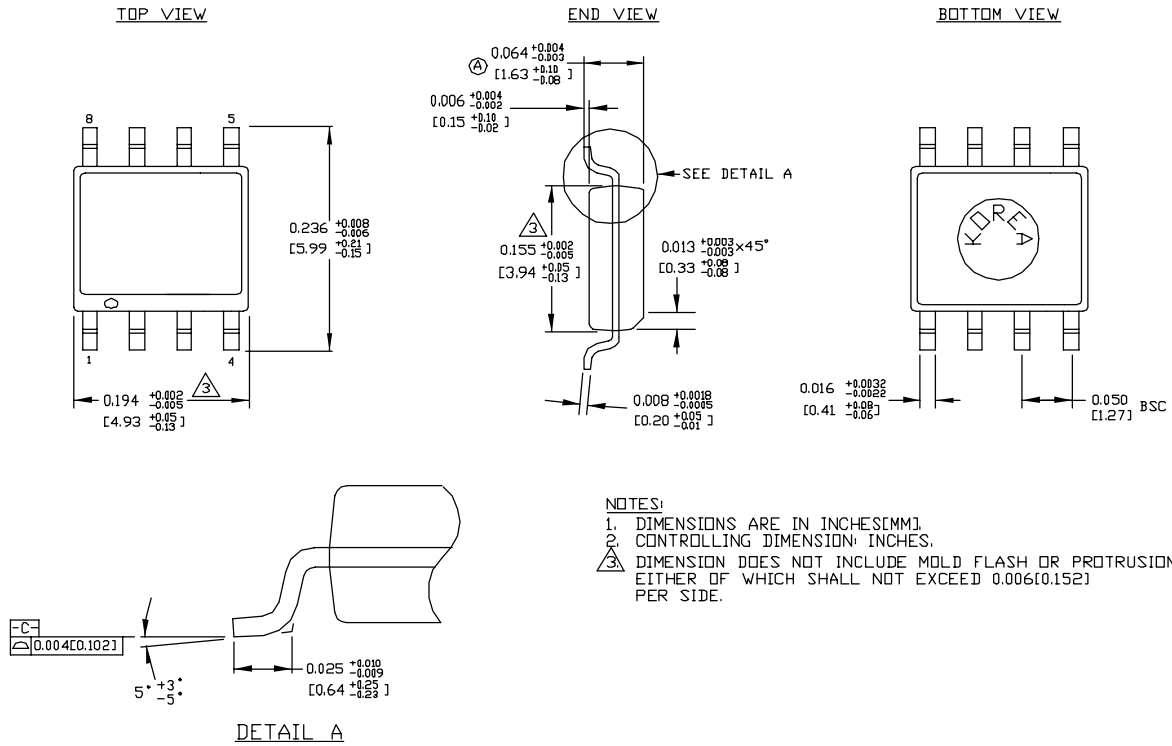


Figure 12

Package Information



8-Pin SOIC (M)

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