

## Features

- Fully operational to +650V
- Tolerant of negative transient voltages
- dV/dt immune (50V/ns)
- Latch-up protected over entire operating range
- Fault-current shutdown for all drive outputs
- User selectable delay or latching function for clearing of the FAULT signal, independent user controlled clearing of the FAULT signal is also available
- UVLO protection for all drive outputs
- Enable signal capable of disabling all driver outputs
- 3 half-bridge driver pairs (independent)
- 3.3V logic compatible
- Cross-conduction prevention logic, 220 ns - 360ns Phase leg deadtime
- Peak output current: 600mA Pull-up/Source, 600mA Pull-down/Sink
- Wide operating supply voltage range: 8.0V to 35V
- Capacitive load drive capability: 1250pF in < 100ns
- Matched, low propagation delay times
- Low supply current
- Monolithic construction
- Fault monitoring is accompanied by a FLT signal indication, with programmable reset or user selectable latched protection
- Target package power dissipation capability is 2.0W.
- Full level of function available from -55°C to + 125°C
- Available in 48-Lead 7mm x 7mm MLP Quad package and 44-Lead PLCC package

## General Description

The IXA531 is a monolithic, 3-phase, MOSFET/IGBT gate driver consisting of three independent, high and low side output channels. In addition to the six inputs, which are CMOS/TTL Compatible, for the three corresponding high side and three low side outputs, there are dedicated lines for FAULT, ENABLE and RESET. Overload/Short Circuit protection is implemented by sensing a voltage across a shunt or low value resistor which carries load current. Upon Overload/Short Circuit detection, all outputs are disabled. Likewise ENABLE (EN) pin, when LOW under abnormal operating conditions, affords soft shut down of outputs. FAULT (FLT) signal's status indicates that shut down has occurred either due to Overload/Short Circuit in driven MOSFET/IGBT or Under Voltage on  $V_{CL}$ . Clearing of FAULT (FLT) signal and restoration of normal operation ensue automatically after a programmed delay using an RC Network wired at RST (RESET) pin. Matched propagation delays ensure proper operation even at very high switching frequencies. Absence of cross conduction in output stages removes possibility of shoot through in driven power MOSFETs or IGBTs.

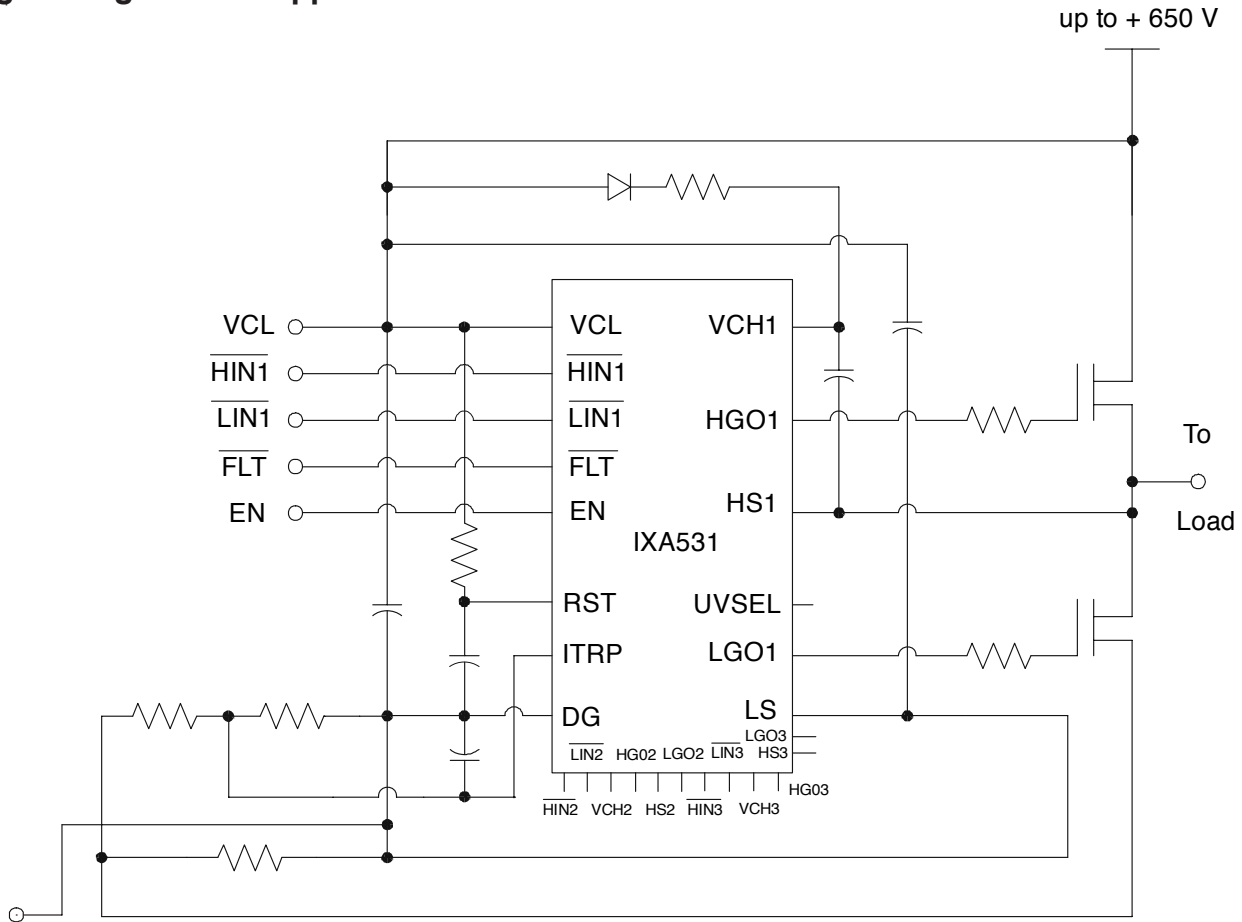
## Applications

- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

## Ordering Information

| Part      | Package     |
|-----------|-------------|
| IXA531S10 | 48L - SSLGA |
| IXA531L4  | 44L - PLCC  |

**Warning: The IXA531 is ESD sensitive.**

**Fig. 1. Single Phase Application**


### Pin Description And Configuration

| SYMBOL                          | FUNCTION         | DESCRIPTION  |
|---------------------------------|------------------|--|
| $\overline{\text{HIN}}_{1,2,3}$ | HS Input         | High side Input signal, TTL or CMOS compatible; HGO1,2,3 out of phase  |
| $\overline{\text{LIN}}_{1,2,3}$ | LS Input         | Low side Input signal, TTL or CMOS compatible; LGO1,2,3 out of phase   |
| EN                              | Enable           | Chip enable. When driven high, both outputs go low.  |
| DG                              | Ground           | Logic Reference Ground   |
| VCH1,2,3                        | Supply Voltage   | High Side Power Supply   |
| HGO1,2,3                        | Output           | High side driver output  |
| HS1,2,3                         | Return           | High side voltage return   |
| VCL                             | Supply Voltage   | Low side and Logic fixed power supply. This power supply provides power for all outputs. Voltage range is from 8.0 to 35V. |
| LGO1,2,3                        | Output           | Low side driver output   |
| LS                              | Low side return  | Low side driver return   |
| $\overline{\text{FLT}}$         | Fault            | Indicates Low-Side under voltage or Over Current Trip  |
| ITRP                            | Trip             | Input for over current shutdown  |
| RST                             | Delay after trip | Externally connected RC network decide FAULT CLEAR delay.  |

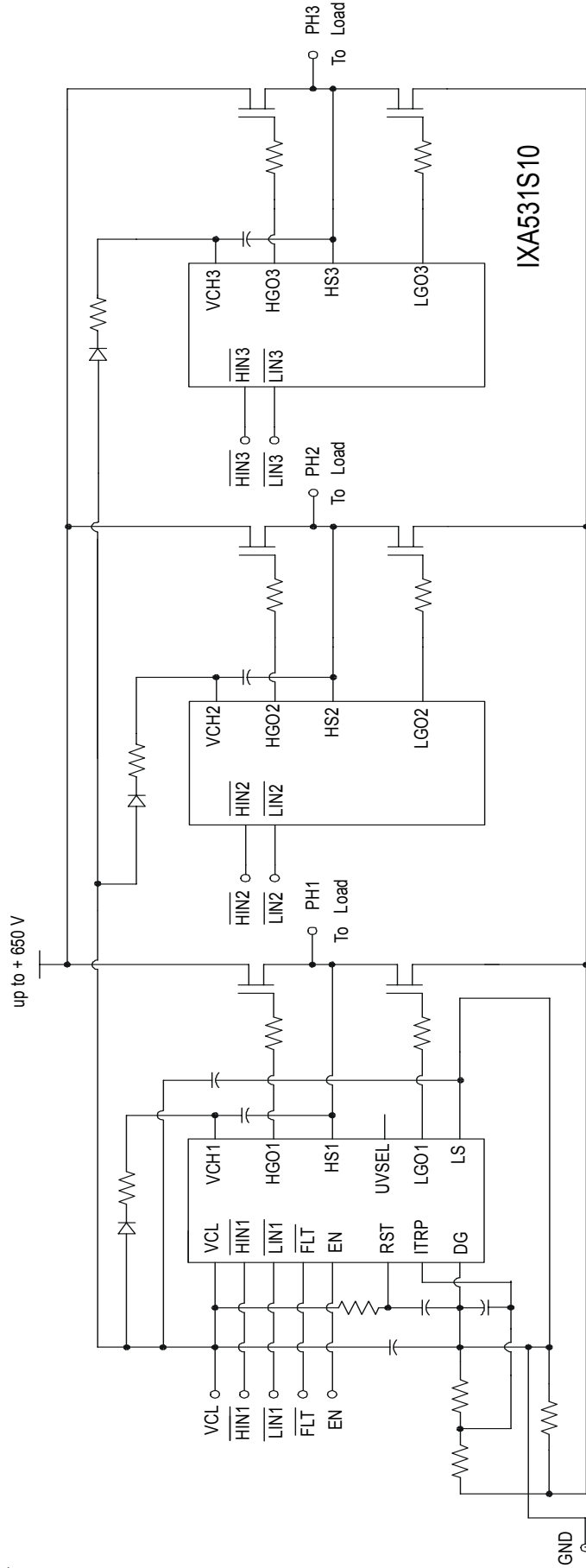


Fig. 2. 3-Phase Application for the IXA531.

### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to LS. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions

| Symbol            | Definition   | Min.                       | Max.   | Units |
|-------------------|--|----------------------------|--|-------|
| V <sub>CH</sub>   | High side floating supply voltage , (V <sub>CH1,2,3</sub> )        | -200                       | 650  | V     |
| V <sub>HS</sub>   | High side floating supply offset voltage , (V <sub>HS1,2,3</sub> ) | V <sub>CH1,2,3</sub> - 35  | V <sub>CH1,2,3</sub> + 0.3                                       | V     |
| V <sub>HGO</sub>  | High side floating output voltage , (V <sub>HGO1,2,3</sub> )       | V <sub>HS1,2,3</sub> - 0.3 | V <sub>CH1,2,3</sub> + 0.3                                       | V     |
| V <sub>CL</sub>   | Low side and logic fixed supply voltage                            | 8.0                        | 35   | V     |
| V <sub>DG</sub>   | Logic Supply offset voltage  | V <sub>LS</sub> - 0.7      | V <sub>LS</sub> + 0.7  | V     |
| V <sub>LGO</sub>  | Low side output voltage  | -0.3                       | V <sub>CL</sub> + 0.3  | V     |
| V <sub>IN</sub>   | Input voltage <u>HIN1,2,3</u> , <u>LIN1,2,3</u> , ITRP, RST , EN   | V <sub>DG</sub> - 0.3      | Lower of<br>(V <sub>DG</sub> + 35) or<br>(V <sub>CL</sub> + 0.3) | V     |
| V <sub>FLT</sub>  | FAULT output voltage   | V <sub>DG</sub> - 0.3      | V <sub>CL</sub> + 0.3  | V     |
| dV/dt             | Allowable offset voltage slew rate                                 |                            | 50   | V/ns  |
| P <sub>D</sub>    | Package power dissipation@ T <sub>A</sub> ≤ +25°C                  |                            | 2.0  | W     |
| R <sub>thJA</sub> | Thermal resistance, junction to ambient                            |                            | 63   | K/W   |
| T <sub>J</sub>    | Junction temperature   |                            | 125  | °C    |
| T <sub>S</sub>    | Storage temperature  | -55                        | 150  | °C    |
| T <sub>L</sub>    | Lead temperature (soldering, 10 seconds)                           |                            | 300  | °C    |

### Recommended Operating Conditions

\*For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute values referenced to LS. The V<sub>HS</sub> offset rating is tested with all supplies biased at 15V differential.

| Symbol                | Definition   | Min.                               | Max.                      | Units |
|-----------------------|--|------------------------------------|---------------------------|-------|
| V <sub>CH1,2,3</sub>  | High side floating supply voltage                          | V <sub>HS1,2,3</sub> + 12          | V <sub>HS1,2,3</sub> + 35 | V     |
| V <sub>HS1,2,3</sub>  | High side floating supply offset voltage                   | -200                               | 650                       | V     |
| V <sub>HGO1,2,3</sub> | High side floating output voltage                          | V <sub>HS1,2,3</sub>               | V <sub>CH1,2,3</sub>      | V     |
| V <sub>LGO1,2,3</sub> | Low side output voltage                                    | 0                                  | V <sub>CL</sub>           | V     |
| V <sub>CL</sub>       | Low side and logic fixed supply voltage                    | 12                                 | 35                        | V     |
| V <sub>DG</sub>       | Logic Supply offset voltage                                | V <sub>LS</sub> - 0.3              | V <sub>LS</sub> + 0.3     | V     |
| V <sub>FLT</sub>      | FAULT output voltage                                       | V <sub>DG</sub>                    | V <sub>CL</sub>           | V     |
| V <sub>RST</sub>      | RST input voltage  | V <sub>DG</sub>                    | V <sub>CL</sub>           | V     |
| V <sub>ITRP</sub>     | ITRP input voltage   | V <sub>DG</sub>                    | V <sub>CL</sub>           | V     |
| V <sub>IN</sub>       | Logic input voltage <u>HIN1,2,3</u> , <u>LIN1,2,3</u> , EN | V <sub>DG</sub> or V <sub>LS</sub> | V <sub>CL</sub>           | V     |
| T <sub>A</sub>        | Ambient temperature  | -40                                | 125                       | °C    |

**Static Electrical Characteristics**

$V_{BIAS}$  ( $V_{CL}$ ,  $V_{CH1,2,3}$ ) = 15V unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to DG and are applicable to all six channels. The  $V_O$  and  $I_O$  parameters are referenced to LS and  $V_{HS1,2,3}$  and are applicable to the respective output leads:  $H_{GO1,2,3}$  and  $L_{GO1,2,3}$ .

| Symbol                  | Definition  | Min. | Typ. | Max. | Units    | Test Conditions                |
|-------------------------|---|------|------|------|----------|--------------------------------|
| $V_{INL}$               | Logic "0" input voltage $\overline{HIN1,2,3}; \overline{LIN1,2,3}$  |      |      | 0.8  | V        |                                |
| $V_{INH}$               | Logic "1" input voltage $\overline{HIN1,2,3}; \overline{LIN1,2,3}$  | 3.0  |      |      | V        |                                |
| $V_{EN,TH+}$            | EN positive going threshold   |      |      | 3.0  | V        |                                |
| $V_{EN,TH-}$            | EN negative going threshold   | 0.8  |      |      | V        |                                |
| $V_{ITRP,TH+}$          | ITRP positive going threshold                                       | 0.37 | 0.46 | 0.55 | V        |                                |
| $V_{ITRP,HYS}$          | ITRP input hysteresis   |      | .07  |      | V        |                                |
| $V_{RST,TH+}$           | RST positive going threshold  |      | 8    |      | V        |                                |
| $V_{RST,HYS}$           | RST input hysteresis  |      | 3    |      | V        |                                |
| $V_{OH1,2,3}$           | High level output voltage, $V_{CH} - V_{HGO}$ or $V_{CL} - V_{LGO}$ |      | 0.9  | 1.4  | V        | $I_O=20mA$                     |
| $V_{OL1,2,3}$           | Low level output voltage, $V_{HGO}$ or $V_{LGO}$                    |      | 0.4  | 0.6  | V        | $I_O=20mA$                     |
| $V_{CLUV+}$             | $V_{CL}$ supply under-voltage positive going threshold              | 10.6 | 11.1 | 11.6 | V        |                                |
| $V_{CHUV+}$             | $V_{CH}$ supply under-voltage positive going threshold              | 10.6 | 11.1 | 11.6 | V        |                                |
| $V_{CLUV-}$             | $V_{CL}$ supply under-voltage negative going threshold              | 10.4 | 10.9 | 11.4 | V        |                                |
| $V_{CHUV-}$             | $V_{CH}$ supply under-voltage negative going threshold              | 10.4 | 10.9 | 11.4 | V        |                                |
| $V_{CLUVH}$             | $V_{CL}$ supply under-voltage lockout hysteresis                    |      | 0.2  |      | V        |                                |
| $V_{CHUVH}$             | $V_{CH}$ supply under-voltage lockout hysteresis                    |      | 0.2  |      | V        |                                |
| $I_{LK}$                | Offset supply leakage current                                       |      |      | 50   | $\mu A$  | $V_{CH1,2,3}=V_{HS1,2,3}=600V$ |
| $I_{QVCH}$              | Quiescent $V_{CH}$ supply current                                   |      | 70   | 120  | $\mu A$  | $V_{IN}=0V$ or 5V              |
| $I_{QVCL}$              | Quiescent $V_{CL}$ supply current                                   |      | 1.6  | 2.3  | mA       | $V_{IN}=0V$ or 5V              |
| $V_{IN}$                | Input clamp voltage (HIN,LIN,ITRP,EN)                               |      | 4.9  |      | V        | $I_{IN}=100\mu A$              |
| $I_{LIN+}$ or $I_{IN+}$ | Logic "1" Input bias current for LIN1,2,3                           |      | 200  | 300  | $\mu A$  | $V_{LIN}=5V$                   |
| $I_{LIN-}$ or $I_{IN-}$ | Logic "0" Input bias current for LIN1,2,3                           |      | 100  | 220  | $\mu A$  | $V_{LIN}=0V$                   |
| $I_{HIN+}$ or $I_{IN+}$ | Logic "1" Input bias current for HIN1,2,3                           |      | 200  | 300  | $\mu A$  | $V_{HIN}=5V$                   |
| $I_{HIN-}$ or $I_{IN-}$ | Logic "0" Input bias current for HIN1,2,3                           |      | 100  | 220  | $\mu A$  | $V_{HIN}=0V$                   |
| $I_{ITRP+}$             | "high" ITRP input bias current                                      |      | 30   | 100  | $\mu A$  | $V_{ITRP}=5V$                  |
| $I_{ITRP-}$             | "low" ITRP input bias current                                       |      | 0    | 1    | $\mu A$  | $V_{ITRP}=0V$                  |
| $I_{EN+}$               | "high" ENABLE input bias current                                    |      | 30   | 100  | $\mu A$  | $V_{EN}=5V$                    |
| $I_{EN-}$               | "low" ENABLE input bias current                                     |      | 0    | 1    | $\mu A$  | $V_{EN}=0V$                    |
| $I_{RST}$               | RST input bias current  |      | 0    | 1    | $\mu A$  | $V_{RST}=0V$ or 15V            |
| $I_{GO+}$               | Output high short circuit pulsed current                            |      | 600  |      | mA       | $V_O=0V, PW<10\mu s$           |
| $I_{GO-}$               | Output low short circuit pulsed current                             |      | 600  |      | mA       | $V_O=15V, PW<10\mu s$          |
| $R_{ON,RST}$            | RST low on resistance   |      | 50   | 100  | $\Omega$ |                                |
| $R_{ON,FLT}$            | FLT low on resistance   |      | 50   | 100  | $\Omega$ |                                |

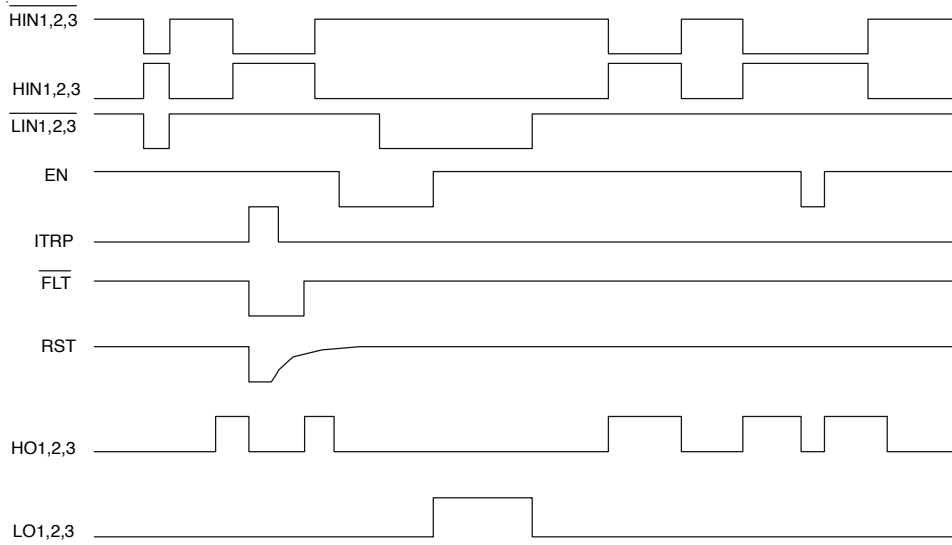
**Dynamic Electrical Characteristics**
 $V_{CL} = V_{CH} = V_{BIAS} = 15V, V_{HS1,2,3} = V_{DG} = V_{LS}, T_A = 25^\circ C$  and  $C_L = 1000pF$  unless otherwise specified.

| Symbol      | Definition  | Min. | Typ. | Max. | Units | Test Conds.                            |
|-------------|---|------|------|------|-------|--|
| $t_{on}$    | Turn-on propagation delay   | 300  | 425  | 550  | nS    | $V_{IN}=0V$ & 5V                       |
| $t_{off}$   | Turn-off propagation delay  | 250  | 400  | 550  | nS    | $V_{IN}=0V$ & 5V                       |
| $t_r$       | Turn-on rise time   |      | 125  | 190  | nS    | ----                                   |
| $t_f$       | Turn-on fall time   |      | 50   | 75   | nS    | ----                                   |
| $t_{EN}$    | ENABLE low to output shutdown propagation delay   | 300  | 450  | 600  | nS    | $V_{IN}, V_{EN} = 0V$ or 5V            |
| $t_{ITRP}$  | ITRP to output shutdown propagation delay   | 500  | 750  | 1000 | nS    | $V_{ITRP}=5V$                          |
| $t_{bl}$    | ITRP blanking time  | 100  | 150  |      | nS    | $V_{IN}=0V$ or 5V<br>$V_{ITRP} = 5V$   |
| $t_{FLT}$   | ITRP to FAULT propagation delay   | 400  | 600  | 800  | nS    | $V_{IN} = 0V$ or 5V<br>$V_{ITRP} = 5V$ |
| $t_{FILIN}$ | Input filter time (HIN, LIN, EN)  | 100  | 200  |      | nS    | $V_{IN} = 0V$ & 5V                     |
| $t_{FLCLR}$ | FAULT clear time RST=2meg, C=1nF  | 1.3  | 1.65 | 2    | mS    | $V_{IN} = 0V$ or 5V<br>$V_{ITRP}=0V$   |
| DT          | Dead time   | 220  | 290  | 360  | nS    | $V_{IN} = 0V$ & 5V                     |
| MT          | Matching delay ON and OFF   |      | 40   | 75   | nS    | External Dead Time >400nsec            |
| MDT         | Matching delay, max ( $t_{on}, t_{off}$ ) - min ( $t_{on}, t_{off}$ ) ( $t_{on}, t_{off}$ are applicable to all 3 channels) |      | 25   | 70   | nS    |  |
| PM          | Output pulse width matching, PWM <sub>IN</sub> -PWM <sub>OUT</sub>  |      | 40   | 75   | nS    |  |

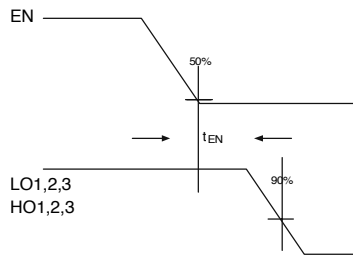
| VCL   | VCH   | ITRP               | ENABLE | FAULT      | LGO1,2,3 | HGO1,2,3 |
|-------|-------|--------------------|--------|------------|----------|----------|
| <UVCL | X     | X                  | X      | 0(note 1)  | 0        | 0        |
| 15V   | <UVCH | 0V                 | 15V    | high imp   | LIN1,2,3 | 0        |
| 15V   | 15V   | 0V                 | 15V    | high imp   | LIN1,2,3 | HIN1,2,3 |
| 15V   | 15V   | >V <sub>ITRP</sub> | 15V    | 0 (note 2) | 0        | 0        |
| 15V   | 15V   | 0V                 | 0V     | high imp   | 0        | 0        |

**Notes:** A Cross Conduction logic prevents LGO1,2,3 and HGO1,2,3 for each channel from turning on simultaneously.

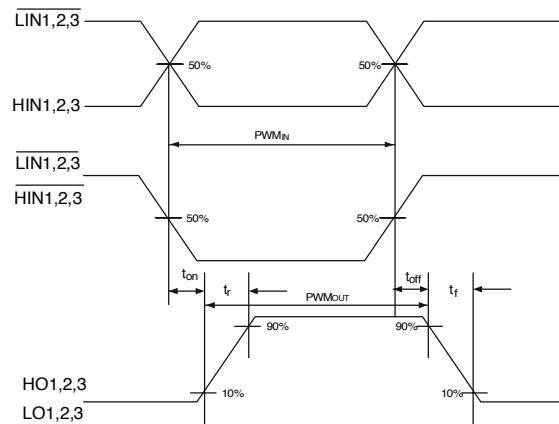
- UVCL is not latched, when  $VCL > UVCL$ , FAULT returns to high impedance.
- When  $ITRP < V_{ITRP}$ , FAULT returns to high-impedance after RST pin becomes greater than 8V (@VCL= 15V).



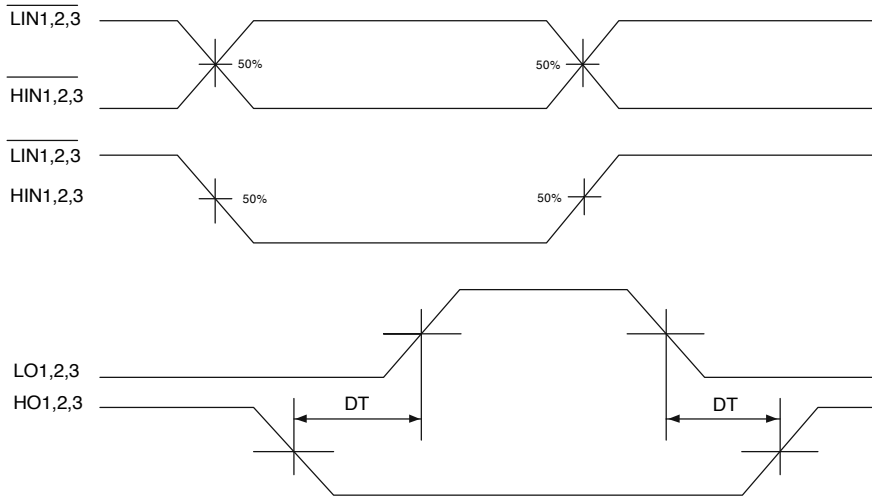
**Fig. 3. Timing Diagram**



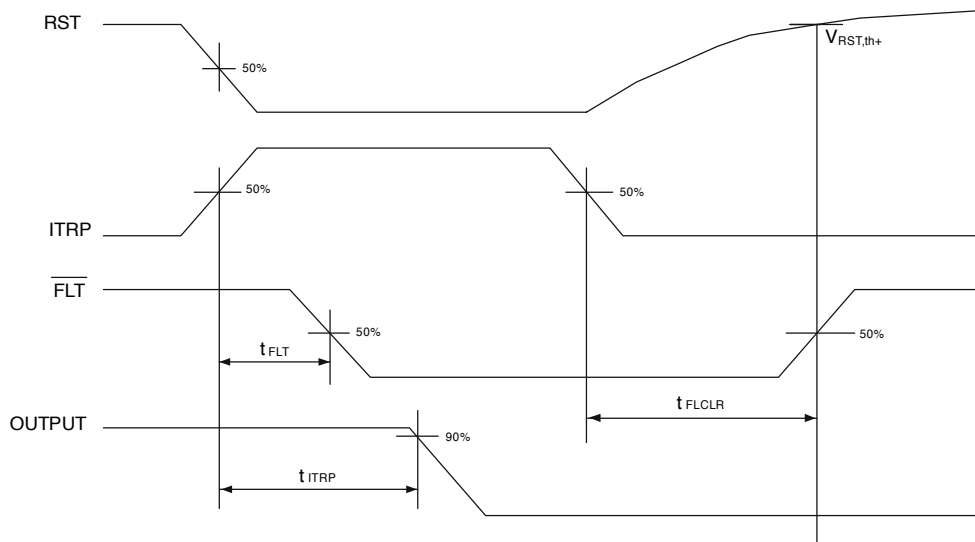
**Fig. 4. ENABLE Timing Waveforms**



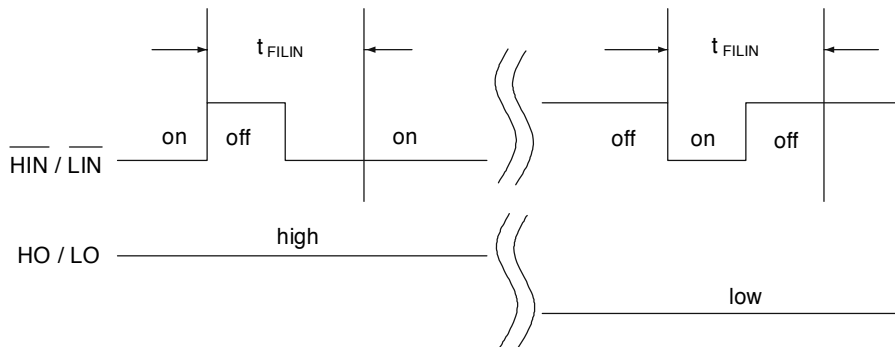
**Fig. 5. Switching Time Definitions**



**Fig. 6. Deadtime Waveforms**



**Fig. 7. ITRP / RST Waveforms**



**Fig. 8. ENABLE Timing Waveforms**



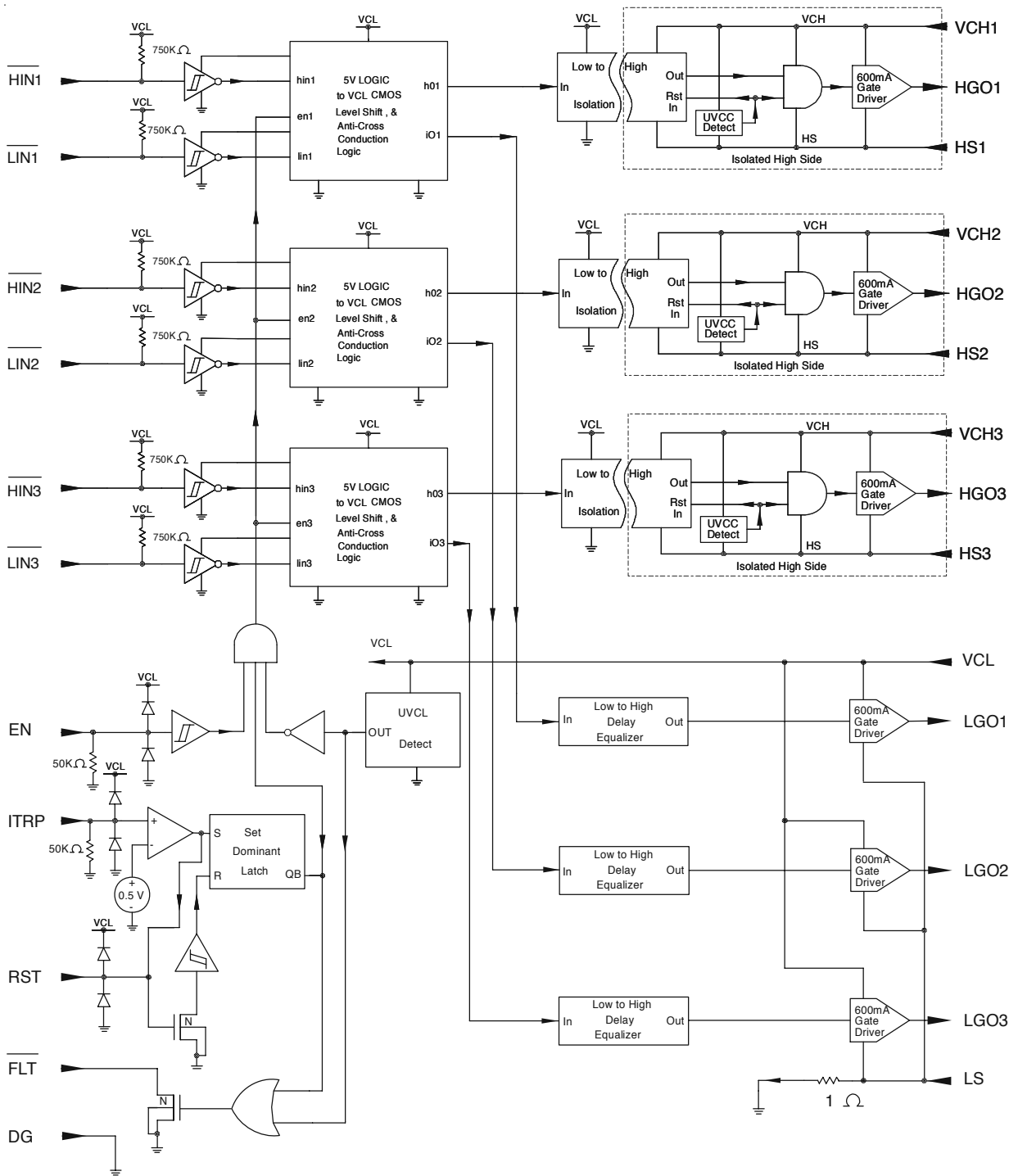


Fig. (9) IXA531 Block Diagram

Fig. 10. Pin Diagram for the IXA531S10 48-Lead MLP Quad Package

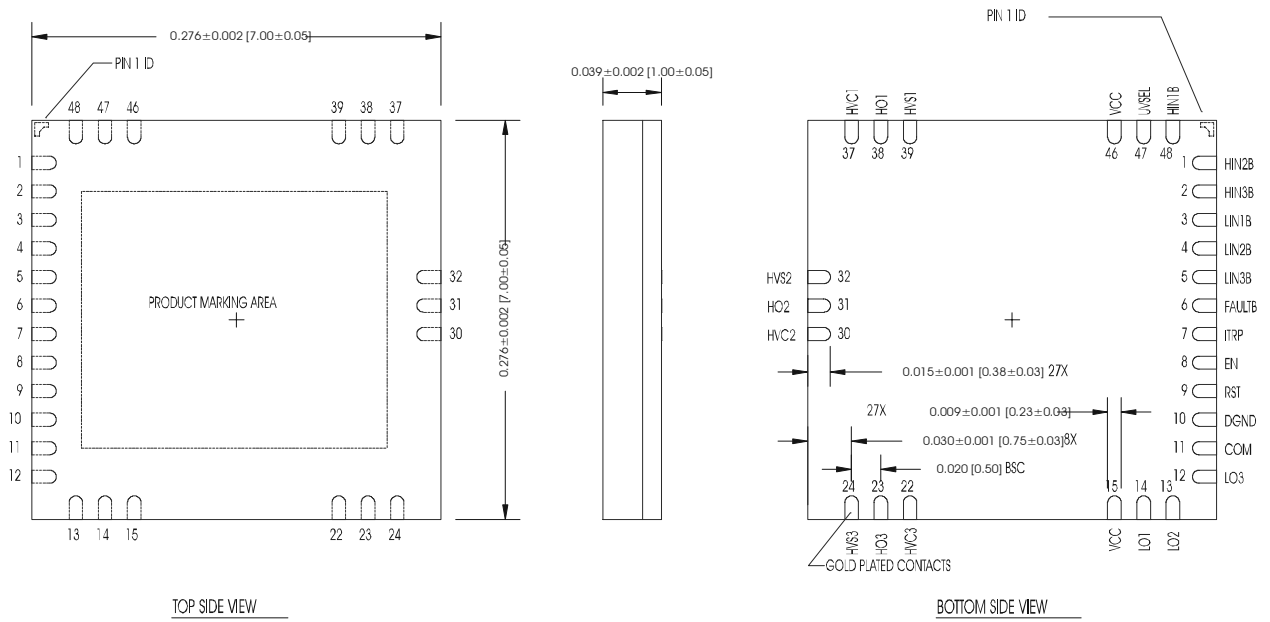


Fig. 11. Pin Diagram for the IXA531L4 44-Lead PLCC package

