Register Description 3

The 82443BX contains two sets of software accessible registers, accessed via the Host CPU I/O address space:

1. Control registers that are I/O mapped into the CPU I/O space. These registers control access to PCI and AGP configuration space.
2. Internal configuration registers residing within the 82443BX, partitioned into two logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to Host-to-PCI Bridge functionality. This set (device 0) controls PCI interface operations, DRAM configuration, and other chip-set operating parameters and optional features. The second register set (device 1) is dedicated to Host-to-AGP Bridge functions (controls AGP interface configurations and operating parameters).

The following nomenclature is used for register access attributes.

RO	**Read Only**. If a register is read only, writes to this register have no effect.
R/W	**Read/Write**. A register with this attribute can be read and written
R/WC	**Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	**Read/Write Once.** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
R/WL	**Read/Write/Lock.** This register includes a lock bit. Once the lock bit has been set to 1, the register becomes read only.

The 82443BX supports PCI configuration space access using the mechanism denoted as Configuration Mechanism #1 in the PCI specification.

The 82443BX internal registers (both I/O Mapped and Configuration registers) are accessible by the Host CPU. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFADD which can only be accessed as a Dword. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field).

Some of the 82443BX registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

Note: Software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the 82443BX contains address locations in the configuration space of the Host-to-PCI Bridge entity that are marked either "Reserved" or "Intel Reserved". The 82443BX responds to accesses to "Reserved" address locations by completing the host cycle. When a "Reserved" register location is read, a zero value is returned. ("Reserved" registers can be 8-, 16-, or 32-bit in size). Writes to "Reserved" registers have no effect on the

82443BX. Registers that are marked as "Intel Reserved" must not be modified by system software. Writes to "Intel Reserved" registers may cause system failure. Reads to "Intel Reserved" registers may return a non-zero value. Software should not write to reserved configuration locations in the device-specific region (above address offset 3Fh)

Upon reset, the 82443BX sets its internal configuration registers to predetermined default states. However, there are a few exceptions to this rule.

1. When a reset occurs during the POS/STR state, several configuration bits are not reset to their default state. These bits are noted in the following register description.
2. Some register values at reset are determined by external strapping options.

The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the 82443BX registers accordingly.

3.1 I/O Mapped Registers

The 82443BX contains three registers that reside in the CPU I/O address space – the Configuration Address (CONFADD) Register, the Configuration Data (CONFDATA) Register, and the Power Management Control Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.1.1 CONFADD—Configuration Address Register

I/O Address:	0CF8h Accessed as a Dword
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

CONFADD is a 32 bit register accessed only when referenced as a Dword. A Byte or Word reference will "pass through" the Configuration Address Register onto the PCI bus as an I/O cycle. The CONFADD register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CFGE).** When this bit is set to 1 accesses to PCI configuration space are enabled. If this bit is reset to 0 accesses to PCI configuration space are disabled.
30:24	**Reserved.**
23:16	**Bus Number.** When the Bus Number is programmed to 00h the target of the Configuration Cycle is either the 82443BX or the PCI Bus that is directly connected to the 82443BX, depending on the Device Number field. A type 0 Configuration Cycle is generated on PCI if the Bus Number is programmed to 00h and the 82443BX is not the target. If the Bus Number is non-zero a type 1 configuration cycle is generated on PCI or AGP with the Bus Number mapped to AD[23:16] during the address phase.
15:11	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 Configuration Cycle this field is decoded and one bit among AD[31:11] is driven to a 1. The 82443BX is always Device Number 0 for the Host-to-PCI bridge entity and Device Number 1 for the Host- AGP entity. Therefore, the 82443BX internally references the AD11 and AD12 pins as corresponding IDSELs for the respective devices during PCI configuration cycles. NOTE: The AD11 and AD12 must not be connected to any other PCI bus device as IDSEL signals.
10:8	**Function Number.** This field is mapped to AD[10:8] during PCIx configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The 82443BX only responds to configuration cycles with a function number of 000b; all other function number values attempting access to the 82443BX (Device Number = 0 and 1, Bus Number = 0) will generate a master abort.
7:2	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	Reserved.

3.1.2 CONFDATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

CONFDATA is a 32 bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFADD is 1 any I/O reference that falls in the CONFDATA I/O space will be mapped to configuration space using the contents of CONFADD.

3.1.3 PM2_CTL—ACPI Power Control 2 Control Register

I/O Address: 0022h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register is used to disable both the PCI and AGP arbiters in the 82443BX to prevent any external bus masters from acquiring the PCI or AGP bus. Any currently running PCI cycles will terminate properly.

Accesses to this register are controlled by the Power Management Control Register (Offset 7Ah). When bit 6 of the PMCR is set to '1', the ACPI Register at I/O location 0022h is enabled. When bit 6 is set to '0', I/O accesses to location 0022h are forwarded to PCI or AGP (if within programmable IO range).

Bit	Description
7:1	Reserved
0	**Primary PCI and AGP Arbiter Request Disable (ARB_DIS).** When this bit is set to 1, the 82443BX will not respond to any PCI REQ# signals, AGP requests, or PHOLD# from PIIX4E going active until this bit is set back to 0. Only External AGP and PCI requests are masked from the arbiters. If the PIIX is in passive release mode, masking will not occur until an active release is seen via PHLDA# assertion. This prevents possible deadlock. ARB_DIS has no effect on AGP side band signals or AGP data transfer requests.

3.2 PCI Configuration Space Access

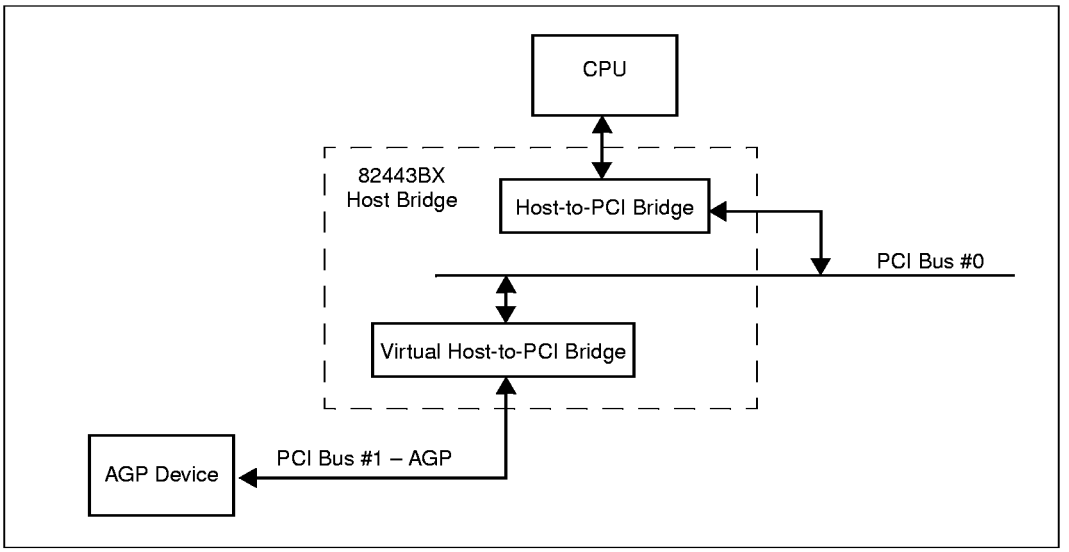
The 82443BX implementation manifests two PCI devices within a single physical component body:

- Device 0 = Host-to-PCI Bridge = PCI bus #0 interface, Main Memory Controller, Graphics Aperture controller, 82443BX specific AGP control registers.
- Device 1 = Host-to-AGP interface = "Virtual" PCI-to-PCI Bridge, including AGP address space mapping, normal PCI interface, and associated AGP sideband signal control.

Corresponding configuration registers for both devices are mapped as devices residing on PCI (bus 0). Configuration register layout and functionality for the Device #0 should be inspected carefully, as new features added to the 82443BX initiated a reasonable level of change relative to other proliferation's of the Pentium® Pro processor AGPsets (i.e. 440FX, 440LX). Configuration registers of the 82443BX Device #1 are based on the normal configuration space template of a PCI-to-PCI Bridge as described in the *PCI to PCI Bridge Architecture Specification.*

Figure 3-1shows the PCI bus hierarchy for the 82443BX). In the PCI bus hierarchy, the primary PCI bus is the highest level bus in the hierarchy and is PCI bus #0. The PCI-to-PCI bridge function provides access to the AGP/PCI bus 0. This bus is below the primary bus in the PCI bus hierarchy and is represented as PCI Bus #1.

Figure 3-1. 82443BX PCI Bus Hierarchy



3.2.1 Configuration Space Mechanism Overview

The 82443BX supports two bus interfaces: PCI (referenced as Primary PCI) and AGP (referenced as AGP). The AGP interface is treated as a second PCI bus from the configuration point of view. The following sections describe the configuration space mapping mechanism associated with both buses.

Note: The configuration space for device #1 is controlled by the AGP_DIS bit in the PMCR register. When the AGP_DIS bit (PMCR[1]) is set to 0, the configuration space for device #1 is enabled, and the registers for device #1 are accessible through the configuration mechanism defined below. When the AGP_DIS bit (PMCR[1]) is set to 1, the configuration space for device #1 is disabled. All configuration cycles (reads and writes) to device #1 of bus 0 will cause the master abort status bit for device #0/ bus 0 to be set. Configuration read cycles will return data of all 1's. Configuration write cycles will have no effect on the registers.

3.2.2 Routing the Configuration Accesses to PCI or AGP

Routing of configuration accesses to AGP is controlled via PCI-to-PCI bridge normal mechanism using information contained within the PRIMARY BUS NUMBER, the SECONDARY BUS NUMBER, and the SUBORDINATE BUS NUMBER registers of the Host-to-AGP internal "virtual" PCI-to-PCI bridge device. Detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles on one of the two buses is described below.

To distinguish between PCI configuration cycles targeting the two logical device register sets supported in the 82443BX, this document refers to the Host-to-PCI bridge PCI interface as PCI and the Host- AGP PCI interface as AGP.

3.2.3 PCI Bus Configuration Mechanism Overview

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: **Configuration Read** and **Configuration Write**. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by a mapping mechanism implemented within the chip-set. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The 82443BX supports only Mechanism #1.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register a Dword I/O write cycle is used to place a value into CONFADD that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. CONFDATA then becomes a window into the four bytes of configuration space specified by the contents of CONFADD. Any read or write to CONFDATA will result in the Host Bridge translating CONFADD into a PCI configuration cycle.

3.2.3.1 Type 0 Access

If the Bus Number field of CONFADD is 0, a Type 0 Configuration cycle is performed on PCI (i.e. bus #0). CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The Host-to-PCI Bridge entity within the 82443BX is accessed as Device #0 on the PCI bus segment. The Host- /AGP Bridge entity within the 82443BX is accessed as Device #1 on the PCI bus segment. To access Device #2, the 82443BX will assert AD13, for Device #3 will assert AD14, and so forth up to Device #20 for which will assert AD31. Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which will result in a Master Abort.

3.2.3.2 Type 1 Access

If the Bus Number field of CONFADD is non-zero, then a Type 1 Configuration cycle is performed on PCI bus (i.e. bus #0). CONFADD[23:2] is mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

3.2.4 AGP Bus Configuration Mechanism Overview

This mechanism is compatible with PCI mechanism #1 supported for the PCI bus as defined above. The configuration mechanism is the same for both accessing AGP or PCI-only devices attached to the AGP interface.

3.2.5 Mapping of Configuration Cycles on AGP

From the AGPset configuration perspective, AGP is seen as another PCI bus interface residing on a Secondary Bus side of the "virtual" PCI-to-PCI bridge referred to as the 82443BX Host- AGP bridge. On the Primary bus side, the "virtual" PCI-to-PCI bridge is attached to the BUS #0 referred to in this document as the PCI interface. The "virtual" PCI-to-PCI bridge entity is used to map Type #1 PCI Bus Configuration cycles on PCI onto Type #0 or Type #1 configuration cycles on the AGP interface.

Type 1 configuration cycles on PCI that have a BUS-NUMBER that matches the SECONDARY-BUS-NUMBER of the "virtual" PCI to PCI bridge will be translated into Type 0 configuration cycles on the AGP interface. Type 1 configuration cycles on PCI that have a BUS-NUMBER that is behind the "virtual" P2P bridge will be translated into Type 1 configuration cycles on the AGP interface.

Note: The PCI bus supports a total of 21 devices by mapping bits 15:11 of the CONFADD to the IDSEL lines on AD[31:11]. For secondary PCI busses (including the AGP bus), only 16 devices are supported by mapping bits 15:11 of the CONFADD to the IDSEL lines (AD[31:16]).

To prepare for mapping of the configuration cycles on AGP the initialization software will go through the following sequence:

1. Scan all devices residing on the PCI bus (i.e., Bus #0) using Type 0 configuration accesses.
2. For every device residing at bus #0 which implements PCI-to-PCI bridge functionality, it will configure the secondary bus of the bridge with the appropriate number and scan further down the hierarchy. This process will include the configuration of the "virtual" PCI-to-PCI Bridge within the 82443BX used to map the AGP address space in a software specific manner.

3.3 Host-to-PCI Bridge Registers (Device 0)

Table 3-1 shows the 82443BX configuration space for device #0.

Table 3-1. 82443BX Register Map — Device 0 (Sheet 1 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	7190h/7192h	RO
04–05h	PCICMD	PCI Command Register	0006h	R/W
06–07h	PCISTS	PCI Status Register	0210h/0200h	RO, R/WC
08	RID	Revision Identification	00/01h/02h	RO
09	—	Reserved	00h	—
0Ah	SUBC	Sub-Class Code	00h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch	—	Reserved	00h	—
0Dh	MLT	Master Latency Timer	00h	R/W
0Eh	HDR	Header Type	00h	RO
10–13h	APBASE	Aperture Base Address	00000008h	R/W,RO
14–2Bh	—	Reserved	00h	—
2C–2Dh	SVID	Subsystem Vendor Identification	00h	R/WO
2E–2Fh	SID	Subsystem Identification	00h	R/WO
30–33h	—	Reserved	00h	—
34h	CAPPTR	Capabilities Pointer	A0h/00h	RO
35–4Fh	—	Reserved	00h	—
50–53h	NBXCFG	440BX Configuration	[0000h]:[00S0_0000_0000_000S_0S00b]	R/W
54–56h	—	Reserved	00h	—
57h	DRAMC	DRAM Control	00S0_0000b	R/W
58h	DRAMT	DRAM Timing	03h	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	00h	R/W
60–67h	DRB[7:0]	DRAM Row Boundary (8 registers)	01h	R/W
68h	FDHC	Fixed DRAM Hole Control	00h	R/W
69–6Eh	MBSC	Memory Buffer Strength Control	0000-0000-0000h	R/W
6F–70h	—	Reserved	00h	—
71h	—	Intel Reserved	1Fh	—
72h	SMRAM	System Management RAM Control	02h	R/W
73h	ESMRAMC	Extended System Management RAM Control.	38h	R/W
74–75h	RPS	SDRAM Row Page Size	0000h	R/W
76–77h	SDRAMC	SDRAM Control Register	0000h	R/W
78–79h	PGPOL	Paging Policy Register	00h	R/W
7Ah	PMCR	Power Management Control Register	0000_S0S0b	R/W
7B–7Ch	SCRR	Suspend CBR Refresh Rate Register	0038h	R/W
7D–7Fh	—	Reserved	00h	—

Table 3-1. 82443BX Register Map — Device 0 (Sheet 2 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
80–83h	EAP	Error Address Pointer Register	00000000h	RO, R/WC
84–8Fh	—	Reserved	00h	—
90h	ERRCMD	Error Command Register	80h	R/W
91–92h	ERRSTS	Error Status Register	0000h	R/WC, RO
93h	—	Reserved	00h	R/W
94–97h	—	Intel Reserved	00006104h	—
98–99h	—	Intel Reserved	0500h	—
9Ah	—	Intel Reserved	00h	—
9B–9Fh	—	Reserved	—	—
A0–A3h	ACAPID	AGP Capability Identifier	00100002h 00000000h	RO
A4–A7h	AGPSTAT	AGP Status Register	1F000203h	RO
A8–ABh	AGPCMD	AGP Command Register	00000000h	RW
AC–AFh	—	Reserved	00h	—
B0–B3h	AGPCTRL	AGP Control Register)	00000000h	R/W
B4h	APSIZE	Aperture Size Control Register	00h	R/W
B5–B7h	—	Reserved	00h	—
B8–BBh	ATTBASE	Aperture Translation Table	00000000h	R/W
BCh	—	Reserved	—	—
BDh	—	Reserved	—	—
BE–BFh	—	Reserved	00h	—
C0–C3h	—	Intel Reserved	00000000h	—
C4–C7h	—	Intel Reserved	00000000h	—
C8h	—	Intel Reserved	18h	—
C9h	—	Intel Reserved	0Ch	—
CA–CCh	MBFS	Memory Buffer Frequency Select	000000h	R/W
CD–CFh	—	Reserved	00h	—
D0–D7h	BSPAD	BIOS Scratch Pad	00...00h	R/W
D8–DFh		Intel Reserved	000....000h	—
E0–E7h	DWTC	DRAM Write Thermal Throttling Control	000....000h	R/W/L
E8–EFh	DRTC	DRAM Read Thermal Throttling Control	000....000h	R/W/L
F0–F1h	BUFFC	Buffer Control Register	0000h	R/W/L
F2–F7h	—	Intel Reserved	0000F800h	—
F8–FBh	—	Intel Reserved	00000F20h	—
FC–FFh	—	Intel Reserved	00000000h	—

NOTES:
1. The ‘S’ symbol represents the strapping option.
2. Write operations must not be attempted to the Intel Reserved registers.

3.3.1 VID—Vendor Identification Register (Device 0)

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number.** This is a 16-bit value assigned to Intel. Intel VID = 8086h.

3.3.2 DID—Device Identification Register (Device 0)

Address Offset: 02–03h
Default Value: 7190h/7192h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number.** This is a 16 bit value assigned to the 82443BX Host-to-PCI Bridge Function #0. 7190h = When the AGP_DIS bit (PMCR[1]) is set to 0, the DID =7190h. 7192h = When the AGP_DIS bit is set to 1, the DID = 7192h.

3.3.3 PCICMD—PCI Command Register (Device 0)

Address Offset: 04–05h
Default: 0006h
Access: Read/Write
Size 16 bits

This 16-bit register provides basic control over the 82443BX PCI interface ability to respond to PCI cycles. The PCICMD Register enables and disables the SERR# signal, 82443BX response to PCI special cycles, and enables and disables PCI bus master accesses to main memory.

Bit	Descriptions
15:10	Reserved.
9	**Fast Back-to-Back.** Fast back-to-back cycles to different PCI targets are not implemented by the 82443BX. 0 = Hardwired to 0.
8	**SERR# Enable (SERRE).** Note that this bit only controls SERR# for the PCI bus. Device #1 has its own SERRE bit to control error reporting for the bus conditions occurred on the AGP bus. Two control bits are used in a logical OR manner to control SERR# pin driver. 1 = If this bit is set to a 1, the 82443BX's SERR# signal driver is enabled and SERR# is asserted when an error condition occurs, and the corresponding bit is enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. Also, if this bit is set and the 82443BX's PCI parity error reporting is enabled by the PERRE bit located in this register, then the 82443BX will report address and data parity errors (when it is potential target). 0 = SERR# is never driven by the 82443BX.
7	**Address/Data Stepping.** Not implemented (hardwired to 0).
6	**Parity Error Enable (PERRE).** Note that the PERR# signal is not implemented by the 82443BX. 1 = Enable. Address and data parity errors are reported via SERR# mechanism (if enabled via SERRE bit). 0 = Disable. Address and data parity errors are not reported via the 82443BX SERR# signal. (NOTE: Other types of error conditions can be still signaled via SERR# mechanism.) NOTE: The 82443BX PCI bus interface is still required to generate parity even if parity error reporting is disabled via this bit.
5	Reserved.
4	**Memory Write and Invalidate Enable.** The 82443BX never uses this command. 0 = Hardwired to 0.
3	**Special Cycle Enable.** The 82443BX ignores all special cycles generated on the PCI. 0 = Hardwired to 0.
2	**Bus Master Enable (BME).** The 82443BX does not support disabling of its bus master capability on the PCI Bus. 1 = Hardwired to 1, permitting the 82443BX to function as a PCI Bus master.
1	**Memory Access Enable (MAE).** This bit enables/disables PCI master access to main memory (DRAM). The 82443BX always allows PCI master access to main memory. 1 = Hardwired to 1.
0	**I/O Access Enable (IOAE).** The 82443BX does not respond to PCI bus I/O cycles. 0 = Hardwired to 0.

3.3.4 PCISTS—PCI Status Register (Device 0)

Address Offset: 06–07h
Default Value: 0210h/0200h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort on the PCI bus. PCISTS also indicates the DEVSEL# timing that has been set by the 82443BX hardware for target responses on the PCI bus. Bits [15:12] and bit 8 are read/write clear and bits [10:9] are read only.

Bit	Descriptions
15	**Detected Parity Error (DPE).** Note that the function of this bit is not affected by the PERRE bit. PERR# is not implemented in the 82443BX. 1 = Indicates 82443BX's detection of a parity error in the address or data phase of PCI bus transactions. 0 = Software sets DPE to 0 by writing a 1 to this bit.
14	**Signaled System Error (SSE).** 1 = This bit is set to 1 when the 82443BX asserts SERR# for any enabled error condition under device 0. 0 = Software sets SSE to 0 by writing a 1 to this bit.
13	**Received Master Abort Status (RMAS).** Note that Master abort is the normal and expected termination of PCI special cycles. 1 = When the 82443BX terminates a PCI bus transaction (82443BX is a PCI master) with an unexpected master abort, this bit is set to 1. 0 = Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS).** 1 = When a 82443BX-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. The 82443BX also asserts SERR# if enabled in the ERRCMD register. 0 = Software resets RTAS to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS).** The 82443BX does not generate target abort. 0 = Hardwired to a 0
10:9	**DEVSEL# Timing (DEVT).** This 2-bit field indicates the timing of the DEVSEL# signal when the 82443BX responds as a target on PCI, and indicates the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle. 01 = Medium (hardwired to 01)
8	**Data Parity Detected (DPD).** 82443BX does not implement the PERR# pin. However, data parity errors are still detected and reported on SERR# (if enabled by SERRE and PERRE). 0 = Hardwired to 0
7	**Fast Back-to-Back (FB2B).** The 82443BX as a target does not support fast back-to-back transactions on the PCI bus. 0 = Hardwired to 0
6:5	Reserved.
4	**Capability List (CLIST).** 1 = When the AGP DIS bit (PMCR[1]) is set to 0, this bit is set to 1. 0 = When the AGP DIS bit (PMCR[1]) is set to 1, this bit is set 0.
3:0	Reserved.

3.3.5 RID—Revision Identification Register (Device 0)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the 82443BX Function #0. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number.** This is an 8-bit value that indicates the revision identification number for the 82443BX Function #0. B-1 = 02h

3.3.6 SUBC—Sub-Class Code Register (Device 0)

Address Offset: 0Ah
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the 82443BX Function #0. This code is 00h indicating a Host Bridge device. The register is read only.

Bit	Description
7:0	**Sub-Class Code (SUBC).** This is an 8-bit value that indicates the category of Bridge into which the 82443BX falls. The code is 00h indicating a Host Bridge.

3.3.7 BCC—Base Class Code Register (Device 0)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the 82443BX Function #0. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	**Base Class Code (BASEC).** This is an 8-bit value that indicates the Base Class Code for the 82443BX. This code has the value 06h, indicating a Bridge device.

3.3.8 MLT—Master Latency Timer Register (Device 0)

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register controls the amount of time that 82443BX can burst data on the PCI Bus as a PCI master. The MLT[2:0] bits are reserved and assumed to be 0 when determining the Count Value.

Bit	Description
7:3	**Master Latency Timer Count Value for PCI Bus Access.** MLT is an 8-bit register that controls the amount of time the 82443BX, as a PCI bus master, can burst data on the PCI Bus. The default value of MLT is 00h and disables this function. For example, if the MLT is programmed to 18h, then the value is 24 PCI clocks.
2:0	Reserved.

3.3.9 HDR—Header Type Register (Device 0)

Offset: 0Eh
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space.

Bit	Descriptions
7:0	**Header Type (HEADT).** This read only field always returns 0 when read. Writes have no affect on this field.

3.3.10 APBASE—Aperture Base Configuration Register (Device 0)

Offset: 10–13h
Default: 00000008h
Access: Read/Write, Read Only
Size: 32 bits

The APBASE is a normal PCI Base Address register that is used to request the base of the Graphics Aperture. The normal PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to "0" or behave as hardwired to "0"). To allow for flexibility (of the aperture) an additional register called APSIZE is used as a "back-end" register to control which bits of the APBASE will behave as hardwired to "0". This register will be programmed by the 82443BX specific BIOS code that will run before any of the generic configuration software is run.

Note: Bit 9 of the NBXCFG register is used to prevent accesses to the aperture range before this register is initialized by the configuration software and appropriate translation table structure has been established in the main memory.

Bit	Description
31:28	**Upper Programmable Base Address bits (R/W).** These bits are used to locate the range size selected via lower bits 27:4. Default = 0000b
27:22	**Lower "Hardwired"/Programmable Base Address bits.** These bits behave as a "hardwired" or as a programmable depending on the contents of the APSIZE register as defined below: **27 26 25 24 23 22 Aperture Size** r/w r/w r/w r/w r/w r/w 4 MB r/w r/w r/w r/w r/w 0 8 MB r/w r/w r/w r/w 0 0 16 MB r/w r/w r/w 0 0 0 32 MB r/w r/w 0 0 0 0 64 MB r/w 0 0 0 0 0 128 MB 0 0 0 0 0 0 256 MB Bits 27:22 are controlled by the bits 5:0 of the APSIZE register in the following manner: If bit APSIZE[5]=0 then APBASE[27]=0 and if APSIZE[5]=1 then APBASE[27]=r/w (read/write). The same applies correspondingly to other bits. Default for APSIZE[5:0]=000000b forces default APBASE[27:22] =000000b (i.e., all bits respond as "hardwired" to 0). This provides a default to the maximum aperture size of 256 MB. The 82443BX specific BIOS is responsible for selecting smaller size (if required) before PCI configuration software runs and establishes the system address map.
21:4	**Hardwired to "0".** This forces minimum aperture size selected by this register to be 4MB.
3	**Prefetchable (RO).** This bit is hardwired to "1" to identify the Graphics Aperture range as a prefetchable (i.e., the device returns all bytes on reads regardless of the byte enables), and the 82443BX may merge processor writes into this range without causing errors.
2:1	**Type (RO).** These bits determine addressing type and they are hardwired to "00" to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space.
0	**Memory Space Indicator (RO).** Hardwired to "0" to identify aperture range as a memory range.

3.3.11 SVID—Subsystem Vendor Identification Register (Device 0)

Offset: 2C–2Dh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (R/WO).** This value is used to identify the vendor of the subsystem. The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

3.3.12 SID—Subsystem Identification Register (Device 0)

Offset: 2E–2Fh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (R/WO).** This value is used to identify a particular subsystem. The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

3.3.13 CAPPTR—Capabilities Pointer Register (Device 0)

Offset: 34h
Default: A0h/00h
Access: Read Only
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location where the AGP normal registers are located.

Bit	Description
7:0	**Pointer to the start of AGP normal register block.** A0h = When the AGP_DIS bit (PMCR[1]) is set to 0, the value in this field is A0h. 00h = When the AGP_DIS bit (PMCR[1]) is set to 1, this field is set to 00h.

3.3.14 NBXCFG—NBX Configuration Register (Device 0)

Offset: 50–53h
Default: bits 31–16: 0000h
bits 15–0: 00S0-0000-000S-0S00b
Access: Read/Write, Read Only for strapping options
Size: 32 bits

Bit	Description
31:24	**SDRAM Row Without ECC.** Bit[n] of this 8 bit array corresponds to row[n] of the SDRAM array. When reading a SDRAM row (DIMM) which is none-ECC, the 82 443BX drives the ECC data lines during the first data transfer in a burst read. 0 = ECC components are populated in this row. The 82443BX will not drive the ECC signals. 1 = ECC components are not populated in this row. The 82443BX will drive the ECC lines in the first read data transferred when this row is addressed.
23:19	Reserved.
18	**Host Bus Fast Data Ready Enable (HBFDRE).** 0 = Assertion of DRAM data on host bus occurs one clock after sampling snoop results. (default) 1 = Assertion of DRAM data on host bus occurs on the same clock the snoop result is being sampled. This mode is faster by one clock cycle.

Bit	Description
17	**ECC - EDO static Drive mode.** 0 = Normal mode of operation (default). 1 = ECC signals are always driven. This mode is used in a mobile system. EDO components are used, but ECC components are not populated in any of the DRAM rows.
16	**IDSEL_REDIRECT.** This is a programmable option to make the 82443BX compatible with 430TX base design. For CPU initiated configuration cycles to PCI, Device 1 which are targeted to the 82443BX's host to AGP bridge: 0 = When set to '0' (default), IDSEL1 (or AD12) is allocated to this bridge. The external AD12 is never activated. CPU initiated configuration cycles to BUS0, DEVICE7 are targeted a PCI bus device that its IDSEL input is connected to IDSEL7 (AD18). 1 = When set to '1', IDSEL7 (or AD18) is allocated to this bridge. Since it is internal in the 82443BX, the external AD18 is never activated. CPU initiated configuration cycles to BUS0, DEVICE7 are targeted a PCI bus device that its IDSEL input is connected to IDSEL1 (AD12). In some 430TX based systems, this is connected to PIIX4E. Note that CPU initiated configuration cycles to other PCI buses or other devices are normally mapped and are not affected.
15	**WSC# Handshake Disable.** In the Uni-Processor mode, this bit should be set to '1'. In the Dual-Processor mode where external IOAPIC is used, this bit should be set to '0' (default). Setting this bit to '0', enables the WSC# handshake mechanism.
14	Intel Reserved.
13:12	**Host/DRAM Frequency.** These bits are used to determine the host and DRAM frequency. Bit 13 is set by an external strapping option at reset. These bits are also used to select the required refresh rate. These bits apply to both SDRAM and EDO, with the exception that the setting '00' for 100 MHz is illegal for an EDO system. 00 = 100 MHz 01 = Reserved 1 0 = 66 MHz 11 = Reserved
11	**AGP to PCI Access Enable.** When PHLDA# is active or there is an outstanding passive release transaction pending: 1) this bit is set to 1 and the 82443BX allows AGP to PCI traffic, or 2) this bit is set to 0 (default) and the 82443BX blocks AGP to PCI traffic. The AGP to PCI traffic must not target the ISA bus. 1 = Enable 0 =Disable
10	**PCI Agent to Aperture Access Disable.** This bit is used to prevent access to the aperture from the PCI side. 1 = Disable 0 = Enable (default). If this bit is "0" (default) and bit 9 = 1, accesses to the aperture are enabled for the PCI side. Note: This bit is don't care if bit 9 of this register = 0.
9	**Aperture Access Global Enable.** This bit is used to prevent access to the aperture from any port (CPU, PCI or AGP) before aperture range is established by the configuration software and appropriate translation table in the main DRAM has been initialized. Default is "0". It must be set after system is fully configured for aperture accesses. 1 = Enable. Note that this bit globally controls accesses to the aperture. Once enabled, bit 10 provides the next level of control for accesses originated from the PCI side. 0 = Disable
8:7	**DRAM Data Integrity Mode (DDIM) (R/W).** These bits select one of 4 DRAM data integrity modes. 00 = Non-ECC (Byte-Wise Writes supported) (Default) 01 = EC-only - Error Checking with No correction 10 = ECC Mode (Error Checking/Correction) 11 = ECC Mode with hardware scrubbing enabled

Bit	Description
6	**ECC Diagnostic Mode Enable (EDME) (R/W).** 1 = Enable. When this bit is set to 1, the 82443BX will enter ECC Diagnostic test mode and the 82443BX forces the MECC[7:0] lines to 00h for all writes to memory. During reads, the read MECC[7:0] lines are compared against internally generated ECC. Recognized errors are indicated via the ERRSTS register as in normal ECC operation. 0 = Normal operation mode (default).
5	**MDA Present (MDAP).** This bit is used to indicate the presence of a secondary monochrome adapter on the PCI bus, while the primary graphics controller is on the AGP bus. This bit works in conjunction with the VGA_EN bit (Register 3E, bit 3 of device 1) as follows: **VGA_EN** / **MDAP** / **Description** 0 / X / **All VGA cycles are sent to PCI.** PCI master cycles to the VGA range are not claimed by the 82443BX. 1 / 0 / **All VGA cycles are sent to AGP.** PCI master writes to VGA range are claimed by the 82443BX and forwarded to the AGP bus. 1 / 1 / **All VGA cycles are sent to AGP, except** for cycles in the MDA range (or the aliased ranges defined below). PCI master writes in the VGA range (outside of the MDA range) are claimed by the 82443BX and forwarded to AGP. PCI and AGP master read/writes to the MDA range are ignored by the 82443BX. The MDA ranges are a subset of the VGA ranges as follows: Memory: 0B0000h–0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh
4	Reserved.
3	**USWC Write Post During I/O Bridge Access Enable (UWPIO) (R/W).** 1 = Enable. Host USWC writes to PCI memory are posted. 0 = Disable. Posting of USWC is not allowed.
2	**In-Order Queue Depth (IOQD) (RO).** This bit reflects the value sampled on A7# on the deassertion of the CPURST#. It indicates the depth of the Pentium® Pro processor bus in-order queue (i.e., level of Pentium Pro processor bus pipelining). 1 = In-order queue = maximum. If A7# is sampled "1" (i.e,. undriven on the Pentium Pro processor bus), the depth of the Pentium Pro processor bus in-order queue is configured to the maximum allowed by the Pentium Pro processor protocol (i.e., 8). However, the actual maximum supported by the 82443BX is 4, and it is controlled by the 82443BX's Pentium Pro processor interface logic using the BNR# signaling mechanism. 0 = A7# is sampled asserted (i.e., "0"). The depth of the Pentium Pro processor bus in-order queue is set to 1 (i.e., no pipelining support on the Pentium Pro processor bus). NOTE: During reset, A7# can be driven either by the 82443BX or by an external source as defined by the strapping option on the MAB11# pin.
1:0	Reserved.

3.3.15 DRAMC—DRAM Control Register (Device 0)

Address Offset: 57h
Default Value: 00S0_0000b
Access: Read/Write
Size: 8 bits

Bit	Description
7:6	Reserved.
5	**Module Mode Configuration (MMCONFIG).** This bit is set by an external strapping option. The combination of this bit and the SDRAMPWR bit (SDRAMC register) determine the functioning of the CKE signals as defined as follows: **SDRAMPWR** / **MMCONFIG** / **CKE Operation** 0 / 0 / 3 DIMM, CKE[5:0] driven, self-refresh entry staggered. SDRAM dynamic power down available. X / 1 / 3 DIMM, CKE0 only, self-refresh entry not staggered. SDRAM dynamic power down unavailable. 1 / 0 / 4 DIMM, GCKE only, self-refresh entry staggered. SDRAM dynamic power down unavailable. **NOTE:** Under MMCONFIG mode, the AGP must be disabled.
4:3	**DRAM Type (DT).** This field indicates the DRAM type used to populate the entire array. When set to 00, EDO timings are used for all cycles to main memory. When set to 01, SDRAM timings are used for all cycles to memory. When set to 10, timings for memory cycles accommodate Registered SDRAMs. For registered SDRAM timings, all address and control lines to the SDRAMs are assumed to be registered, while memory data and ECC bits are not registered. EDO, SDRAM and Registered SDRAM cannot be mixed within a system. 00 = EDO 01 = SDRAM 10 = Registered SDRAM 11 = Reserved **NOTE:** When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.
2:0	**DRAM Refresh Rate (DRR).** The DRAM refresh rate is adjusted according to the frequency selected by this field. Disabling the refresh cycle (000) results in the eventual loss of DRAM data. Changing DRR value will reset the refresh request timer. This field is used in conjunction with the SDRAM frequency bits in the NBXCFG register to determine the correct load value for the refresh timer. 000 = Refresh Disabled 001 = 15.6 us 010 = 31.2 us 011 = 62.4 us 100 = 124.8 us 101 = 249.6 us 110 = Reserved 111 = Reserved NOTE: When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.

3.3.16 DRAMT—DRAM Timing Register (Device 0)

Address Offset: 58h
Default Value: 03h
Access: Read/Write
Size: 8 bits

This 8-bit register controls main memory DRAM timings. Refer to the DRAM section for details regarding the DRAM timings programmed in this register.

Bit	Description
7:2	Reserved.
1	**EDO RASx# Wait State (RWS).** When RWS = 1, one additional wait state is inserted before RAS# is asserted for row misses. This provides one clock of additional MAX[13:0] setup time to RASx# assertion. This bit does not affect page misses since the MAX[13:0] lines are setup several clocks in advance of RAS# assertion for page misses. 0 = 1 tASR 1 = 2 tASR
0	**EDO CASx# Wait State (CWS).** When CWS = 1, one additional wait state is inserted before the assertion of the first CASx# for page hit cycles. This allows one additional clock of MA setup time to the CASx# for the leadoff page hit cycle. Page miss and row miss timings are not affected by this bit. 0 = 1 Tasc 1 = 2 Tasc

3.3.17 PAM[6:0]—Programmable Attribute Map Registers (Device 0)

Address Offset: 59h (PAM0) – 5Fh (PAM6)
Default Value: 00h
Attribute: Read/Write

The 82443BX allows programmable memory attributes on 13 *Legacy* memory segments of various sizes in the 640 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the Pentium Pro processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE **Read Enable**. When RE = 1, the host read accesses to the corresponding memory segment are claimed by the 82443BX and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI.

WE **Write Enable**. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the 82443BX and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 3-2.

Table 3-2. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
x	x	0	0	**Disabled.** DRAM is disabled and all accesses are directed to PCI. The 82443BX does not respond as a PCI target for any read or write access to this area.
x	x	0	1	**Read Only.** Reads are forwarded to DRAM and writes are forwarded to PCI for termination. This write protects the corresponding memory segment. The 82443BX will respond as a PCI target for read accesses but not for any write accesses.
x	x	1	0	**Write Only.** Writes are forwarded to DRAM and reads are forwarded to the PCI for termination. The 82443BX will respond as a PCI target for write accesses but not for any read accesses.
x	x	1	1	**Read/Write.** This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by the 82443BX and forwarded to DRAM. The 82443BX will respond as a PCI target for both read and write accesses.

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process, the BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. Table 3-3 shows the PAM registers and the associated attribute bits:

Table 3-3. PAM Registers and Associated Memory Segments

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	R	WE	RE	0F0000h – 0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h – 0C3FFFh	ISA Add-on BIOS[1]	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h – 0C7FFFh	ISA Add-on BIOS[1]	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h – 0CBFFFh	ISA Add-on BIOS[1]	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h – 0CFFFFh	ISA Add-on BIOS[1]	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h – 0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h – 0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h – 0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h – 0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h – 0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h – 0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h – 0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h – 0EFFFFh	BIOS Extension	5Fh

NOTE:
1. The C0000h to CFFFFh segment can be used for SMM space if enabled by the SMRAM register

DOS Application Area (00000h–9FFFh)

The DOS area is 640 KB and it is further divided into two parts. The 512 KB area at 0 to 7FFFFh is always mapped to the main memory controlled by the 82443BX, while the 128 KB address range from 080000 to 09FFFFh can be mapped to PCI or to main DRAM. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI) via 82443BX's FDHC configuration register.

Video Buffer Area (A0000h–BFFFFh)

This 128 KB area is not controlled by attribute bits. The host-initiated cycles in this region are always forwarded to either PCI or AGP unless this range is accessed in SMM mode. ***Routing of accesses is controlled by the Legacy VGA control mechanism of the "virtual" PCI-to-PCI bridge device embedded within the 82443BX.***

This area can be programmed as SMM area via the SMRAM register. When used as a SMM space this range can not be accessed from PCI or AGP.

Expansion Area (C0000h–DFFFFh)

This 128 KB area is divided into eight 16 KB segments which can be assigned with different attributes via PAM control register as defined by Table 3-3.

Extended System BIOS Area (E0000h–EFFFFh)

This 64 KB area is divided into four 16 KB segments which can be assigned with different attributes via PAM control register as defined by the Table 3-3.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64 KB segment which can be assigned with different attributes via PAM control register as defined by the Table 3-3.

3.3.18 DRB[0:7]—DRAM Row Boundary Registers (Device 0)

Address Offset: 60h (DRB0) – 67h (DRB7)
Default Value: 01h
Access: Read/Write
Size: 8 bits/register

The 82443BX supports 8 physical rows of DRAM. The width of a row is 64 bits. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 8 MB granularity. For example, a value of 01h indicates 8 MB.

60h DRB0 = Total memory in row0 (in 8 MB)
61h DRB1 = Total memory in row0 + row1 (in 8 MB)
62h DRB2 = Total memory in row0 + row1 + row2 (in 8 MB)
63h DRB3 = Total memory in row0 + row1 + row2 + row3 (in 8 MB)
64h DRB4 = Total memory in row0 + row1 + row2 + row3 + row4 (in 8 MB)
65h DRB5 = Total memory in row0 + row1 + row2 + row3 + row4 + row5 (in 8 MB)
66h DRB6 = Total memory in row0 + row1 + row2 + row3 + row4 + row5 + row6 (in 8 MB)
67h DRB7 = Total memory in row0 + row1 + row2 + row3 + row4 + row5 + row6 + row7 (in 8 MB)

The DRAM array can be configured with single or double-sided DIMMs using 2MX8, 4Mx16, or 8Mx8 parts. The array also supports x4 width DRAM components on registered DIMMs. Each register defines an address range that will cause a particular CS# line (or RAS# in the EDO case) to be asserted (e.g., if the first DRAM row is minus 8 MB, then accesses within the 0 to 8 MByte range will cause CSx0#/RASx0# to be asserted). The DRAM Row Boundary (DRB) Registers are programmed with an 8-bit upper address limit value. This upper address limit is compared to bits [30:23] of the requested address, for each row, to determine if DRAM is being targeted.

Note: DRAM is selected only if address[31:30] are zero.

Bit	Description
7:0	**Row Boundary Address.** This 8-bit value is compared against address lines A[30:23] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB = row size). NOTE: When PCIRST# assertion occurs during POS/STR, these bits are not reset to '01h'.

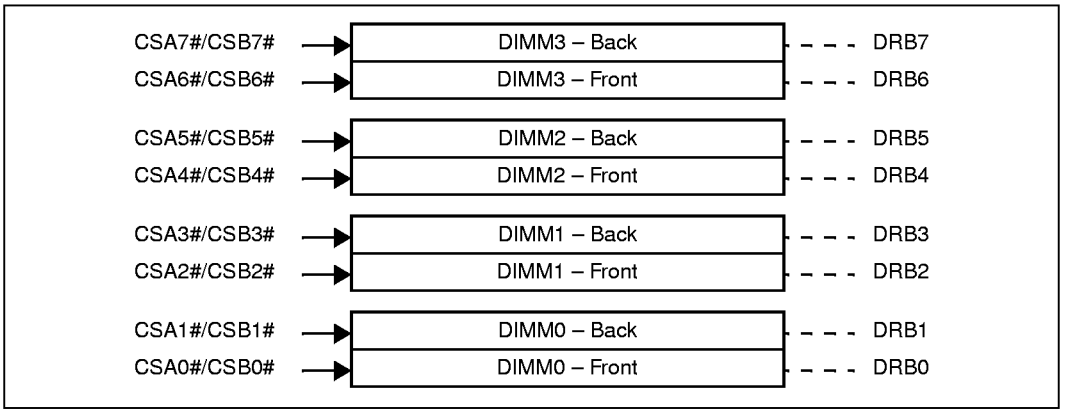
Row Boundary Address

These 8 bit values represent the upper address limits of the eight rows (i.e., this row minus previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). DRB7 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB7.

Note: The 82443BX supports a maximum of 1 GB of DRAM using registered SDRAM DIMMs. (an example of this configuration is 4 double-sided registered DIMMs using 16Mx4 parts).

As an example of a general purpose configuration where eight physical rows are configured for either single-sided or double-sided DIMMs, the memory array would be configured like the one shown in Figure 3-2. In this configuration, the 82443BX drives eight CS# signals directly to the DIMM rows. If single-sided DIMMs are populated, the even CS# signals are used and the odd CS#s are not connected. If double-sided DIMMs are used, all four CS# signals are used per DIMM.

Figure 3-2. SDRAM DIMMs and Corresponding DRB Registers



The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided DIMMs on a motherboard.

Example #1 Single-sided DIMMs

Assume a total of 16 MB of DRAM are required using single-sided 1MB x 64 DIMMs. In this configuration, two DIMMs are required.

DRB0 = 01h	populated (1 DIMM, 8 Mbyte this row)
DRB1 = 01h	empty row
DRB2 = 02h	populated (1 DIMM, 8 Mbyte this row)
DRB3 = 02h	empty row
DRB4 = 02h	empty row
DRB5 = 02h	empty row
DRB6 = 02h	empty row
DRB7 = 02h	empty row

Example #2 Mixed Single-/Double-sided DIMMs

As another example, consider a system that is initially shipped with 8 MB of memory using a 1M x 64 DIMM and that rest of the memory array should be upgradable up to a maximum supported memory of 200 MB. This can be handled by further populating the array with one 16M x 64 single-sided DIMM (one row) and one 8M x 64 double-sided DIMM (two rows), yielding a total of 200 MB of DRAM. The DRB Registers are programmed as follows:

DRB0 = 01h	populated with 8 MB, 1MB x 64 single-sided DIMM
DRB1 = 01h	empty row
DRB2 = 05h	populated with 32 MB, 1/2 of 8M x 64 DIMM
DRB3 = 09h	populated with 32 MB, the other 1/2 of 8M x 64 DIMM
DRB4 = 19h	populated with 128 MB, 16M x 64 single-sided DIMM
DRB5 = 19h	empty row
DRB6 = 19h	empty row
DRB7 = 19h	empty row

3.3.19 FDHC—Fixed DRAM Hole Control Register (Device 0)

Address Offset: 68h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This 8-bit register controls 2 fixed DRAM holes: 512 KB – 640 KB and 15 MB –16 MB.

Bit	Description
7:6	**Hole Enable (HEN).** This field enables a memory hole in DRAM space. Host cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole will be ignored by the 82443BX (no DEVSEL#). NOTE: A selected hole is not remapped. 00 = None 01 = 512 KB–640 KB (128 KB bytes) 10 = 15 MB – 16 MB (1 MB byte) 11 = Reserved
5:0	Reserved.

3.3.20 MBSC—Memory Buffer Strength Control Register (Device 0)

Address Offset: 69–6Eh
Default Value: 000000000000h
Access: Read/Write
Size: 48 bits

This register programs the various DRAM interface signal buffer strengths, based on non-mixed memory configurations of DRAM type (EDO or SDRAM), DRAM density (x8, x16, or x32), DRAM technology (16MB or 64 MB), and rows populated. Note that x4 DRAM may only be supported when used on registered DIMMs.

Note: The choice of 100 MHz or 66 MHz buffer is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vice versa).

Bit	Description
47:40	Reserved
39:38	**MAA[13:0], WEA#, SRASA#, SCASA# Buffer Strengths.** This field sets the buffer strength for the MAA[13:0], WEA#, SRASA#, SCASA# pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
37:36	**MAB[12:11, 9:0]# & MAB[13,10], WEB#, SRASB#, SCASB# Buffer Strengths.** This field sets the buffer strength for MAB[12:11, 9:0]# & MAB[13,10], WEB#, SRASB#, SCASB# pins. Note that the address's MAB# are inverted copies of MAA, with the exception of MAB[13,10]. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
35:34	**MD [63:0] Buffer Strength Control 2.** **4 DIMM FET Configuration:** This field sets the buffer strength for the MD[63:0] path that is connected to DIMM2 and DIMM3. The buffer strength is programmable based on the SDRAM load in detected in **DIMM slots 2&3**. This path is enabled when FENA is asserted (High) by the 82443BX. **3 DIMM & 4 DIMM non-FET Configuration:** This field should be programmed to the same value as MD[63:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (100 MHz only)
33:32	**MD [63:0] Buffer Strength Control 1.** **4 DIMM FET Configuration:** This field sets the buffer strength for the MD[63:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM load in detected in **DIMM slots 0&1.** This path is enabled when FENA is asserted (Low) by the 82443BX. **3 DIMM & 4 DIMM non-FET Configurations:** The buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (100 MHz only)

Bit	Description
31:30	**MECC [7:0] Buffer Strength Control 2.** **4 DIMM FET Configuration:** This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM2 and DIMM3 The buffer strength is programmable based upon the SDRAM ECC load detected in **DIMM slots 2&3**. This path is enabled when FENA is deasserted (High) by the 82443BX. **3 DIMM & 4 DIMM non-FET Configurations:** This field should be programmed to the same value as MECC[7:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM load detected in all DIMM connectors. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (100 MHz only)
29:28	**MECC [7:0] Buffer Strength Control 1.** **4 DIMM FET Configuration:** This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM ECC load detected in **DIMM slots 0&1.** This path is enabled when FENA is deasserted (High) by the 82443BX. **3 DIMM & 4 DIMM non-FET Configuration:** The buffer strength is programmable based upon the SDRAM ECC load detected in all DIMM slots. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (100 MHz only)
27:26	**CSB7#/CKE5 Buffer Strength.** This field sets the buffer strength for CSB7#/CKE5 pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
25:24	**CSA7#/CKE3 Buffer Strength.** This field sets the buffer strength for CSA7#/CKE3 pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
23:22	**CSB6#/CKE4 Buffer Strength.** This field sets the buffer strength for CSB6#/CKE4 pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
21:20	**CSA6#/CKE2 Buffer Strength.** This field sets the buffer strength for CSA6#/CKE2pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
19	**CSA5#/RASA5#, CSB5#/RASB5# Buffer Strength.** This field sets the buffer strength for the CSA5#/RASA5#, CSB5#/RASB5# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
18	**CSA4#/RASA4#, CSB4#/RASB4# Buffer Strength.** This field sets the buffer strength for the CSA4#/RASA4#, CSB4#/RASB4# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
17	**CSA3#/RASA3#, CSB3#/RASB3# Buffer Strength.** This field sets the buffer strength for the CSA3#/RASA3#, CSB3#/RASB3# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)

Bit	Description
16	**CSA2#/RASA2#, CSB2#/RASB2# Buffer Strength.** This field sets the buffer strength for the CSA2#/RASA2#, CSB2#/RASB2# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
15	**CSA1#/RASA1#, CSB1#/RASB1# Buffer Strength.** This field sets the buffer strength for the CSA1#/RASA1#, CSB1#/RASB1# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
14	**CSA0#/RASA0#, CSB0#/RASB0# Buffer Strength.** This field sets the buffer strength for the CSA0#/RASA0#, CSB0#/RASB0# pins. 0 = 1x (66 MHz & 100 MHz) 1 = 2x (66 MHz & 100 MHz)
13:12	**DQMA5/CASA5# Buffer Strength.** This field sets the buffer strength for the DQMA5/CASA5# pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz only)
11:10	**DQMA1/CASA1# Buffer Strength.** This field sets the buffer strength for the DQMA1/CASA1# pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
9:8	**DQMB5/CASB5# Buffer Strength.** This field sets the buffer strength for the DQMB5/CASB5# pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz only)
7:6	**DQMB1/CASB1# Buffer Strength.** This field sets the buffer strength for the DQMB1/CASB1# pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz only)
5:4	**DQMA[7:6,4:2,0]/CASA[7:6,4:2,0]# Buffer Strength.** This field sets the buffer strength for the DQMA[7:6]/CASA[7:6]#, DQMA[4:2]/CASA[4:2]#, and the DQMA[0]/CASA[0]# pins. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
3:2	**CKE1/GCKE Buffer Strength.** This field sets the buffer strength for the CKE1 pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)
1:0	**CKE0/FENA Buffer Strength.** This field sets the buffer strength for the CKE0/FENA pin. 00 = 1x (66 MHz & 100 MHz) 01 = Reserved (Invalid setting) 10 = 2x (66 MHz & 100 MHz) 11 = 3x (66 MHz & 100 MHz)

3.3.21 SMRAM—System Management RAM Control Register (Device 0)

Address Offset: 72h
Default Value: 02h
Access: Read/Write
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Description
7	Reserved
6	**SMM Space Open (D_OPEN).** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only.
5	**SMM Space Closed (D_CLS).** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference "through" SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
4	**SMM Space Locked (D_LCK).** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, H_SMRAM_EN, TSEG_SZ, TSEG_EN and DRB7 become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRAME).** If G_SMRAME is set to a 1 and H_SMRAM_EN is set to 0, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG) (RO).** This field programs the location of SMM space. "SMM DRAM" is not remapped. It is simply "made visible" if the conditions are right to access SMM space, otherwise the access is forwarded to PCI. 010 = Hardwired to 010 to indicate that the 82443BX supports the SMM space at A0000h–BFFFFh.

3.3.22 ESMRAMC—Extended System Management RAM Control Register (Device 0)

Address Offset: 73h
Default Value: 38h
Access: Read/Write
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 Mbyte.

Bit	Description
7	**H_SMRAM_EN (H_SMRAME).** Controls the SMM memory space location (i.e above 1 Mbyte or below 1 Mbyte). 1 = When G_SMRAME is 1 and H SMRAME is set to 1, the High SMRAM memory space is enabled, the Compatible SMRAM memory is disabled, and accesses in the 0A0000h to 0FFFFFh range are forwarded to PCI, while SMRAM accesses from 100A0000h to 100FFFFFh are remapped to DRAM address A0000h to FFFFFh 0 = When G SMRAME is set to a 1 and H SMRAM EN is set to 0, then the Compatible SMRAM space is enabled. Once D_LCK is set, this bit becomes read only.
6	**E_SMRAM_ERR (E_SMERR).** 1 = This bit is set when CPU accesses the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. 0 = It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	**SMRAM_Cache (SM_CACHE).** This bit is forced to '1' by 82443BX.
4	**SMRAM_L1_EN (SM_L1).** This bit is forced to '1' by 82443BX.
3	**SMRAM_L2_EN (SM_L2).** This bit is forced to '1' by 82443BX.
2:1	**TSEG_SZ[1:0] (T_SZ).** Selects the size of the TSEG memory block, if enabled. This memory is taken from the top of DRAM space (i.e., TOM - TSEG_SZ), which is no longer claimed by the memory controller (all accesses to this space are sent to the PCI bus if TSEG_EN is set). The physical address for the extended SMRAM memory appears is from (256M + TOM - TSEG_SZ) to (256M + TOM). This address is remapped to DRAM address (TOM - TSEG_SZ) to TOM. This field decodes as follows: 00 = (TOM–128KB) to TOM 01 = (TOM–256KB) to TOM 10 = (TOM–512KB) to TOM 11 = (TOM–1MB) to TOM Once D_LCK is set, this bit becomes read only.
0	**TSEG_EN (T_EN).** Enabling of SMRAM memory (TSEG, 128 KB, 256 KB, 512 KB or 1 MB of additional SMRAM memory) for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Once D_LCK is set, this bit becomes read only.

3.3.23 RPS—SDRAM Row Page Size Register (Device 0)

Address Offset: 74h–75h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register sets the row page size for SDRAM only. For EDO memory, the page size is fixed at 2 KB.

Bit	Description
15:0	**Page Size (PS).** Each pair of bits in this register indicate the page size used for one row of DRAM. The encoding of the two bit fields. **Bits[1:0] — Page Size** 00 — 2 KB 01 — 4 KB 10 — 8 KB 11 — Reserved **RPS bits — Corresponding DRB register** 1:0 — DRB[0], row 0 3:2 — DRB[1], row 1 5:4 — DRB[2], row 2 7:6 — DRB[3], row 3 9:8 — DRB[4], row 4 11:10 — DRB[5], row 5 13:12 — DRB[6], row 6 15:14 — DRB[7], row 7

3.3.24 SDRAMC—SDRAM Control Register (Device 0)

Address Offset: 76h–77h
Default Value: 00h
Access: Read/Write
Size: 16 bits

Bit	Description
15:10	Reserved
9:8	**Idle/Pipeline DRAM Leadoff Timing (IPDLT).** Adds a clock delay to the lead-off clock count when bits 9:8 are set to 01. All other settings are illegal.

Bit	Description
7:5	**SDRAM Mode Select (SMS).** These bits allow the 82443BX to drive various commands to the SDRAMs. These special modes are intended for initialization at power up. **SMS** **Mode** 000 **Normal SDRAM Operation.** (default) 001 **NOP Command Enable**. In this mode all CPU cycles to SDRAM result in NOP Command on the SDRAM interface. 010 **All Banks Precharge Enable**. In this mode all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface. 011 **Mode Register Set Enable**. In this mode all CPU cycles to SDRAM result in a mode register set command on the SDRAM interface. The Command is driven on the MAx[13:0] lines. MAx[2:0] must always be driven to 010 for burst of 4 mode. MA3 must be driven to 1 for interleave wrap type. MAx4 needs to be driven to the value programmed in the CAS# Latency bit. MAx[6:5] should always be driven to 01. MAx[12:7] must be driven to 000000. BIOS must calculate and drive the correct host address for each row of memory such that the correct command is driven on the MAx[12:0] lines. 100 **CBR Enable**. In this mode all CPU cycles to SDRAM result in a CBR cycle on the SDRAM interface. 101 **Reserved.** 110 **Reserved.** 111 **Reserved.** Note: BIOS must take into consideration MAB inversion when programming for 3 and 4 DIMM.
4	**SDRAMPWR.** The SDRAMPWR bit controls how the CKE signals are driven for different DRAM configurations. For a 3 DIMM configuration, SDRAMPWR should be set to '0'. For a 4 DIMM configuration, SDRAMPWR should be set to '1'. In this case the 82443BX drives a single CKE signal (GCKE). The combination of SDRAMPWR and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register (Section 3.3.15, "DRAMC—DRAM Control Register (Device 0)" on page 3-19) for more details. Note: When PCIRST# assertion occurs during POS/STR, these bits are not reset to 0.
3	**Leadoff Command Timing (LCT).** These bits control when the SDRAM command pins (SRASx#, SCASx# and WEx#) and CSx# are considered valid on leadoffs for CPU cycles. 0 = 4 CS# Clock 1 = 3 CS# Clock The LCT Bit should be initialized by BIOS as recommended below: • Desktop platforms running at 100 MHz should leave the LCT bit set to its default value of 0. • Desktop platforms running at 66 MHz should leave the LCT bit set to its default value of 0, if load on either MAA or MAB signals is > 9. Otherwise, set the LCT bit to 1, if load on both MAA and MAB is ≤ 9. • Mobile platforms will be run at 66MHz and should set the LCT bit to 1.
2	**CAS# Latency (CL).** This bit controls the number of CLKs between when a read command is sampled by the SDRAMs and when the 82443BX samples read data from the SDRAMs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command the when the 82443BX samples read data. For a registered DIMM with CL=2, this bit should be set to 1. 0 = 3 DCLK CAS# latency. 1 = 2 DCLK CAS# latency.
1	**SDRAM RAS# to CAS# Delay (SRCD).** This bit controls the number of DCLKs from a Row Activate command to a read or write command. 0 = 3 clocks will be inserted between a row activate command and either a read or write command. 1 = 2 clocks will be inserted between a row activate and either a read or write command.
0	**SDRAM RAS# Precharge (SRP).** This bit controls the number of DCLKs for RAS# precharge. 0 = 3 clocks of RAS# precharge. 1 = 2 clocks of RAS# precharge.

3.3.25 PGPOL—Paging Policy Register (Device 0)

Address Offset: 78–79h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:8	**Banks per Row (BPR).** Each bit in this field corresponds to one row of the memory array. Bit 15 corresponds to row 7 while bit 8 corresponds to row 0. These bits are defined only for SDRAM systems and define whether the corresponding row has a two bank implementation or a four bank implementation. Those with two banks (bit=0) can have up to two pages open at any given time. Those with four banks (bit=1) can have up to four pages open at any time. Note that the bits referencing empty rows are 'don't care'. 0 = 2 banks 1 = 4 banks
7:5	Reserved.
4	Intel Reserved.
3:0	**DRAM Idle Timer (DIT).** This field determines the number of clocks that the DRAM controller will remain in the idle state before precharging all pages. This field is used for both EDO and SDRAM memory systems. 0000 = 0 clocks 0001 = 2 clocks 0010 = 4 clocks 0011 = 8 clocks 0100 = 10 clocks 0101 = 12 clocks 0110 = 16 clocks 0111 = 32 clocks 1XXX = Infinite (pages are not closed for idle condition).

3.3.26 PMCR—Power Management Control Register (Device 0)

Address Offset: 7Ah
Default Value: 0000_S0S0b
Access Read/Write
Size 8 Bits

Bit	Description
7	**Power Down SDRAM Enable (PDSE).** 1 = Enable. When PDSE=1, an SDRAM row in idle state will be issued a power down command. The SDRAM row will exit power down mode only when there is a request to access this particular row. 0 = Disable
6	**ACPI Control Register Enable (SCRE).** 1 = Enable. The ACPI control register in the 82443BX is enabled, and all CPU cycles to IO address 0022h are handled by the 82443BX and are not forwarded to PCI. 0 = Disable (default). All CPU cycles to IO address 0022h are passed on to the PCI bus.
5	**Suspend Refresh Type (SRT).** This bit determines what type of EDO DRAM refresh is used during Power On Suspend (POS/STR) or Suspend to RAM modes. SRT has no effect on SDRAM refresh. 1 = Self refresh mode 0 = CBR fresh mode NOTE: When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.
4	**Normal Refresh Enable (NREF_EN).** This bit is used to enable normal refresh operation following a POS/STR state. After coming out of reset the software must set this bit before doing an access to memory. 1 = Enable 0 = Disable
3	**Quick Start Mode (QSTART) (RO).** 1 = Quick start mode of operation is enabled for the processor. This mode is entered using a strapping option that is sampled by the 82443BX and the CPU during reset. This register bit is Read Only and a configuration write to it is ignored.
2	**Gated Clock Enable (GCLKEN).** GCLKEN enables internal dynamic clock gating in the 82443BX when a AGPset "IDLE" state occurs. This happens when the 82443BX detects an idle state on all its buses. 1 = Enable 0 = Disable
1	**AGP Disable (AGP_DIS).** This register bit is Read Only and a configuration write to it is ignored. 1 = Disable. The AGP interface and the clocks of AGP associated logic are permanently disabled. This mode is entered using a strapping option that is sampled by the 82443BX during reset. 0 = Enable
0	**CPU reset without PCIRST enable (CRst_En).** This bit enables the 82443BX to assert CPU reset without an incoming PCIRST#. This option allows the reset of the processor when the system is coming out of POS state. Defaults to '0' upon PCIRST# assertion. 1 = Enable 0 = Disable NOTE: When PCIRST# assertion occurs during POS/STR, this bit is not reset to '0'.

3.3.27 SCRR—Suspend CBR Refresh Rate Register (Device 0)

Address Offset: 7Bh–7Ch
Default Value: 0038h
Access Read/Write
Size 16 Bits

Bit	Description
15:13	Reserved.
12	**Suspend CBR refresh Rate Auto Adjust Enable (SRRAEN).** SRRAEN bit is cleared to its default during cold reset only. It is not affected by PCIRST# during resume from suspend. 0 = Disable (default). Indicates that the suspend CBR refresh rate is not updated by the 82443BX hardware to track the system operating conditions. In this case, it is expected that BIOS will set the SRR to reflect the worst case operating conditions so that minimum refresh rate will be provided. 1 = Enable. Indicates that the 82443BX hardware adjusts the suspend refresh rate according to system operating conditions by comparing the number of OSCCLKs in a given time. This mode allows the system to dynamically adjust the refresh rate and thus minimize suspend power consumption while guaranteeing required refresh rate.
11:0	**Suspend CBR Refresh Rate (SRR).** The rate is loaded into the counter which counts down on OSCCLK rising edges. When it expires, a suspend CBR refresh request is triggered. This bit field may be loaded by BIOS to reflect the desirable refresh rate. In addition, the 82443BX will update it automatically, when the above SRRAEN = 1. In either case, the register is accessible for read and write operation at all times. • This 12-bit field provides a dynamic range greater than the maximum CBR refresh rate that is supported of 249.6uSEC. • SRR bit field is cleared to its default during cold reset only. It is not affected by PCIRST# during resume from suspend. • The default value of this register is 038h, or 56 decimal. It represents a 15.5uS time between refreshes with the slowest corner OSCCLK cycle time of 270nS.

3.3.28 EAP—Error Address Pointer Register (Device 0)

Address Offset: 80–83h
Default Value: 00000000h
Access Read Only, Read/Write-Clear
Size 32 Bits

Bit	Description
31:12	**Error Address Pointer (EAP) (RO).** This field is used to store the 4 KB block of main memory of which an error (single bit or multi-bit error) has occurred. Note that this field represents the address of the first error occurrence after bits 1:0 have been cleared by software. Once bits 1:0 are set to a value different than 00b, as a result of an error, this bit field is locked and doesn't change as a result of a new error.
11:2	Reserved.
1	**Multiple Bit Error (MBE) (R/WC).** This bit indicates that a multi-bit ECC error has occurred, and the address has been logged in bits 31:12. The EAP register is locked until the CPU clears this bit by writing a 1. Software uses bits 1:0 to detect whether the logged error address is for Single or Multi bit error, since both Single and Multiple Error bits of the Error Status register can be set. Once software completes the error processing, a value of '1' is written to this bit field to clear the value (back to 0) and unlock the error logging mechanism. Note: Any ECC errors received during initialization should be ignored.
0	**Single Bit Error (SBE) (R/WC).** 1 = Indicates that a single bit ECC error has occurred, and the address has been logged in bits 31:12. The EAP register is locked until the CPU clears this bit by writing a 1. Note: Any ECC errors received during initialization should be ignored.

3.3.29 ERRCMD—Error Command Register (Device 0)

Address Offset: 90h
Default Value: 80h
Access: Read/Write
Size: 8 bits

This 8-bit register controls the 82443BX responses to various system errors. The actual assertion of SERR# is enabled via the PCI Command register.

Bit	Description
7	**SERR# on AGP Non-Snoopable Access Outside of Graphics Aperture.** When enabled and bit 10 of ERRSTS registers transitions from 0 to 1 (during an AGP access to the address outside of the graphics aperture) then an SERR# assertion event will be generated. 1 = Enable (default). 0 = Disable.
6	**SERR# on Invalid AGP DRAM Access.** AGP non-snoopable READ accesses to locations outside the graphics aperture and outside the main DRAM range (i.e., in 640 KB – 1 MB range or above top of memory) are invalid. When this bit is set, bit 9 of the ERRSTS will be set and SERR# will be asserted, read accesses are not directed to main memory or the aperture range. 1 = Enable. 0 = Disable reporting of this condition via SERR#.
5	**SERR# on Access to Invalid Graphics Aperture Translation Table Entry.** When enabled, the 82443BX sets bit 8 of the ERRSTS and asserts SERR# following a read or write access to an invalid entry in the Graphics Aperture Translation Table residing in main memory. 1 = Enable. 0 = Disable reporting of this condition via SERR#.
4	**SERR# on Receiving Target Abort.** 1 = Enable. The 82443BX asserts SERR# on receiving a target abort on either the PCI or AGP. 0 = Disable. The 82443BX does not assert SERR# on receipt of a target abort.
3	**SERR# on Detected Thermal Throttling Condition.** 1 = Enable. The 82443BX asserts SERR# when thermal throttling condition is detected for either the read or the write function. 0 = The 82443BX does not assert SERR# for thermal throttling.
2	**SERR# Assertion Mode.** 1 = SERR# is a level mode signal. Systems that connect SERR# to EXTSMI# for error reporting should set this bit to 1. 0 = SERR# is asserted for 1 PCI clock (normal PCI mode). (default)
1	**SERR# on Receiving Multiple-Bit ECC/Parity Error.** When enabled, the 82443BX asserts SERR# when it detects a multiple-bit error reported by the DRAM controller. For systems not supporting ECC this bit must be disabled. 1 = Enable. 0 = Disable. Note: Any ECC errors received during initialization should be ignored.
0	**SERR# on Receiving Single-bit ECC Error.** When enabled, the 82443BX asserts SERR# when it detects a single-bit ECC error. For systems not supporting ECC, this bit must be disabled. 1 = Enable. 0 = Disable. Note: Any ECC errors received during initialization should be ignored.

3.3.30 ERRSTS—Error Status Register (Device 0)

Address Offset: 91–92h
Default Value: 0000h
Access: Read Only, Read/Write Clear
Size: 16 bits

This 16-bit register is used to report error conditions via the SERR# mechanism. SERR# is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD register).

Bit	Description
15:13	Reserved.
12	**Read thermal Throttling Condition.** 1 = Read thermal throttling condition occurred. 0 = Software writes "1" to clear this bit. Default=0
11	**Write Thermal Throttling Condition.** 1 = Write thermal throttling condition occurred. 0 = Software writes "1" to clear this bit. Default=0
10	**AGP non-snoopable access outside of Graphics Aperture.** 1 = AGP access occurred to the address that is outside of the graphics aperture range. 0 = Software writes "1" to clear this bit. Default=0
9	**Invalid AGP non-snoopable DRAM read access (R/WC).** 1 = AGP non-snoopable READ access was attempted outside of the graphics aperture and outside of main memory (i.e,. in 640 KB – 1 MB range or above top of memory). 0 = Software must write a "1" to clear this status bit.
8	**Access to Invalid Graphics Aperture Translation Table Entry (AIGATT) (R\WC).** 1 = An invalid translation table entry was returned in response to a graphics aperture read or write access. 0 = Software must write a "1" to clear this bit.
7:5	**Multi-bit First Error (MBFRE) (RO).** This field contains the encoded value of the DRAM row in which the first multi-bit error occurred. A simple binary encoding is used to indicate the row containing the multi-bit error. When an error is detected, this field is updated and the MEF bit is set. This field will then be locked (no further updates) until the MEF flag has been reset. If MEF is 0, the value in this field is undefined. 000 = Row 0 001 = Row 1 … 111 = Row 7
4	**Multiple-bit ECC (uncorrectable) Error Flag (MEF) (R/WC).** 1 = Memory data transfer had an uncorrectable error(i.e., multiple-bit error). When enabled, a multiple bit error is reported by the DRAM controller and propagated to the SERR# pin, if enabled by bit 1 in the ERRCMD register. 0 = BIOS writes a 1 to clear this bit and unlock the MBFRE field. (Default = 0).
3:1	**Single-bit First Row Error (SBFRE) (RO).** This field contains the encoded value of the DRAM row in which the first single-bit error occurred. A simple binary encoding is used to indicate the row containing the single-bit error. When an error is detected, this field is updated and SEF is set. This field is then locked (no further updates) until the SEF flag has been reset. If SEF is 0, the value in this field is undefined. 000 = Row 0 001 = Row 1 … 111 = Row 7
0	**Single-bit (correctable) ECC Error Flag (SEF) (R/WC).** 1 = Memory data transfer had a single-bit correctable error and the corrected data was sent for the access. When ECC is enabled, a single bit error is reported and propagated to the SERR# pin, if enabled by bit 0 in the ERRCMD register. 0 = BIOS writes a 1 to clear this bit and unlock the SBFRE field.

3.3.31 ACAPID—AGP Capability Identifier Register (Device 0)

Address Offset: A0–A3h
Default Value: 00100002h/00000000h
Access: Read Only
Size: 32 bits

This register provides normal identifier for AGP capability.

Bit	Description
31:24	Reserved
23:20	**Major AGP Revision Number.** This field provides a major revision number of AGP specification to which this version of the 82443BX conforms. When the AGP DIS bit (PMCR[1]) is set to 0, this number is set to value of "0001b" (i.e., implying Rev 1.x). When the AGP DIS bit (PMCR[1]) is set to 1, This number is set to "0000b".
19:16	**Minor AGP Revision Number.** These bits provide a minor revision number of AGP specification to which this version of 82443BX conforms. This number is hardwired to value of "0000" (i.e., implying Rev x.0). Together with major revision number this field identifies 82443BX as an AGP REV 1.0 compliant device.
15:8	**Next Capability Pointer.** AGP capability is the first and the last capability described via the capability pointer mechanism. 0s = Hardwired to 0s to indicate the end of the capability linked list.
7:0	**AGP Capability ID.** This field identifies the linked list item as containing AGP registers. When the AGP DIS bit (PMCR[1]) is set to 0, this field has a value of 0000_0010b assigned by the PCI SIG. When the AGP DIS bit (PMCR[1]) is set to 1, this field has a value of 00h.

3.3.32 AGPSTAT—AGP Status Register (Device 0)

Address Offset: A4–A7h
Default Value: 1F000203h
Access: Read Only
Size: 32 bits

This register reports AGP compliant device capability/status.

Bit	Description
31:24	**AGP Maximum Request Queue Depth (RO).** This field is hardwired to 1Fh to indicate a maximum of 32 outstanding AGP command requests can be handled by the 82443BX.
23:10	Reserved
9	**AGP Side Band Addressing Supported.** This bit indicates that the 82443BX supports side band addressing. It is hardwired to 1.
8:2	Reserved
1:0	**AGP Data Transfer Type Supported (R/W).** Bit 0 identifies if AGP compliant device supports 1x data transfer mode and bit 1 identifies if AGP compliant device supports 2x data transfer mode. Configuration software will update this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP masters configuration space). 00 = Not allowed 01 = 1x data transfer mode supported 10 = 2x data transfer mode supported 11 = (default) NOTE: The selected data transfer mode apply to both AD bus and SBA bus.

3.3.33 AGPCMD—AGP Command Register (Device 0)

Address Offset: A8–ABh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides control of the AGP operational parameters.

Bit	Description
31:10	Reserved.
9	**AGP Side Band Enable.** This bit enables the side band addressing mechanism. 1 = Enable. 0 = Disable.
8	**AGP Enable.** When disabled, the 82443BX ignores all AGP operations, including the sync cycle. Any AGP operations received while this bit is set to 1 is serviced even if this bit is reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1X mode the command will be issued. When this bit is set to 1 the 82443BX will respond to AGP operations delivered via PIPE#, or to operations delivered via SBA if the AGP Side Band Enable bit is also set to 1. The AGP parameters in the AGPCMD and AGPCTRL registers must be set prior to setting this bit '1'. With the exception of the GTLB_ENABLE (bit 7, AGPCTRL), and ATTBASE register (offset B8h), which can be modified dynamically. 1 = Enable. 0 = Disable.
7:2	Reserved.
1:0	**AGP Data Transfer Rate.** One (and only one) bit in this field must be set to indicate the desired data transfer rate (Bit 0 for 1X, Bit 1 for 2X). The same bit must be set on both master and target. Configuration software will update this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP masters configuration space.) 00 = default 01 = 1x data transfer rate. 10 = 2x data transfer rate. 11 = Illegal NOTE: This field applies to AD and SBA buses.

3.3.34 AGPCTRL—AGP Control Register (Device 0)

Address Offset: B0–B3h
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides for additional control of the AGP interface.

Bit	Description
31:16	Reserved.
15	**Snoopable Writes In Order With AGP Reads Disable (AGPDCD).** When set to 0 (default), the 82443BX maintains ordering between snoopable write cycles and AGP reads. When set to 1, the 82443BX handles the AGP reads and snoopable writes as independent streams. **AGPDCD (Bit 15) / AGPRSE (Bit 13) / Description** 0 / 0 / DWB is visible to AGP reads. DWB flushes only when address hit. 0 / 1 / Illegal. 1 / 0 / Illegal 1 / 1 / DWB flushes when write to AGP occurs
14	Reserved
13	**Graphics Aperture Write-AGP Read Synchronization Enable (AGPRSE).** When this bit is set the 82443BX will ensure that all writes posted in the Global Write Buffer to the Graphics Aperture are retired to DRAM before the 82443BX will initiate any CPU-to-AGP cycle. This can be used to ensure synchronization between the CPU and AGP master. The AGPDCD bit description defines the interaction between the AGPRSE bit and the AGPDCD bit. 1 = Enable 0 = Disable (Default)
12:8	Reserved
7	**GTLB Enable (and GTLB Flush Control).** 1 = Enable. Normal operations of the Graphics Translation Lookaside Buffer. 0 = Disable (default). The GTLB is flushed by clearing the valid bits associated with each entry.
6:0	Reserved.

3.3.35 APSIZE—Aperture Size Register (Device 0)

Address Offset: B4h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register determines the effective size of the Graphics Aperture used for a particular 82443BX configuration. This register can be updated by the 82443BX-specific BIOS configuration sequence before the PCI normal bus enumeration sequence takes place. If the register is not updated, a default value selects an aperture of maximum size (i.e., 256 MB). The size of the table that will correspond to a 256 MB aperture is not practical for most applications and, therefore, these bits must be programmed to a smaller practical value that forces adequate address range to be requested via the APBASE register from the PCI configuration software.

Bit	Description
7:6	Reserved.
5:0	**Graphics Aperture Size (APSIZE) (R/W).** Each bit in APSIZE[5:0] operates on similarly ordered bits in APBASE[27:22] of the Aperture Base configuration register. When a particular bit of this field is "0", it forces the similarly ordered bit in APBASE[27:22] to behave as "hardwired" to 0. When a particular bit of this field is set to "1", it allows corresponding bit of the APBASE[27:22] to be read/write accessible. Only the following combinations are allowed: 11 1111 = 4 MB 11 1110 = 8 MB 11 1100 = 16 MB 11 1000 = 32 MB 11 0000 = 64 MB 10 0000 = 128 MB 00 0000 = 256MB Default for APSIZE[5:0]=000000b forces default APBASE[27:22] =000000b (i.e., all bits respond as "hardwired" to 0). This provides maximum aperture size of 256 MB. As another example, programming APSIZE[5:0]=111000b hardwires APBASE[24:22]=000b and while enabling APBASE[27:25] as read/write programmable.

3.3.36 ATTBASE—Aperture Translation Table Base Register (Device 0)

Address Offset: B8–BBh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table base located in the main DRAM. The ATTBASE register may be dynamically changed.

Note: The address provided via ATTBASE is 4KB aligned.

Bit	Description
31:12	**Aperture Translation Table Base Address.** Bits 31:12 correspond to address bits 31:12, respectively. This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory.
11:0	Reserved.

3.3.37 MBFS—Memory Buffer Frequency Select Register (Device 0)

Address Offset: CA–CCh
Default Value: 000000h
Access: Read/Write
Size: 24 bits

The settings in this register enable the 100 MHz or 66 MHz buffers for each of the following signal groups.

Note: The choice of 100 MHz or 66 MHz buffer is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vice versa).

Bit	Description
23	Reserved
22	**MAA[13:0], WEA#, SRASA#, SCASA# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for MAA[13:0], WEA#, SRASA#, SCASA#. 0 = 66 MHz 1 = 100 MHz
21	**MAB[12:11, 9:0]# & MAB[13,10], WEB#, SRASB#, SCASB# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for MAB[12:11, 9:0]# & MAB[13,10], WEB#, SRASB#, SCASB#. Note that the address's MABx# are inverted copies of MAA, with the exception of MAB[13,10]. 0 = 66 MHz 1 = 100 MHz
20	**MD [63:0] (100 MHz/66 MHz buffer select bit [Control 2]).** This bit enables either 100 MHz or 66 MHz buffers for MD [63:0] [Control 2]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
19	**MD [63:0] (100 MHz/66 MHz buffer select bit [Control 1]).** This bit enables either 100 MHz or 66 MHz buffers for MD [63:0] [Control 1]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
18	**MECC [7:0] (100 MHz/66 MHz buffer select bit [Control 2]).** This bit enables either 100 MHz or 66 MHz buffers for MECC [7:0] [Control 2]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
17	**MECC [7:0] (100 MHz/66 MHz buffer select bit [Control 1]).** This bit enables either 100 MHz or 66 MHz buffers for MECC [7:0] [Control 1]. (Refer to the corresponding MBSC register for programming details). 0 = 66 MHz 1 = 100 MHz
16	**CSB7#/CKE5 (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSB7#/CKE5. 0 = 66 MHz 1 = 100 MHz

Bit	Description
15	**CSA7#/CKE3 (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSA7#/CKE3. 0 = 66 MHz 1 = 100 MHz
14	**CSB6#/CKE4 (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSB6#/CKE4. 0 = 66 MHz 1 = 100 MHz
13	**CSA6#/CKE2 (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSA6#/CKE2. 0 = 66 MHz 1 = 100 MHz
12	**CSA5#/RASA5#, CSB5#/RASB5# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSA5#/RASA5#, CSB5#/RASB5#. 0 = 66 MHz 1 = 100 MHz
11	**CSA4#/RASA4#, CSB4#/RASB4# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSA4#/RASA4#, CSB4#/RASB4#. 0 = 66 MHz 1 = 100 MHz
10	**CSA3#/RASA3#, CSB3#/RASB3# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSA3#/RASA3#, CSB3#/RASB3#. 0 = 66 MHz 1 = 100 MHz
9	**CSA2#/RASA2#, CSB2#/RASB2# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSA2#/RASA2#, CSB2#/RASB2#. 0 = 66 MHz 1 = 100 MHz
8	**CSA1#/RASA1#, CSB1#/RASB1# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CSA1#/RASA1#, CSB1#/RASB1#. 0 = 66 MHz 1 = 100 MHz
7	CSA0#/RASA0#, CSB0#/RASB0# (100 MHz/66 MHz buffer select bit). This bit enables either 100 MHz or 66 MHz buffers for CSA0#/RASA0#, CSB0#/RASB0#. 0 =66 MHz 1 = 100 MHz
6	**DQMA5/CASA5# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for DQMA5/CASA5#. 0 = 66 MHz 1 = 100 MHz
5	**DQMA1/CASA1# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for DQMA1/CASA1#. 0 = 66 MHz 1 = 100 MHz
4	**DQMB5/CASB5# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for DQMB5/CASB5#. 0 = 66 MHz 1 = 100 MHz

Bit	Description
3	**DQMB1/CASB1# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for DQMB1/CASB1#. 0 = 66 MHz 1 = 100 MHz
2	**DQMA[7:6,4:2,0]/CASA[7:6,4:2,0]# (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for DQMA[7:6]/CASA[7:6]#, DQMA[4:2]/CASA[4:2]#, and the DQMA[0]/CASA[0]#. 0 = 66 MHz 1 = 100 MHz
1	**CKE1/GCKE (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers forCKE1. 0 = 66 MHz 1 = 100 MHz
0	**CKE0/FENA (100 MHz/66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for CKE0/FENA. 0 = 66 MHz 1 = 100 MHz

3.3.38 BSPAD—BIOS Scratch Pad Register (Device 0)

Address Offset: D0–D7h
Default Value: 0000-0000-0000-0000h
Access: Read/Write
Size: 64 bits

This register provides 8 bytes general purpose read/write registers for the BIOS to perform the configuration routine. The 82443BX will provide this 8 byte register in the PCI configuration space of the 82443BX device0 on bus 0. The registers in this range will be defined as read/write and will be initialized to all 0's after PCIRST#. The BIOS will can access these registers through the normal PCI configuration register mechanism, accessing 1,2 or 4 bytes in every data access.

Bit	Description
64:0	**BIOS Work Space.**

3.3.39 DWTC—DRAM Write Thermal Throttling Control Register (Device 0)

Offset: E0h–E7h
Default: 0000_0000_0000_0000h
Access: Read/Write/Lock
Size: 64 bits

A locking mechanism is included to protect contents of this register as well as the DRAM Read Thermal Throttling Control register described below.

Bits	Description
63	**Throttle Lock (TLOCK).** This bit secures the DRAM thermal throttling control registers. 1 = All configuration register bits in E0h–E7h and E8h–EFh (read throttle control) become read-only. 0 = Default
62:46	Reserved
45:38	**Global DRAM Write Sampling Window (GDWSW).** This 8-bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of QWords written is counted.
37:26	**Global QWord Threshold (GQT).** The 12-bit value held in this field is multiplied by 215 to arrive at the number of QWords that must be written within the Global DRAM Write Sampling Window in order to cause the thermal throttling mechanism to be invoked.
25:20	**Throttle Time (TT).** This value provides a multiplier between 0 and 63 which specifies how long thermal throttling remains in effect as a number of Global DRAM Write Sampling Windows. For example, if GDWSW is programmed to 1000_0000b and TT is set to 01_0000b, then thermal throttling will be performed for ~2 seconds once invoked (128 ms * 16).
19:13	**Throttle Monitoring Window (TMW).** The value in this register is padded with four 0's to specify a window of 0–2047 DRAM CLKs with 16 clock granularity. While the thermal throttling mechanism is invoked, DRAM writes are monitored during this window—if the number of QWords written during the window reaches the Throttle QWord Maximum, then write requests are blocked for the remainder of the window.
12:3	**Throttle QWord Maximum (TQM).** The Throttle QWord Maximum defines the maximum number of QWords between 0–1023 which are permitted to be written to DRAM within one Throttle Monitoring Window while the thermal throttling mechanism is in effect.
2:0	**DRAM Write Throttle Mode.** Normal DRAM write monitoring and thermal throttling operation are enabled when bits 2:0 are set to 100. All other combinations are Intel Reserved. 000-011 = Intel Reserved 100 = Normal Operations 101-111 = Intel Reserved

3.3.40 DRTC—DRAM Read Thermal Throttling Control Register (Device 0)

Offset: E8h–EFh
Default: 0000_0000_0000_0000h
Access: Read/Write/Lock
Size: 64 Bits

The contents of this register are protected by making the bits read-only once a '1' is written to the Throttle Lock bit (bit 63 of configuration register E0–E7h)

Bits	Description
63:46	Reserved
45:38	**Global DRAM Read Sampling Window (GDRSW).** This 8-bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of QWords read from DRAM is counted.
37:26	**Global Read QWord Threshold (GRQT).** The 12-bit value held in this field is multiplied by 215 to arrive at the number of QWords that must be written within the Global DRAM Read Sampling Window in order to cause the thermal throttling mechanism to be invoked.
25:20	**Read Throttle Time (RTT**). This value provides a multiplier between 0 and 63 which specifies how long read thermal throttling remains in effect as a number of Global DRAM Read Sampling Windows. For example, if GDRSW is programmed to 1000_0000b and RTT is set to 01_0000b, then read thermal throttling will be performed for ~2 seconds once invoked (128 ms * 16).
19:13	**Read Throttle Monitoring Window (RTMW).** The value in this register is padded with 4 0's to specify a window of 0–2047 DRAM CLKs with 16 clock granularity. While the thermal throttling mechanism is invoked, DRAM reads are monitored during this window—if the number of QWords read during the window reaches the Throttle QWord Maximum, then Host and PCI read requests, as well as all AGP requests, are blocked for the remainder of the window.
12:3	**Read Throttle QWord Maximum (RTQM).** The Read Throttle QWord Maximum defines the maximum number of QWords between 0–1023 which are permitted to be read from DRAM within one Read Throttle Monitoring Window while thermal throttling mechanism is in effect.
2:0	**DRAM Read Throttle Mode.** Normal DRAM read monitoring and thermal throttling operation are enabled when bits 2:0 are set to 100. All other combinations are Intel Reserved. 000-011 = Intel Reserved 100 = Normal Operations 101-111 = Intel Reserved

3.3.41 BUFFC—Buffer Control Register (Device 0)

Offset: F0–F1h
Default: 0000h
Access: Read/Write
Size: 16 bits

The Jam Latch design provides the AGP sub-system with a variable strength, to better accommodate the clamping requirements.

The Jam Latch Register should be enabled by the BIOS during the resume sequence from STR, if these Jam Latch control bits had been enabled before the STR was executed.

Bit	Description
15:10	Reserved.
9:6	**AGP Jam Latch Strength Select.** Bit 9 = 1; Enable strong pull-up Bit 8 = 1; Enable weak pull-up Bit 7 = 1; Enable strong pull-down Bit 6 = 1; Enable weak pull-down
5:0	Intel Reserved.

3.4 PCI-to-PCI Bridge Registers (Device 1)

The configuration space for device #1 is controlled by the AGP_DIS bit in the PMCR register.

Note: When AGP_DIS = 0, the configuration space for device #1 is enabled, and the registers defined below are accessible through the configuration mechanism defined in the first section of this document.

Note: When the AGP_DIS = 1, the configuration space for device #1 is disabled. All configuration cycles (reads and writes) to device #1 of bus 0 will cause the master abort status bit for device #0/ bus 0 to be set. Configuration read cycles will return data of all 1's. Configuration write cycles will have no effect on the registers.

Table 3-4. 82443BX Configuration Space—Device 1

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	7191h	RO
04–05h	PCICMD1	PCI Command Register	0000h	R/W
06–07h	PCISTS1	PCI Status Register	0220h	RO, R/WC
08h	RID1	Revision Identification	00/01h	RO
09h	—	Reserved	00h	—
0Ah	SUBC1	Sub-Class Code	04h	RO
0Bh	BCC1	Base Class Code	06h	RO
0Ch	—	Reserved	00h	—
0Dh	MLT1	Master Latency Timer	00h	R/W
0Eh	HDR1	Header Type	01h	RO
0F–17h	—	Reserved	00h	—
18h	PBUSN	Primary Bus Number	00h	RO
19h	SBUSN	Secondary Bus Number	00h	R/W
1Ah	SUBUSN	Subordinate Bus Number	00h	R/W
1Bh	SMLT	Secondary Bus Master Latency Timer	00h	R/W
1Ch	IOBASE	I/O Base Address Register	F0h	R/W
1Dh	IOLIMIT	I/O Limit Address Register	00h	R/W
1E–1Fh	SSTS	Secondary PCI-to-PCI Status Register	02A0h	R/WC, RO
20–21h	MBASE	Memory Base Address Register	FFF0h	R/W
22–23h	MLIMIT	Memory Limit Address Register	0000h	R/W
24–25h	PMBASE	Prefetchable Memory Base Address Reg.	FFF0h	R/W
26–27h	PMLIMIT	Prefetchable Memory Limit Address Reg.	0000h	R/W
28–3Dh	—	Reserved	0	c
3Eh	BCTRL	Bridge Control Register	80h	R/W
3F–FFh	—	Reserved	00h	—

3.4.1 VID1—Vendor Identification Register (Device 1)

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number.** This is a 16-bit value assigned to Intel. Intel VID = 8086h.

3.4.2 DID1—Device Identification Register (Device 1)

Address Offset: 02–03h
Default Value: 7191h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number.** This is a 16 bit value assigned to the 82443BX device #1. 82443BX device #1 DID =7191h.

3.4.3 PCICMD1—PCI-to-PCI Command Register (Device 1)

Address Offset: 04–05h
Default: 0000h
Access: Read/Write
Size 16 bits

Bit	Descriptions
15:10	Reserved.
9	**Fast Back-to-Back:** Not Applicable. Hardwired to 0.
8	**SERR# Enable (SERRE1).** When enabled the SERR# signal driver (common for PCI and AGP) is enabled for error conditions that occur on AGP.If both SERRE and SERRE1 are reset to 0, then SERR# is never driven by the 82443BX. Also, if this bit is set and the Parity Error Response Enable Bit (Dev 01h, Register 3Eh, Bit 0) is set, then the 82443BX will report ADDRESS and DATA parity errors on AGP. 1 = Enable. 0 = Disable.
7	**Address/Data Stepping.** Not applicable. Hardwired to 0.
6	**Parity Error Enable (PERRE1).** Hardwired to 0.
5	**Reserved.**
4	**Memory Write and Invalidate Enable: Not applicable.** However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
3	**Special Cycle Enable: Not applicable.** However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
2	**Bus Master Enable (BME1): Not applicable.** However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
1	**Memory Access Enable (MAE1): Not applicable.** However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.
0	**I/O Access Enable (IOAE1): Not applicable.** However, supported as a read/write bit to avoid the problems with normal PCI-to-PCI Bridge configuration software.

3.4.4 PCISTS1—PCI-to-PCI Status Register (Device 1)

Address Offset: 06–07h
Default Value: 0220h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the "virtual" PCI-to-PCI bridge embedded within the 82443BX.

Bit	Descriptions
15	**Detected Parity Error (DPE1).** Not Applicable. Hardwired to 0.
14	Reserved.
13	**Received Master Abort Status (RMAS1).** Not Applicable. Hardwired to 0.
12	**Received Target Abort Status (RTAS1).** Not Applicable. Hardwired to 0.
11	**Signaled Target Abort Status (STAS1).** Not Applicable. Hardwired to 0.
10:9	**DEVSEL# Timing (DEVT1).** Not Applicable. Hardwired to "01b".
8	**Data Parity Detected (DPD1).** Not Applicable. Hardwired to 0.
7	**Fast Back-to-Back (FB2B1).** Not Applicable. Hardwired to 0.
6	Reserved.
5	**66/60 MHz Capability.** Hardwired to "1".
4:0	Reserved.

3.4.5 RID1—Revision Identification Register (Device 1)

Address Offset: 08h
Default Value: 00/01h
Access: Read Only
Size: 8 bits

This register contains the revision number of the 82443BX device #1. These bits are read only and writes to this register have no effect. For the A-0 Stepping, this value is 00h.

Bit	Description
7:0	**Revision Identification Number.** This is an 8-bit value that indicates the revision identification number for the 82443BX device #1. 02h = B1 stepping

3.4.6 SUBC1—Sub-Class Code Register (Device 1)

Address Offset: 0Ah
Default Value: 04h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the 82443BX device #1. This code is 04h indicating a PCI-to-PCI Bridge device. The register is read only.

Bit	Description
7:0	**Sub-Class Code (SUBC1).** This is an 8-bit value that indicates the category of Bridge into which the 82443BX falls. 04h = Host Bridge.

3.4.7 BCC1—Base Class Code Register (Device 1)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the 82443BX device #1. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	**Base Class Code (BASCC).** This is an 8-bit value that indicates the Base Class Code for the 82443BX device #1. 06h = Bridge device.

3.4.8 MLT1—Master Latency Timer Register (Device 1)

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to comply with the normal PCI-to-PCI bridge configuration software.

Bit	Description
7:3	**Not applicable but support read/write operations.** (Reads return previously written data.)
2:0	Reserved.

3.4.9 HDR1—Header Type Register (Device 1)

Offset: 0Eh
Default: 01h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**Header Type (HEADT).** This read only field always returns 01h when read. Writes have no effect.

3.4.10 PBUSN—Primary Bus Number Register (Device 1)

Offset: 18h
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies that "virtual" PCI-to-PCI bridge is connected to bus #0.

Bit	Descriptions
7:0	**Bus Number.** Hardwired to "0".

3.4.11 SBUSN—Secondary Bus Number Register (Device 1)

Offset: 19h
Default: 00h
Access: Read /Write
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" PCI-to-PCI bridge i.e. to AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	**Bus Number.** Programmable Default "0".

3.4.12 SUBUSN—Subordinate Bus Number Register (Device 1)

Offset: 1Ah
Default: 00h
Access: Read /Write
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below AGP.This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	**Bus Number.** Programmable.

3.4.13 SMLT—Secondary Master Latency Timer Register (Device 1)

Address Offset: 1Bh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register control the bus tenure of the 82443BX on AGP the same way the Device 0 MLT controls the access to the PCI bus.

Bit	Description
7:3	**Secondary MLT Counter Value.** The default is 0s (i.e,. SMLT disabled)
2:0	Reserved.

3.4.14 IOBASE—I/O Base Address Register (Device 1)

Address Offset: 1Ch
Default Value: F0h
Access: Read/Write
Size: 8 bits

This register control the CPU to AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Bit	Description
7:4	**I/O Address Base.** Corresponds to A[15:12] of the I/O address. Default = Fh
3:0	Reserved.

3.4.15 IOLIMIT—I/O Limit Address Register (Device 1)

Address Offset: 1Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register controls the CPU to AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Bit	Description
7:4	**I/O Address Limit.** Corresponds to A[15:12] of the I/O address. Default=0
3:0	**Reserved.** (Only 16 bit addressing supported.)

3.4.16 SSTS—Secondary PCI-to-PCI Status Register (Device 1)

Address Offset: 1E–1Fh
Default Value: 02A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

SSTS is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e. AGP side) of the "virtual" PCI-to-PCI bridge embedded within 82443BX.

Bit	Descriptions
15	**Detected Parity Error (DPE1).** Note that the PERRE1 bit does not affect the function of this bit. Also the PERR# is not implemented in the 82443BX. 1 = 82443BX detected of a parity error in the address or data phase of AGP bus transactions. 0 = Software sets DPE1 to 0 by writing a 1 to this bit.
14	**Received System Error (SSE1).** 1 = 82443BX asserted SERR# for any enabled error condition under device 1. Device 1 error conditions are enabled in the SSTS and BCTRL registers. 0 = Software clears SSE1 to 0 by writing a 1 to this bit.
13	**Received Master Abort Status (RMAS1).** 1 = 82443BX terminates a Host-to-AGP with an unexpected master abort. 0 = Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS1).** 1 = 82443BX-initiated transaction on AGP is terminated with a target abort. 0 = Software resets RTAS1 to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS1).** STAS1 is hardwired to a 0, since the 82443BX does not generate target abort on AGP.
10:9	**DEVSEL# Timing (DEVT1).** This 2-bit field indicates the timing of the DEVSEL# signal when the 82443BX responds as a target on AGP, and is hard-wired to the value 01b (medium) to indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle. 01 = Medium. (hardwired)
8	**Data Parity Detected (DPD1).** Hardwired to 0. 82443BX does not implement G_PERR# function. However, data parity errors are still detected and reported on SERR# (if enabled by SERRE, SERRE1 and the BCTRL register, bit 0).
7	**Fast Back-to-Back (FB2B1).** This bit is hardwired to 1. The 82443BX as a target supports fast back-to-back transactions on AGP.
6	Reserved.
5	**66/60MHZ Capability.** Hardwired to 1.
4:0	Reserved.

3.4.17 MBASE—Memory Base Address Register (Device 1)

Address Offset: 20–21h
Default Value: FFF0h
Access: Read/Write
Size: 16 bits

This register controls the CPU to AGP non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

This register must be initialized by the configuration software.

Bit	Description
15: 4	**Memory Address Base (MEM_BASE).** Corresponds to A[31:20] of the memory address. Default=FFF0h
3:0	Reserved.

3.4.18 MLIMIT—Memory Limit Address Register (Device 1)

Address Offset: 22–23h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register controls the CPU to AGP non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

This register must be initialized by the configuration software.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable AGP address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved CPU-AGP memory access performance.

Note: The configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e. prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the 82443BX hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Description
15: 4	**Memory Address Limit (MEM_LIMIT).** Corresponds to A[31:20] of the memory address. Default=0
3:0	Reserved.

3.4.19 PMBASE—Prefetchable Memory Base Address Register (Device 1)

Address Offset: 24–25h
Default Value: FFF0h
Access: Read/Write
Size: 16 bits

This register controls the CPU to AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE=< address =<PREFETCHABLE_MEMORY_LIMIT

This register must be initialized by the configuration software.

Bit	Description
15: 4	**Prefetchable Memory Address Base(PMEM_BASE).**Corresponds to A[31:20] of the memory address. Default=FFF0h
3:0	Reserved.

3.4.20 PMLIMIT—Prefetchable Memory Limit Address Register (Device 1)

Address Offset: 26–27h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register controls the CPU to AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE=< address =<PREFETCHABLE_MEMORY_LIMIT

This register must be initialized by the configuration software.

Note: The prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as Uncachable and the ones that can be designated as a USWC (i.e. prefetchable) from the CPU perspective.

Bit	Description
15: 4	**Prefetchable Memory Address Limit (PMEM_LIMIT).** Corresponds to A[31:20] of the memory address. Default=0
3:0	Reserved.

3.4.21 BCTRL—PCI-to-PCI Bridge Control Register (Device 1)

Address Offset: 3Eh
Default: 80h
Access: Read/Write
Size 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., AGP) as well as some bits that affect the overall behavior of the "virtual" PCI-to-PCI bridge in the 82443BX (e.g., VGA compatible address ranges mapping).

Bit	Descriptions
7	**Fast Back to Back Enable.** 82443BX supports fast back-to-back cycles on AGP, and therefore this bit is hardwired to 1.
6	**Secondary Bus Reset:** 82443BX does not support generation of reset via this bit on the AGP and therefore this bit is hardwired to 0. NOTE: The only way to perform a hard reset of the AGP is via the system reset either initiated by software or hardware via PIIX4E.
5	**Master Abort Mode.** Not applicable. Hardwired to 0. (This means when acting as a master on AGP the 82443BX will drop writes on the "floor" and return all 1s during reads.)
4	Reserved.
3	**VGA Enable.** Controls the routing of CPU-initiated transactions targeting VGA compatible I/O and memory address ranges. 1 = 82443BX will forward the following CPU accesses to AGP: • memory accesses in the range 0A0000h to 0BFFFFh • I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded) When this bit is set, forwarding of these accesses issued by the CPU is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers. Forwarding of these accesses is also independent of the settings of bit 2 (ISA Enable) of this register or of bit 5 (VGA Palette Snoop Enable) of the PCICMD1 register if this bit is 1. 0 = VGA compatible memory and I/O range accesses are mapped to PCI unless they are redirected to AGP via I/O and memory range registers defined above (IOBASE, IOLIMIT, MBASE, MLIMIT, PMBASE, PMLIMIT). (default)
2	**ISA Enable.** Modifies the response by the 82443BX to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 1 = When this bit is set to 1 82443BX will not forward to AGP any I/O transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead going to AGP these cycles will be forwarded to PCI where they can be subtractively or positively claimed by the ISA bridge. 0 = All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to AGP. (default)
1	Reserved.
0	**Parity Error Response Enable.** Controls 82443BX's response to data phase parity errors on AGP. G_PERR# is not implemented by the 82443BX. However, when this bit is set to 1, address and data parity errors on AGP are reported via SERR# mechanism, if enabled by SERRE1 and SERRE. If this bit is reset to 0, then address and data parity errors on AGP are not reported via the 82443BX SERR# signal. Other types of error conditions can still be signaled via SERR# independent of this bit's state. 1 = Enable. 0 = Disable.