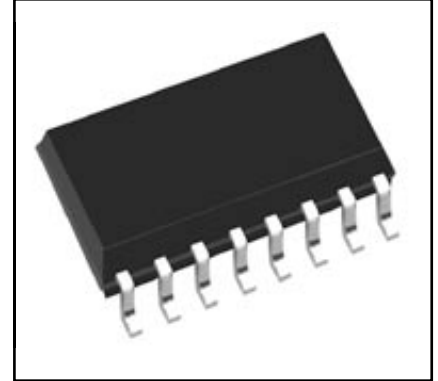
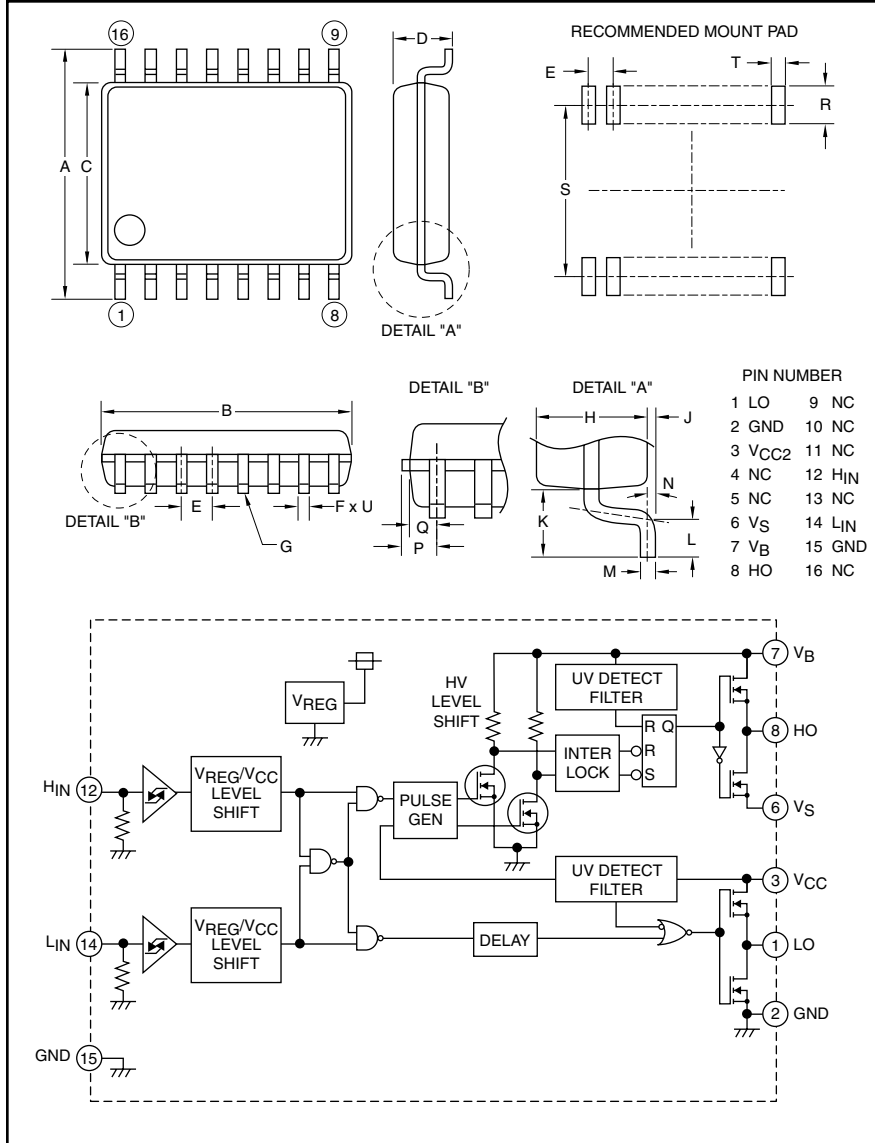


HVIC High Voltage Half-Bridge Driver 600 Volts/±2A



Description:
M81709FP is a high voltage Power MOSFET and IGBT module driver for half-bridge applications.

- Features:**
- Shoot Through Interlock
 - Output Current ±2A
 - Half-Bridge Driver
 - SOP-16 Package

- Applications:**
- HID Ballast
 - PDP
 - MOSFET Driver
 - IGBT Driver
 - Inverter Module Control

Ordering Information:
M81709FP is a ±2A, 600 Volt HVIC, High Voltage Half-Bridge Driver

Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	0.31±0.01	7.8±0.3
B	0.41±0.004	10.1±0.1
C	0.21±0.004	5.3±0.1
D	0.12	2.10
E	0.05	1.27
F	0.02±0.002	0.4±0.05
G	0.004	0.1
H	0.07	1.8
J	0.01±0.004	0.1±0.1
K	0.05	1.25

Dimensions	Inches	Millimeters
L	0.024±0.008	0.6±0.2
M	0.1±0.002	0.2±0.05
N	8°	8°
P	0.03	0.755
Q	0.023	0.605
R	0.05 Min.	1.27 Min.
S	0.30	7.62
T	0.029	0.76
U	0.098 Dia.	0.25 Dia.



Powerex, Inc., 200 E. Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

M81709FP

HVIC, High Voltage Half-Bridge Driver

600 Volts/±2A

Absolute Maximum Ratings, $T_a = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	M81709FP	Units
High Side Floating Supply Absolute Voltage	V_B	-0.5 ~ 624	Volts
High Side Floating Supply Offset Voltage	V_S	$V_B - 24 \sim V_B + 0.5$	Volts
High Side Floating Supply Voltage ($V_{BS} = V_B - V_S$)	V_{BS}	-0.5 ~ 24	Volts
High Side Output Voltage	V_{HO}	$V_S - 0.5 \sim V_B + 0.5$	Volts
Low Side Fixed Supply Voltage	V_{CC}	-0.5 ~ 24	Volts
Low Side Output Voltage	V_{LO}	-0.5 ~ $V_{CC} + 0.5$	Volts
Logic Input Voltage (H_{IN}, L_{IN})	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	Volts
Allowable Offset Voltage Transient	dVs/dt	±50	V/ns
Package Power Dissipation ($T_a = 25^\circ\text{C}$, On Board)	P_d	0.9	Watts
Linear Derating Factor ($T_a > 25^\circ\text{C}$, On Board)	K_θ	9.0	mW/°C
Junction to Case Thermal Resistance	$R_{th(j-c)}$	50	°C/W
Junction Temperature	T_j	-20 ~ 125	°C
Operation Temperature	T_{opr}	-20 ~ 100	°C
Storage Temperature	T_{stg}	-40 ~ 125	°C

Recommended Operating Conditions

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Floating Supply Absolute Voltage	V_B		$V_S + 10$	—	$V_S + 20$	Volts
High Side Floating Supply Offset Voltage	V_S	$V_B > 10V$	-5	—	500	Volts
High Side Floating Supply Voltage	V_{BS}	$V_B = V_B - V_S$	10	—	20	Volts
High Side Output Voltage	V_{HO}		V_S	—	V_B	Volts
Low Side Fixed Supply Voltage	V_{CC}		10	—	20	Volts
Logic Supply Voltage	V_{LO}		0	—	V_{CC}	Volts
Logic Input Voltage	V_{IN}	H_{IN}, L_{IN}	0	—	V_{CC}	Volts

Electrical Characteristics

$T_a = 25^\circ\text{C}$, $V_{CC} = V_{BS} (= V_B - V_S) = 15V$ unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Floating Supply Leakage Current	I_{FS}	$V_B = V_S = 600V$	—	—	1.0	µA
V_{BS} Standby Current	I_{BS}	$H_{IN} = L_{IN} = 0V$	—	0.2	0.5	mA
V_{CC} Standby Current	I_{CC}	$H_{IN} = L_{IN} = 0V$	0.2	0.5	1.0	mA
High Level Output Voltage	V_{OH}	$I_O = 0A, L_O, H_O$	13.8	14.4	—	Volts
Low Level Output Voltage	V_{OL}	$I_O = 0A, L_O, H_O$	—	—	0.1	Volts
High Level Input Threshold Voltage	V_{IH}	H_{IN}, L_{IN}	2.1	3.0	4.0	Volts
Low Level Input Threshold Voltage	V_{IL}	H_{IN}, L_{IN}	0.6	1.5	2.0	Volts
High Level Input Bias Current	I_{IH}	$V_{IN} = 5V$	—	25	75	µA
Low Level Input Bias Current	I_{IL}	$V_{IN} = 0V$	—	—	1.0	µA
V_{BS} Supply UV Reset Voltage	V_{BSuvr}		8.0	8.9	9.8	Volts
V_{BS} Supply UV Hysteresis Voltage	V_{BSuvh}		0.3	0.7	—	Volts
V_{BS} Supply UV Filter Time	$t_{V_{BS}uv}$		—	7.5	—	µs
V_{CC} Supply UV Reset Voltage	V_{CCuvr}		8.0	8.9	9.8	Volts

M81709FP

HVIC, High Voltage Half-Bridge Driver

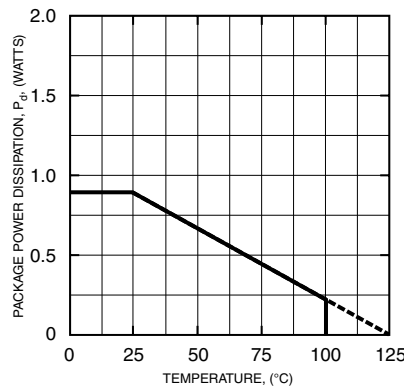
600 Volts/±2A

Electrical Characteristics

T_a = 25°C, V_{CC} = V_{BS} (= V_B - V_S) = 15V unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
V _{CC} Supply UV Hysteresis Voltage	V _{CCuvh}		0.3	0.7	—	Volts
V _{CC} Supply UV Filter Time	t _{VCCuv}		—	7.5	—	µs
Output High Level Short Circuit Pulsed Current	I _{OH}	V _O = 0V, V _{IN} = 5V, P _W < 10µs	—	2.5	—	A
Output Low Level Short Circuit Pulsed Current	I _{OL}	V _O = 15V, V _{IN} = 0V, P _W < 10µs	—	2.5	—	A
Output High Level ON Resistance	R _{OH}	I _O = -200mA, R _{OH} = (V _{OH} - V _O)/I _O	—	10	13	Ω
Output Low Level ON Resistance	R _{OL}	I _O = 200mA, R _{OL} = V _O /I _O	—	2.5	3.0	Ω
High Side Turn-On Propagation Delay	t _{dLH(HO)}	C _L = 1000pF between HO - V _S	100	135	170	ns
High Side Turn-Off Propagation Delay	t _{dHL(HO)}	C _L = 1000pF between HO - V _S	100	135	170	ns
High Side Turn-On Rise Time	t _{rH}	C _L = 1000pF between HO - V _S	—	20	35	ns
High Side Turn-Off Fall Time	t _{fH}	C _L = 1000pF between HO - V _S	—	15	25	ns
LowSide Turn-On Propagation Delay	t _{dLH(LO)}	C _L = 1000pF between LO - GND	100	135	170	ns
Low Side Turn-Off Propagation Delay	t _{dHL(LO)}	C _L = 1000pF between LO - GND	100	135	170	ns
Low Side Turn-On Rise Time	t _{rL}	C _L = 1000pF between LO - GND	—	20	35	ns
Low Side Turn-Off Fall Time	t _{fL}	C _L = 1000pF between LO - GND	—	15	25	ns
Delay Matching, High Side and Low Side Turn-On	Δt _{dLH}	t _{dLH(HO)} - t _{dLH(LO)}	—	—	30	ns
Delay Matching, High Side and Low Side Turn-Off	Δt _{dHL}	t _{dHL(HO)} - t _{dHL(LO)}	—	—	30	ns

THERMAL DERATING FACTOR CHARACTERISTICS



FUNCTION TABLE (X : HORL)

H _{IN}	L _{IN}	V _{BS} U _v	V _{CC} U _v	HO	LO	Behavioral State
L	L	H	H	L	L	LO = HO = Low
L	H	H	H	L	H	LO = High
H	L	H	H	H	L	HO = High
H	H	H	H	L	L	LO = HO = Low
X	L	L	H	L	L	HO = Low, V _{BS} U _v Tripped
X	H	L	H	L	H	LO = High, V _{BS} U _v Tripped
L	X	H	L	L	L	LO = Low, V _{CC} U _v Tripped
H	X	H	L	L	L	HO = LO = Low, V _{CC} U _v Tripped

NOTE: "L" state of V_{BS} U_v, V_{CC} U_v means that U_v trip voltage.
In the case of both input signals (H_{IN} and L_{IN}) are "H", output signals (HO and LO) become "L".

M81709FP

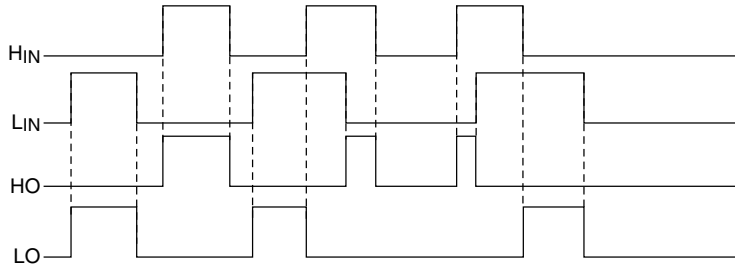
HVIC, High Voltage Half-Bridge Driver

600 Volts/±2A

TIMING DIAGRAM

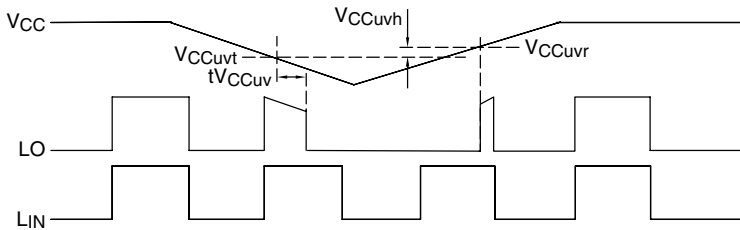
1. Input/Output Timing Diagram

HIGH ACTIVE – When input signal (H_{IN} or L_{IN}) is “H”, then output signal (HO or LO) is “H”. In the case of both input signals (H_{IN} and L_{IN}) are “H”, then output signals (HO and LO) become “L”.

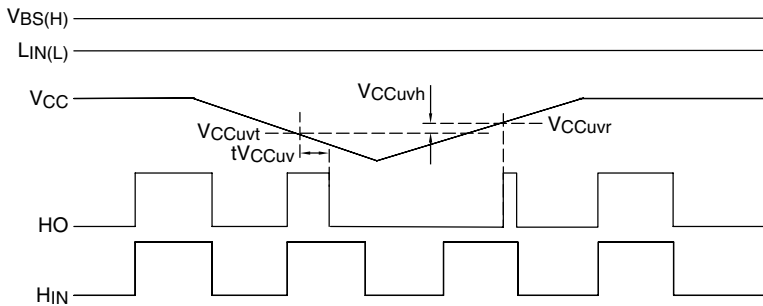


2. VCC(VBS) Supply Under Voltage Lockout Timing Diagram

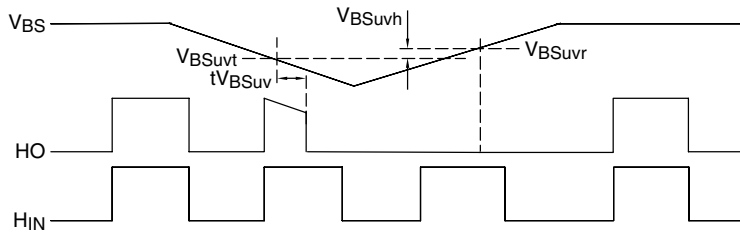
When V_{CC} supply voltage keeps lower UV trip voltage ($V_{CCuvt} = V_{CCuvr} - V_{CCuvh}$) for V_{CC} supply UV filter time, output signal becomes “L”. And then, when V_{CC} supply voltage is higher than UV reset voltage, output signal LO becomes “H”.



When V_{CC} supply voltage keeps lower UV trip voltage ($V_{CCuvt} = V_{CCuvr} - V_{CCuvh}$) for V_{CC} supply UV filter time, output signal becomes “L”. And then, when V_{CC} supply voltage is higher than UV reset voltage, input signal (L_{IN}) is “L”; output signal HO becomes “H”.



When V_{BS} supply voltage keeps lower UV trip voltage ($V_{BSuvt} = V_{BSuvr} - V_{BSuvh}$) for V_{BS} supply UV filter time, output signal becomes “L”. And then, V_{BS} supply voltage is higher than UV reset voltage, output signal HO keeps “L” until next input signal H_{IN} is “H”.



3. Allowable Supply Voltage Transient

It is recommended supplying V_{CC} first and supplying V_{BS} second. In the case of shutting off supply voltage, shut off V_{BS} firstly and shut off V_{CC} second. At the time of starting V_{CC} and V_{BS} , power supply should be increased slowly. If it is increased rapidly, output signal (HO or LO) may be “H”.