High Performance DrMOS – Integrated Power Stage

DESCRIPTION

The SiC778 is an integrated power stage solution optimized for synchronous buck applications offering high current, high efficiency and high power density. Packaged in Vishay's proprietary 6 mm x 6 mm MLP package, SiC778 enables voltage regulator designs to deliver in excess of 40 A per phase current with 91 % peak efficiency.

The internal Power MOSFETs utilize Vishay's state-of-the-art TrenchFET Gen III technology that delivers industry bench-mark performance by significantly reducing switching and conduction losses.

The SiC778 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and a thermal warning (THDN) that alerts the system of excessive junction temperature. The driver is also compatible with a wide range of PWM controllers and supports tri-state PWM, 3.3 V (SiC778ACD) PWM logic, and skip mode (SMOD) to improve light load efficiency.

FEATURES

- Thermally enhanced PowerPAK® MLP6x6-40L package
- Industry benchmark MOSFET with integrated Schottky diode
- Delivers in excess of 40 A continuous current
- 91 % peak efficiency
- High frequency operation up to 1 MHz
- Power MOSFETs optimized for 12 V input stage
- 3.3 V PWM logic with tri-state and hold-off
- SMOD logic for light load efficiency boost
- Low PWM propagation delay (< 20 ns)
- Thermal monitor flag
- Enable feature
- V_{CIN} UVLO
- Compliant with Intel DrMOS 4.0 specification
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck converters
- Multi-phase VRDs for CPU, GPU, and memory
- DC/DC POL modules

TYPICAL APPLICATION DIAGRAM

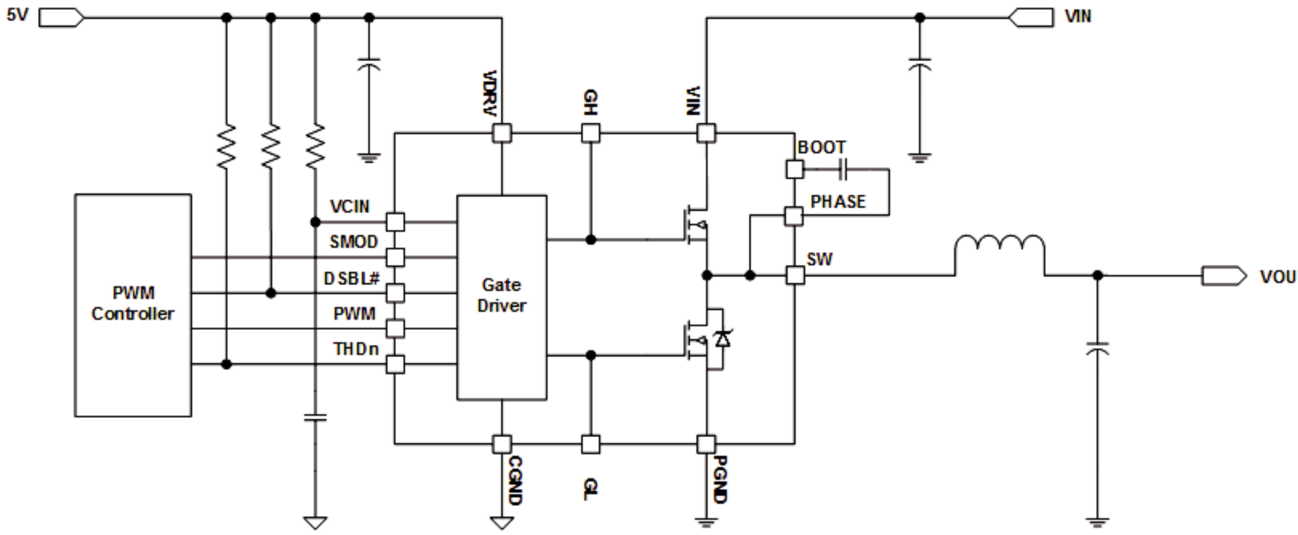


Figure 1: SiC778 Typical Application Diagram

PIN CONFIGURATION

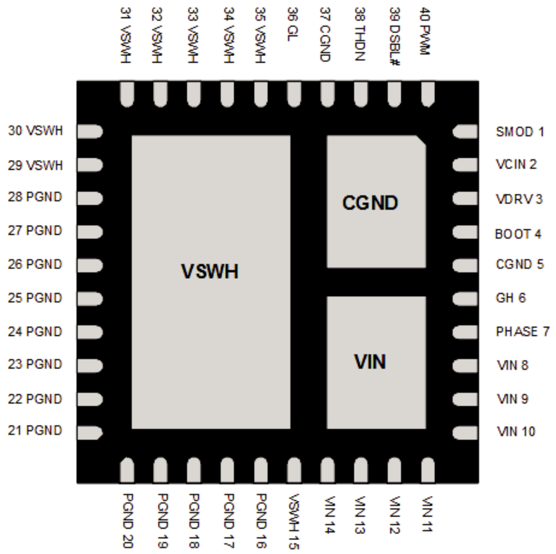


Figure 2 - SiC778 Pin Configuration (Bottom View)

PIN DESCRIPTION

Pin Number	Symbol	Description
1	SMOD#	LS FET turn-off logic. Active low
2	V_{CIN}	Supply voltage for internal logic circuitry
3	V_{DRV}	Supply voltage for internal gate driver
4	BOOT	High side driver bootstrap voltage
5, 37, P1	C_{GND}	Analog ground for the driver IC
6	GH	High side gate signal
7	PHASE	Return path of HS gate driver
8 to 14, P2	V_{IN}	Power stage input voltage. Drain of high side MOSFET
15, 29 to 35, P3	V_{SWH}	Phase node of the power stage
16 to 28	P_{GND}	Power ground
36	GL	Low side gate signal
38	THDN	Thermal shutdown open drain output
39	DSBL#	Disable pin. Active low
40	PWM	PWM input logic

ORDERING INFORMATION

Part Number	Package	Marking Code
SiC778ACD-T1-GE3	PowerPAK MLP66-40L	SiC778A
SiC778DB	Reference board	

ABSOLUTE MAXIMUM RATINGS (1)

Electrical Parameter	Symbol	Limits	Unit
Input Voltage	V_{IN}	- 0.3 to 20	V
Control Input Voltage	V_{CIN}	- 0.3 to 7	
Drive Input Voltage	V_{DRV}	- 0.3 to 7	
Switch Node (DC)	V_{SW}	- 0.3 to 20	
Boot Voltage (DC Voltage)	V_{BS}	- 0.3 to 27	
Boot to Switching Node (DC Voltage)	V_{BS_SW}	- 0.3 to 7	
All Logic Inputs and Outputs (PWM, DSBL, SMOD and THDN)		- 0.3 to V_{CIN} + 0.3	
Max. Operating Junction Temperature	T_J	150	°C
Ambient Temperature	T_A	- 40 to 125	
Storage Temperature		- 65 to 150	

Note:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Input Voltage (V_{IN})	4.5		18	V
Drive Input Voltage (V_{DRV})	4.5	5	5.5	
Control Input Voltage (V_{CIN})	4.5	5	5.5	
Switching Node (LX, DC Voltage)			19	
BOOT-SW	4	4.5	5.5	

THERMAL RESISTANCE RATINGS

Parameter	Min.	Typ.	Max.	Unit
Thermal Resistance from Junction to Case (to P3 PAD V_{SWP} signal)		2.5		°C/W
Thermal Resistance from Junction to PCB		5		

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified $V_{DSBL\#}$ = 5 V, V_{SMOD} = 5 V, V_{IN} = 12 V, V_{DRV} = V_{CIN} = 5 V, T_A = 25 °C	Min.[2]	Typ.[1]	Max.[2]	Unit
Power Supplies						
Control Logic Input Current	I_{VCIN}	$V_{DSBL\#}$ = 0 V, no switching		100		µA
		$V_{DSBL\#}$ = 5 V, no switching		300		
		$V_{DSBL\#}$ = 5 V, f_s = 300 kHz, D = 0.1		300		
Drive Input Current (Dynamic)	I_{VDRV}	f_s = 300 kHz, D = 0.1		16	25	mA
		f_s = 1 MHz, D = 0.1		60		
Drive Input Current (No Switching)		$V_{DSBL\#}$ = 0 V, no switching		30		µA
		$V_{DSBL\#}$ = 5 V, no switching		60		

ELECTRICAL SPECIFICATIONS						
Parameter	**Symbol**	**Test Conditions Unless Specified** $V_{DSBL\#}$ = 5 V, V_{SMOD} = 5 V, V_{IN} = 12 V, V_{DRV} = V_{CIN} = 5 V, T_A = 25 °C	**Min.(2)**	**Typ.(1)**	**Max.(2)**	**Unit**
Bootstrap Supply						
Bootstrap Switch Forward Voltage	V_F	V_{CIN} = 5 V, forward bias current 2 mA			0.4	V
PWM Control Input (SiC778ACD)						
Rising Threshold	$V_{th\_pwm\_r}$		2.1	2.4	2.8	V
Falling Threshold	$V_{th\_pwm\_f}$		0.7	0.9	1.2	
Tri-state Voltage	V_{tri}	PWM pin floating		1.8		
Tri-state Rising Threshold	$V_{th\_tri\_r}$		0.9		1.5	
Tri-state Falling Threshold	$V_{th\_tri\_f}$		1.9	2.2	2.6	
Tri-state Rising Threshold Hysteresis	$V_{hys\_tri\_r}$			225		mV
Tri-state Falling Threshold Hysteresis	$V_{hys\_tri\_f}$			275		
PWM Input Current	I_{PWM}	V_{PWM} = 3.3 V			300	µA
		V_{PWM} = 0 V			- 300	
Timing Specifications						
Tri-State to GH/GL Rising Propagation Delay	$T_{PD\_R\_Tri}$	No load, see fig. 4.		20		ns
Tri-state Hold-Off Time	T_{TSHO}			150		
GH - Turn Off Propagation Delay	$T_{PD\_OFF\_GH}$			20		
GH - Turn ON Propagation Delay (Dead Time Rising)	$T_{PD\_ON\_GH}$			10		
GL - Turn Off Propagation Delay	$T_{PD\_OFF\_GL}$			20		
GL - Turn On Propagation Delay (Dead Time Falling)	$T_{PD\_ON\_GL}$			10		
DSBL# High to GH/GL Rising Propagation Delay	$T_{PD\_R\_DSBL}$			22		
DSBL# Low to GH/GL Falling Propagation Delay	$T_{PD\_F\_DSBL}$			10		
DSBL#, SMOD INPUT						
DSBL# Logic Input Voltage	V_{DSBL}	Enable	2			V
		Disenable			0.8	
SMOD Logic Input Voltage	V_{SMOD}	High State	2			
		Low State			0.8	
Protection						
Under Voltage Lockout	V_{UVLO}	Rising, On Threshold		3.7	4.3	V
		Falling, Off Threshold	2.7	3.2		
Under Voltage Lockout Hysteresis		Note 3		550		mV
THDn Flag Set				160		°C
THDn Flag Clear				135		
THDn Flag Hysteresis				25		
THDn Output Low				0.02		V

Notes:

1.Typical limits are established by characterization and are not production tested.

2.Min. and max. not 100 % production tested.

3.Guaranteed by design.

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L, and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{th\_pwm\_r}$ the low side is turned OFF and the high side is turned ON. When PWM input is driven below $V_{th\_pwm\_f}$ the high side turns off and the low side turns on. For tri-state logic, the PWM input operates as above for driving the MOSFETs. However, there is an third state that is entered into as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC778A to pull the PWM input into the tri-state region (see the tri-state Voltage Threshold diagram below). If the PWM input stays in this region for the tri-state hold-off period, t_{TSHO}, both high side and low side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC778ACD incorporates PWM voltage thresholds that are compatible with 3.3 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFET. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to C_{GND} and shut down the IC.

Diode Emulation Mode (SMOD) Skip

When SMOD pin is low the diode emulation mode is enabled and GL is turned off. This is a non-synchronous conversion mode that improves light load efficiency by reducing switching losses. Conducted losses that occur in synchronous buck regulators when inductor current is negative can also be reduced. Circuitry in the external controller IC detects when inductor current crosses zero and drive SMOD Lo turning the low side MOSFET off. See SMOD operation diagram for additional details. This function can be also be used for a pre-biased output voltage. If SMOD is left unconnected, an internal pull up resistor will pull the pin up to V_{CIN} (logic high) to disable the SMOD function.

Thermal Shutdown Warning (THDN)

The THDN pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 kΩ to pull this pin up to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THDN flag is set. When the junction temperature drops below 135 °C the device will clear the THDN signal. The SiC778 does not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The Switch node V_{SWH} is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating the C_{GND} and P_{GND} should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin. shoot-through protection and adaptive dead time

Shoot-Through Protection and Adaptive Dead Time (AST)

The SiC778A has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on until the other's gate voltage is sufficiently low (1 V), that and built in delays ensure the one power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC778A also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

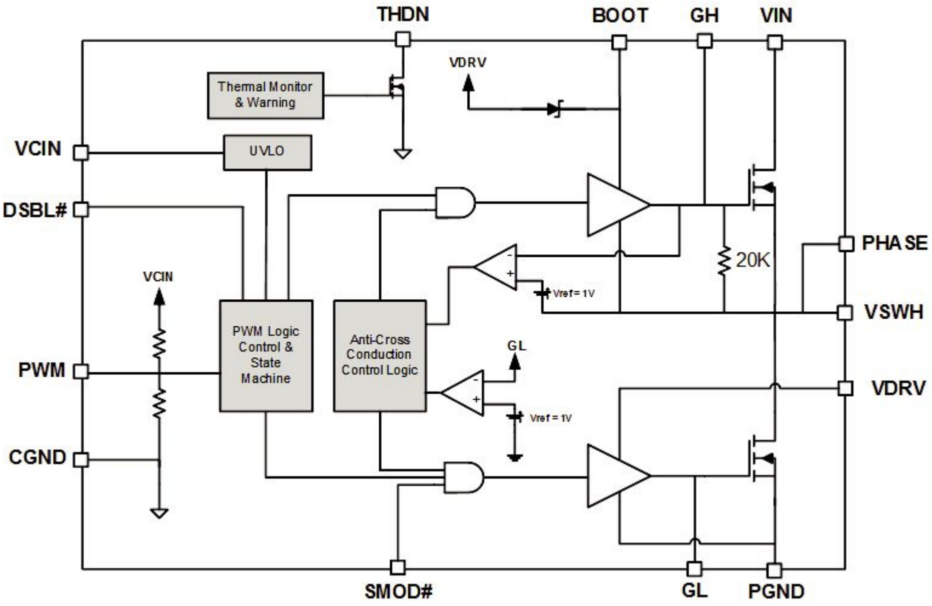


Figure 3: SiC778 Functional Block Diagram

DEVICE TRUTH TABLE

DSBL#	SMOD	PWM	GH	GL
Open	X	X	L	L
L	X	X	L	L
H	L	L	L	L
H	L	H	H	L
H	H	H	H	L
H	H	L	L	H
H	L	Tri-state	L	L
H	H	Tri-state	L	L

DEFINITION OF PWM LOGIC AND TRI-STATE

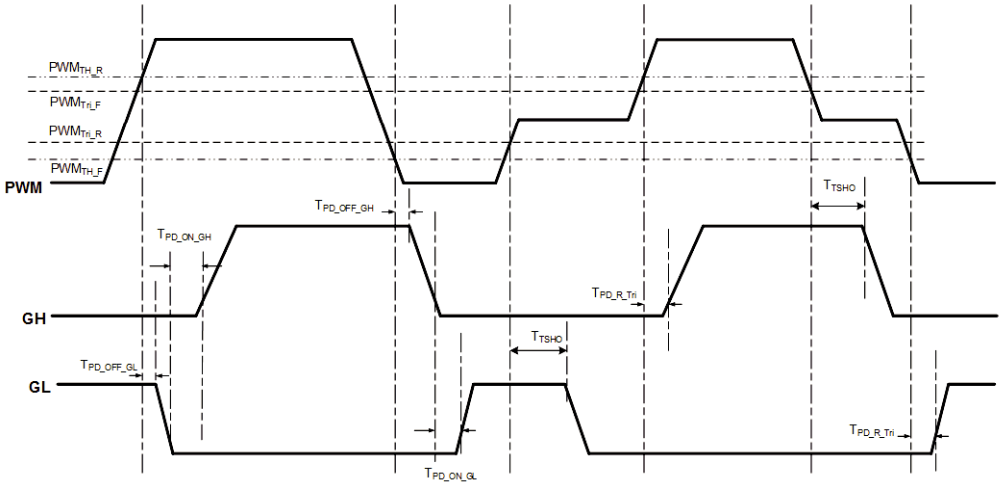


Figure 4: Definition of PWM Logic and Tri-state

SMOD OPERATION DIAGRAM

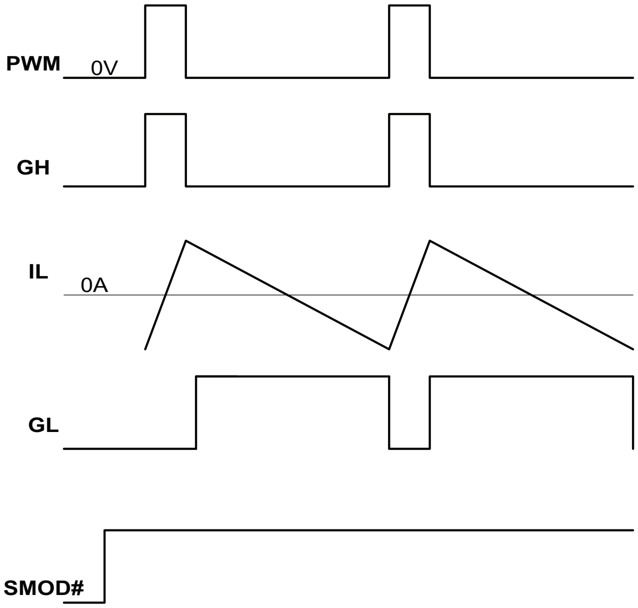


Figure 5: CCM Operation with SMOD# = High

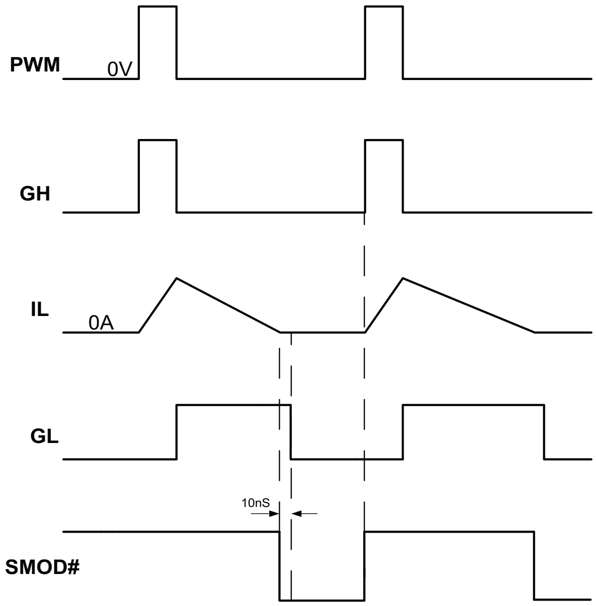
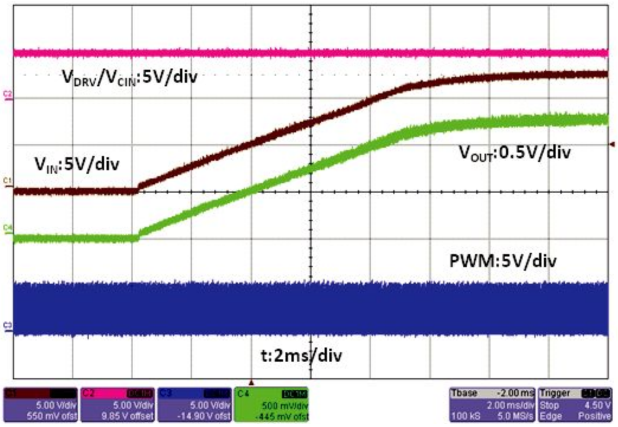
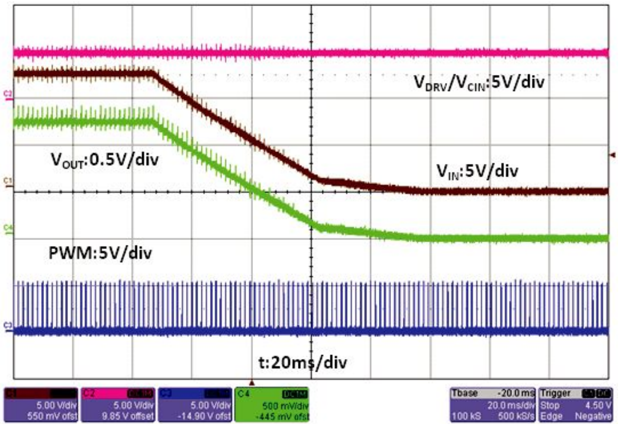


Figure 6: DCM Operation with SMOD# = Active Toggle

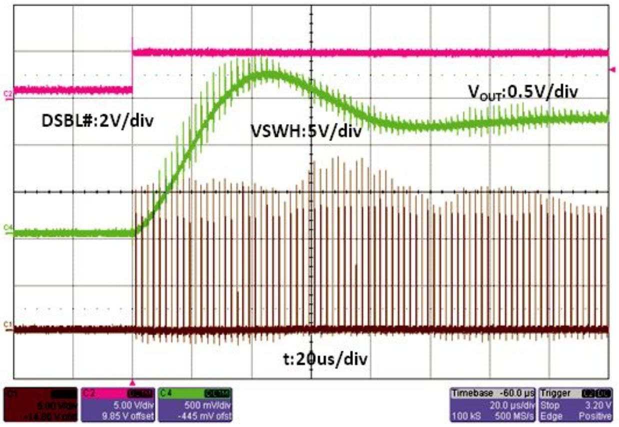
ELECTRICAL CHARACTERISTICS



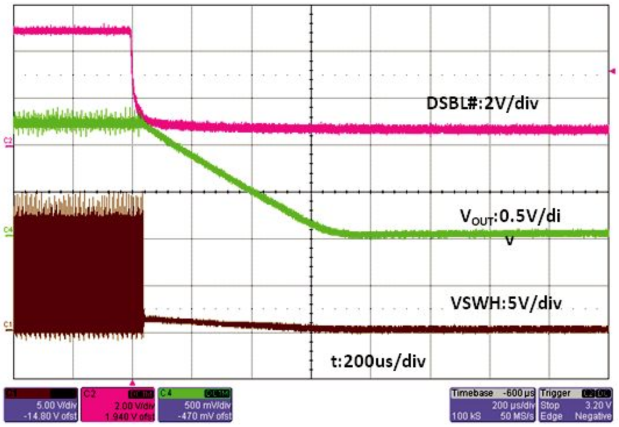
Start-up with V_{IN} Ramping up
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz



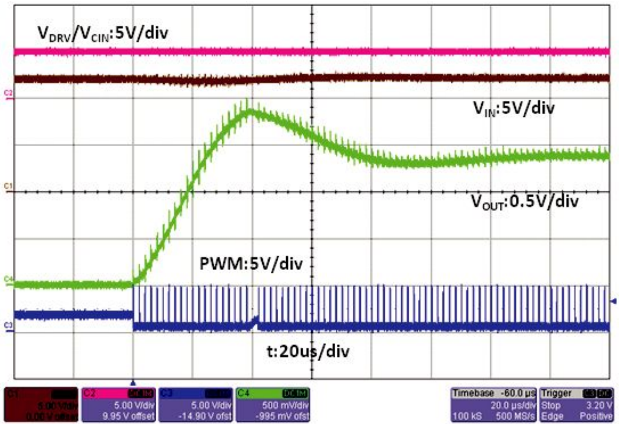
Power Off with V_{IN} Ramping down
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz



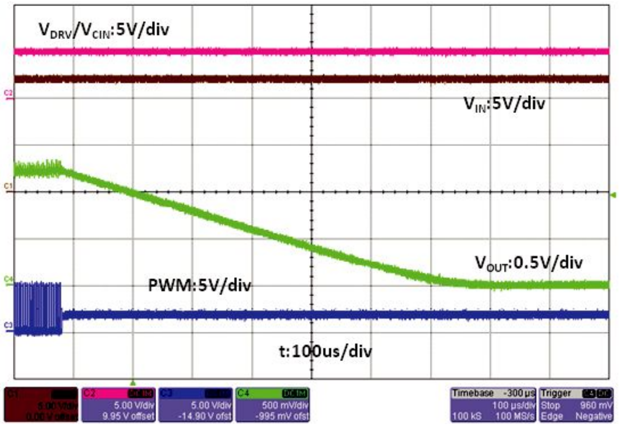
Start-up with DSBL# Toggle High
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz



Shut-down with DSBL# Toggle Low
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz

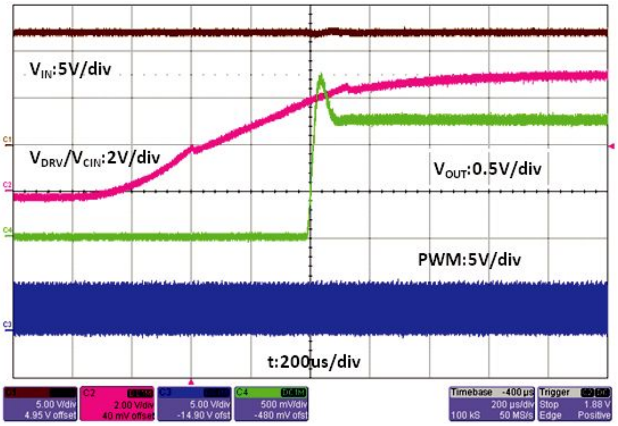


Start-up with PWM existing Tri-state
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz

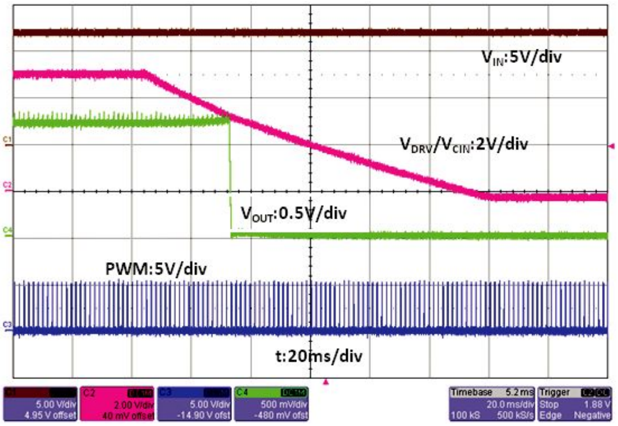


Shut-down with PWM entreing Tri-state
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz

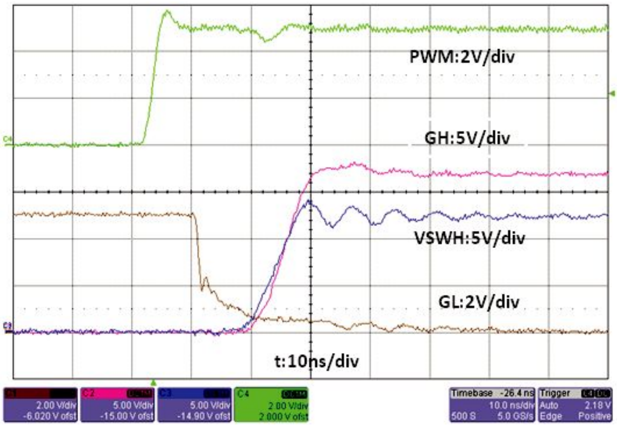
ELECTRICAL CHARACTERISTICS



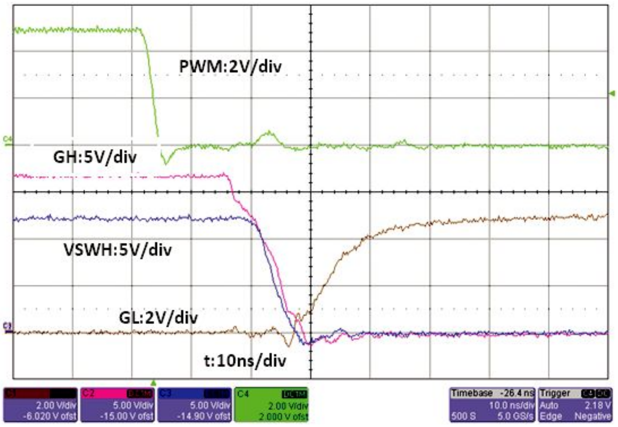
Start-up with V_{DRV}/V_{CIN} Ramping Up
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz



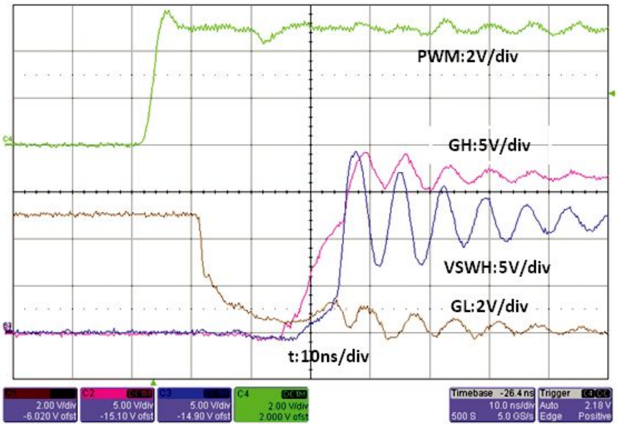
Power Off with V_{DRV}/V_{CIN} Ramping Down
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, I_{OUT} = 1.2 A



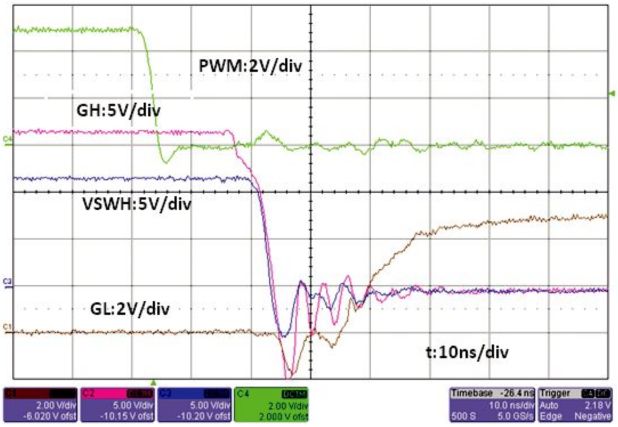
Switching waveform at PWM Rising Edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, I_{OUT} = 0 A



Switching Waveform at PWM Falling Edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz

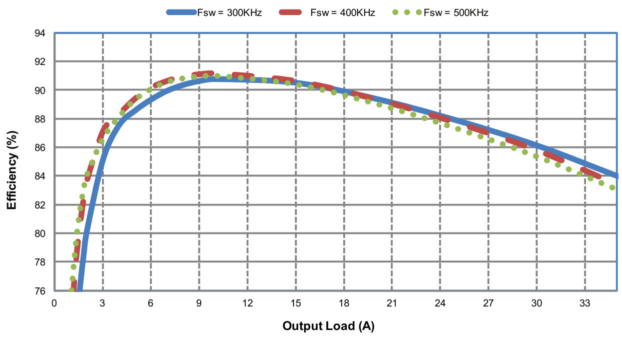


Switching Waveform at PWM Rising Edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, I_{OUT} = 30 A

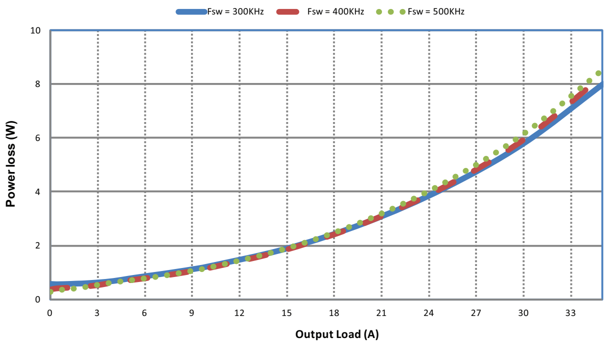


Switching Waveform at PWM Falling Edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, I_{OUT} = 30 A

ELECTRICAL CHARACTERISTICS

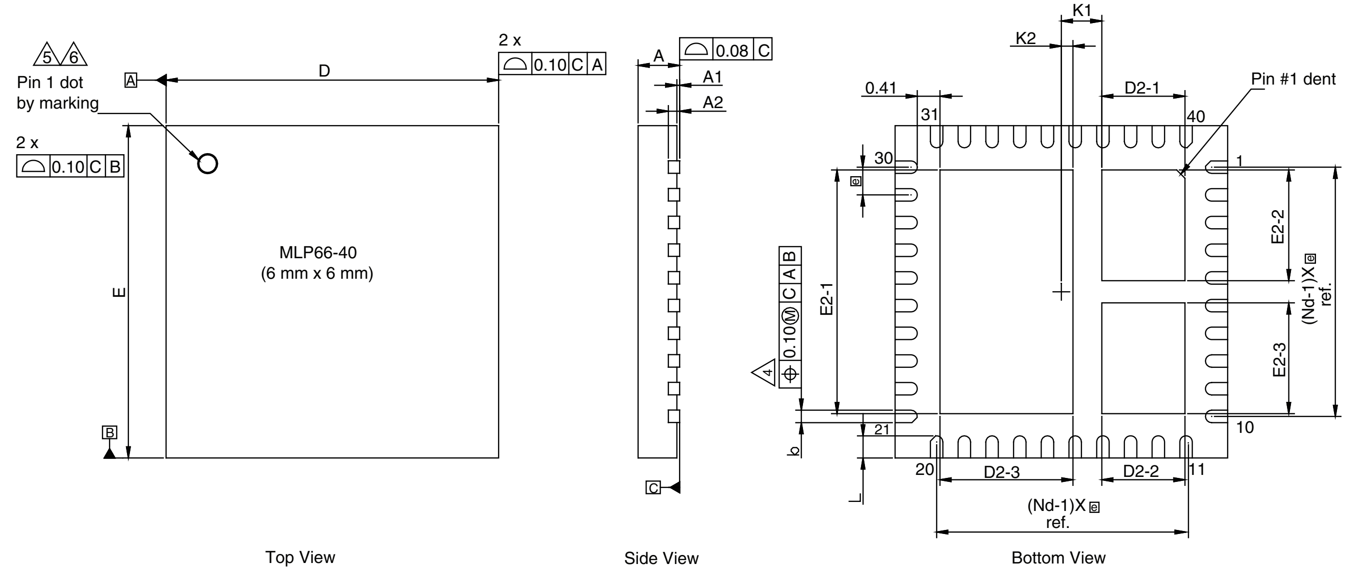


Typical Efficiency
V_{IN} = 12 V, V_{OUT} = 1.2 V, V_{DRV} = V_{CIN}; No Air Flow, O/P Inductance = 0.33 µH



Typical Power Loss
V_{IN} = 12 V, V_{OUT} = 1.2 V, V_{DRV} = V_{CIN}; No Air Flow, O/P Inductance = 0.33 µH

PACKAGE DIMENSIONS



DIM	MILLIMETERS			INCHES		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A(8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0	-	0.05	0	-	0.002
A2	0.20 ref.			0.008 ref.		
b(4)	0.20	0.25	0.30	0.078	0.098	0.011
D	6.00 BSC			0.236 BSC		
e	0.50 BSC			0.019 BSC		
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)	40			40		
Nd (3)	10			10		
Ne (3)	10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC			0.008 BSC		

Notes:

1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5M-1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction .

△4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.

△5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body .

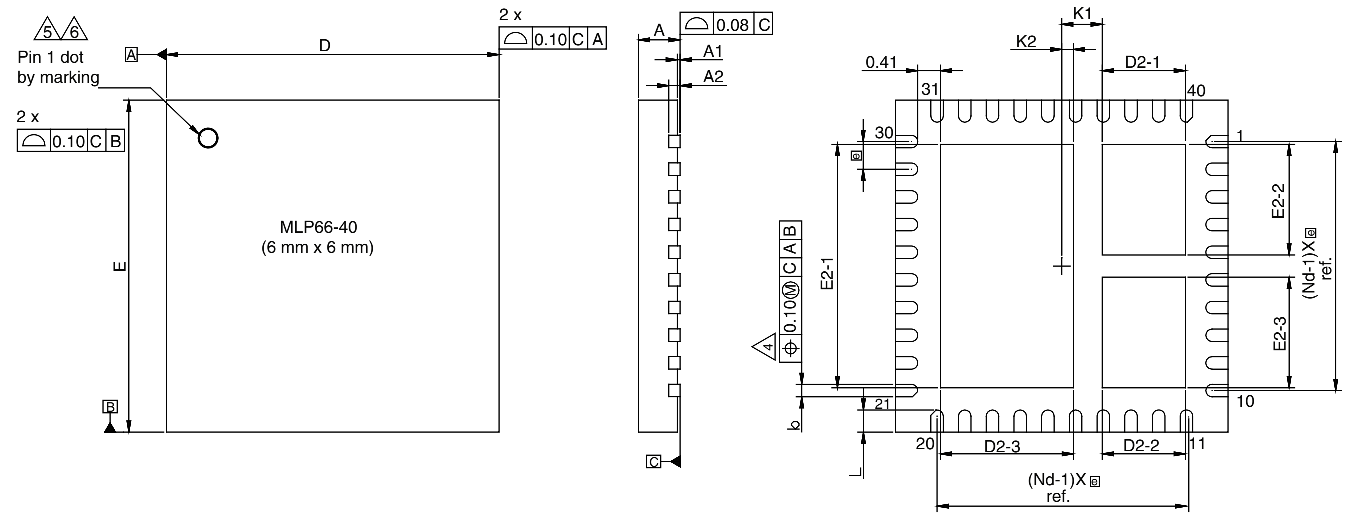
△6. Exact shape and size of this feature is optional.

7. Package warpage max. 0.08 mm.

△8. Applied only for terminals.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63808.

PowerPAK® MLP66-40 Case Outline



Top View Side View Bottom View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b [4]	0.20	0.25	0.30	0.078	0.098	0.011
D	6.00 BSC			0.236 BSC		
e	0.50 BSC			0.019 BSC		
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N [3]	40			40		
Nd [3]	10			10		
Ne [3]	10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC			0.008 BSC		

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Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

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