Structure : Silicon Monolithic Integrated Circuit
Product Name : Power Driver For Compact Disc Players

Device Name : **BA5929FP**

Features :
- 3-ch BTL driver
- Use of an HSOP-25 PIN power package can achieve downsizing of the set.
- A wide dynamic range (Vcc12=5V, Vcc3=12V, 4.2V (typ.) when RL=8Ω)
- A built-in thermal shutdown circuit is installed.
- A built-in general operational amplifier installed.
- Through the standby terminal, the power saving mode can be set.

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	Vcc12, Vcc3	13.5	V
Power Dissipation	Pd	1.45 *1	W
Operating Temperature Range	Topr	-35 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

*1 When mounted on the glass/epoxy board with the size: 70 mm×70 mm, the thickness: 1.6 mm, and the rate of copper foil occupancy area: 3% or less.
Over Ta=25°C, derating at the rate of 11.6mW/°C

○ OPERATING CONDITIONS

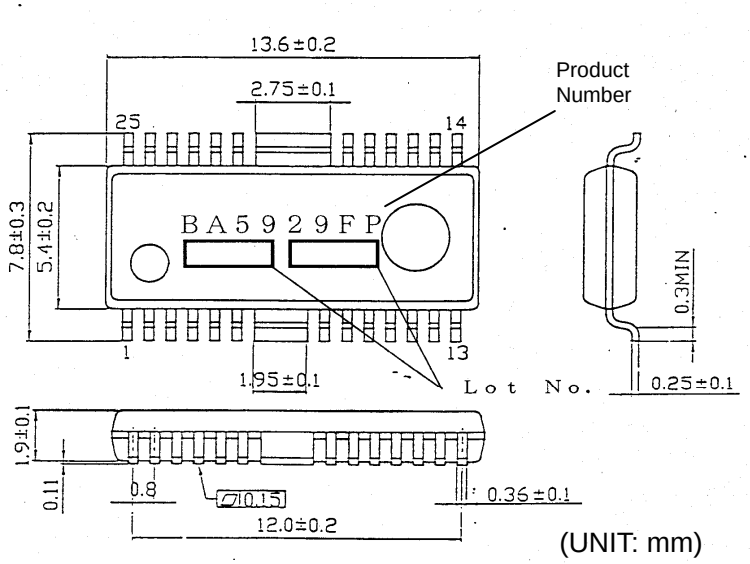
Parameter	Symbol	Limits	Unit
Power Supply Voltage	Vcc12, Vcc3	4.5 to 13.2	V

This product has not been checked for the strategic materials (or service) defined in the Foreign Exchange and Foreign Trade Control Low of Japan so that a verification work is required before exporting it.
Not designed for radiation resistance.

○ ELECTRIC CHARACTERISTICS (Ta=25°C, Vcc12=5V, Vcc3=12V, BIAS=1.65V, R_L=8Ω, unless otherwise noted.)

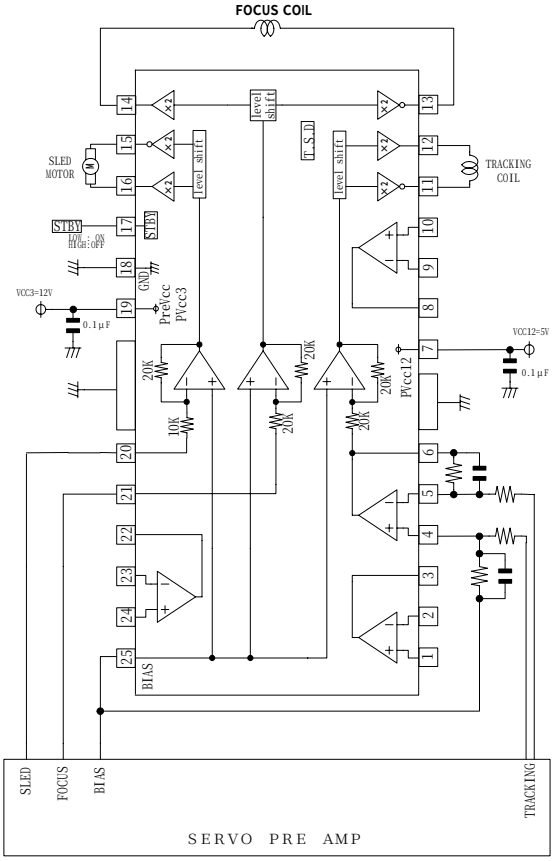
Parameter	Symbol	MIN.	TYP	MAX.	Unit	Condition
Standby Consumption Current	IST	-	-	100	μA	
Consumption Current (at no signal)	IQ	-	18	28	mA	No load applied
Output Offset Voltage	Voof	-70	-	70	mV	
Maximum Output Amplitude (CH1, 2)	VOM12	3.8	4.2	-	V	
Maximum Output Amplitude (CH3)	VOM3	8.5	9.5	-	V	
Closed Circuit Voltage Gain (CH1, 2)	GVC12	10.0	11.5	13.0	dB	VIN=0.1Vrms f=1KHz
Closed Circuit Voltage Gain (CH3)	GVC3	16.0	17.5	19.0	dB	VIN=0.1Vrms f=1KHz
Standby Voltage	VSTBY	-	-	0.5	V	
Standby Reset Voltage	VSTOFF	2.0	-	-	V	
<OP-AMP>						
Offset Voltage	VOFOP	-6	0	6	mV	
Input Bias Current	VBOP	-	-	300	nA	
High-level Output Voltage	VOHOP	10.0	11.3	-	V	
Low-level Output Voltage	VOLOP	-	0.1	0.4	V	
Output Driving Current Sink	ISI	1.0	5.0	-	mA	VCC with 50Ω attached
Output Driving Current Source	ISO	8.0	12.0	-	mA	GND with 50Ω attached
Slew Rate	SROP	-	1	-	V/μs	100KHz square wave, 2Vp-p output

○ OUTLINE DIMENSIONS, SYMBOLS



(UNIT: mm)

○ APPLICATION CIRCUIT DIAGRAM



Resistance unit : [Ω]

○ PIN NUMBERS, PIN NAMES

No.	Pin Name	Description	No.	Pin Name	Description
1	OPIN2P	Operational amplifier 2 Non-inverted input	14	OUT2P	Driver CH2 Positive output
2	OPIN2M	Operational amplifier 2 Inverted input	15	OUT3M	Driver CH3 Negative output
3	OPOUT2	Operational amplifier 2 Output	16	OUT3P	Driver CH3 Positive output
4	OPIN1P	Operational amplifier 1 Non-inverted input	17	STBY	Standby control terminal
5	OPIN1M	Operational amplifier 1 Inverted input	18	GND	GND
6	OPOUT1	Operational amplifier 1 Output	19	PVCC3	VCC (CH3/pre-stage)
7	PVCC12	VCC (CH1/CH2)	20	CH3IN	CH3 Input
8	OPOUT3	Operational amplifier 2 Output	21	CH2IN	CH2 Input
9	OPIN3M	Operational amplifier 2 Inverted input	22	OPOUT4	Operational amplifier 4 Output
10	OPIN3P	Operational amplifier 2 Non-inverted input	23	OPIN4M	Operational amplifier 4 Inverted input
11	OUT1M	Driver CH1 negative output	24	OPIN4P	Operational amplifier 4 Non-inverted input
12	OUT1P	Driver CH1 positive output	25	BIAS	Bias input
13	OUT2M	Driver CH2 negative output			

Note) The positive or negative polarity of driver outputs is determined by the input polarity.
CH1: When the inverted AMP is used for the input stage OP-AMP, the H input results in L at the negative output pin and H at the positive output pin.
CH2/CH3: Applying the signal H to the input pin results in L at the negative output pin and H at the positive output pin.

○ CAUTIONS ON USE

(1) Setting the standby terminal (pin 17) voltage to open or to 0.5V (typ.) or less, the driver will turn OFF and the power saving mode can be set.
Under conditions of normal use, the pin 17 should be pulled-up to 2.0V or above.
(2) On the Bias terminal (pin 25), the applied voltage of 0.7V (typ.) or less will activate a mute function.
Under conditions of normal use, it should be set to 1.3V or above.
(3) Thermal shutdown (TSD) or bias terminal voltage drop will activate the mute function, where only the driver part can be muted. While muting, the voltage at the output terminal will equal to the internal reference voltage (approximately Vcc/2).
(4) Connecting a capacitive load to the OP-AMP output results in a phase margin reduction of the amp and may cause an oscillation or a peak. When connecting a capacitive load, a resistance must be inserted in series between the output and the capacitive load. And after careful consideration of the frequency characteristics, the device should be used within the range where no problem is found in actual use.
(5) The radiating fin must be connected to the external GND.
(6) Short-circuit between output pin -VCC, output pin-GND, or output terminals (load short) must be avoided.
Mounting the ICs in improper directions may damage themselves or produce smoke.
(7) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.
(8) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.
(9) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.
(10) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.
(11) About operations in a strong electric field
When used in a strong electric field, note that a malfunction may occur.
(12) ASO
When using this IC, the output Tr. must be set not to exceed the values specified in the absolute maximum ratings and ASO.
(13) Thermal shutdown circuit
This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open.
The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.
Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

(14) About earth wiring patterns
When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current.
Make sure that the GND wiring patterns of the external components will not change, too.

(15) This IC is a monolithic IC which has a P^+ isolations and P substrate to isolate elements each other.
This P layer and an N layer in each element form a PN junction to construct various parasitic elements.
Due to the IC structure, the parasitic elements are inevitably created by the potential relationship.
Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage. Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level (GND, P substrate) to the input terminals.
In addition, do not apply the voltage to input terminals without applying the power supply voltage to the IC. Also while applying the power supply voltage, the voltage of each input terminal must not be over the power supply voltage, or within the guaranteed values in the electric characteristics.

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