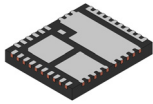


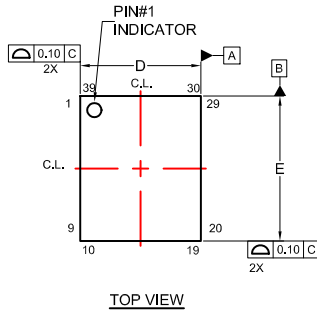
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

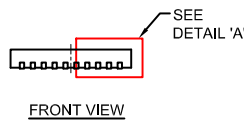


PQFN39 5X6, 0.45P CASE 483BF ISSUE B

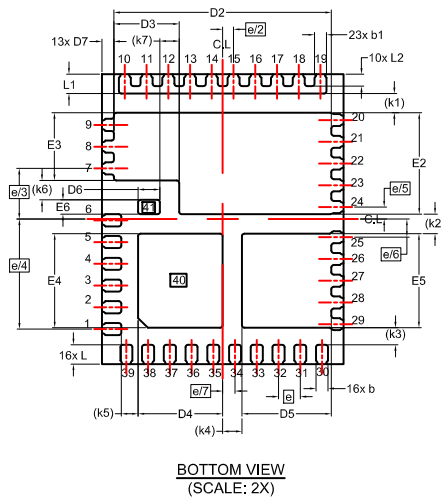
DATE 13 AUG 2019



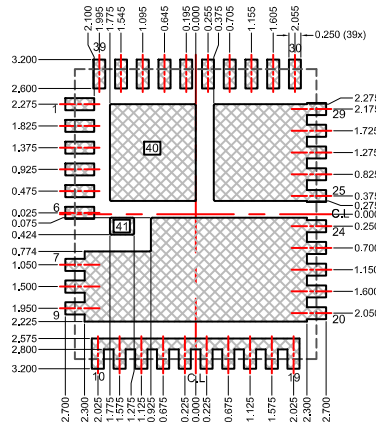
TOP VIEW



FRONT VIEW

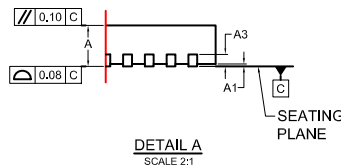


BOTTOM VIEW
(SCALE: 2X)



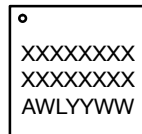
LAND PATTERN
RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR
Pb-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.



DETAIL A
SCALE 2:1

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATED MAY/2005.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
b1	0.20	0.25	0.30
D	4.90	5.00	5.100
D2	4.40	4.50	4.60
D3	1.25	1.35	1.45
D4	1.65	1.75	1.85
D5	1.75	1.85	1.95
D6	0.35	0.45	0.55
D7	0.15	0.25	0.35
E	5.90	6.00	6.10
E2	2.00	2.10	2.20
E3	1.30	1.40	1.50
E4	1.85	1.95	2.05
E5	1.85	1.95	2.05
E6	0.20	0.30	0.40
e	0.450 BSC		
e/2	0.225 BSC		
e/3	1.050 BSC		
e/4	2.275 BSC		
e/5	0.250 BSC		
e/6	0.375 BSC		
e/7	0.255 BSC		
L	0.30	0.40	0.50
L1	0.30	0.40	0.50
L2	0.15	0.25	0.35
k1	0.40 REF		
k2	0.40 REF		
k3	0.35 REF		
k4	0.40 REF		
k5	0.35 REF		
k6	0.40 REF		
k7	0.40 REF		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

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