

# VT1697SB

# Smart Slave IC with Integrated Current and Temperature Sensors

## General Description

The VT1697SB is a feature-rich smart slave IC designed to work with Maxim’s seventh-generation masters to implement a high-density multiphase voltage regulator. Up to six smart slave ICs plus a master IC provide a compact synchronous buck converter that includes accurate individual phase current and temperature reporting through SMBus. This smart-slave device includes protection circuits for overtemperature, VX short, all power supplies UVLO faults, and main power supply OVLO fault. If a fault is detected, the slave IC immediately shuts down and sends a fault signal to the master IC.

Monolithic integration and advanced packaging technologies allow practical per-phase high switching frequencies with significantly lower losses than alternative implementations. This smart slave device is designed to support phase shedding and DCM modes for efficiency optimization over a wide range of load currents. High per-phase current capability designs with low  $C_{OUT}$  enable a design with fewer phases and a smaller footprint.

The VT1697SB is an FCQFN package with exposed top-side thermal pads. Top-side cooling allows improved heat transfer to ambient and reduces PC board and component temperatures.

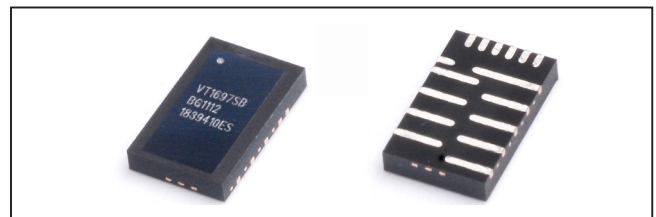
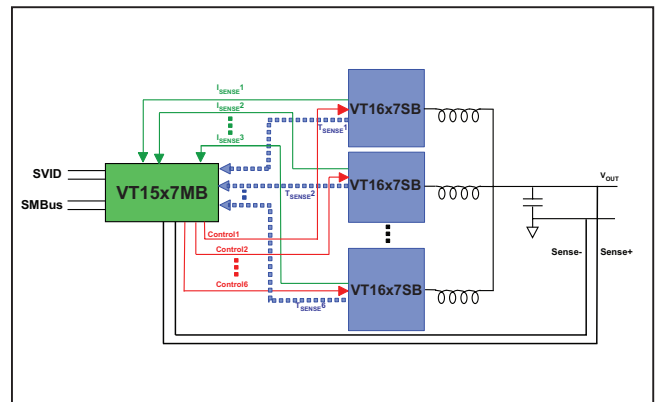
## Applications

- High-Current Voltage Regulators
  - Microprocessor: 32-Bit and 64-Bit I/A RISC Architectures
  - Memory
  - Graphic Processors
  - Networking ASICs

## Benefits and Features

- High Per-Phase Current Capability
- Footprint < 1600mm<sup>2</sup> for a 150A VR
- Precise Temperature Monitoring and Reporting through a Master Controller IC SMBus
- Accurate Per-Phase Current Reporting Using a Master Controller IC
- Top-side Cooling Allows Improved Heat Transfer to Ambient
- Supplies UVLO/OVLO, Bootstrap Voltage UVLO, VX Short Protection
- Overcurrent Protection
- Overtemperature Protection—Fast Shutdown
- Switching Frequency 300KHz—1.3MHz
- Compatible With Coupled Inductor

## Basic Application Circuit



*Ordering Information* appears at end of data sheet.

**Absolute Maximum Ratings**

V <sub>DDH</sub> to V <sub>SS</sub> .....	-0.3V to +23V	V <sub>DD</sub> , V <sub>CC</sub> to GND .....	-0.3V to +2.5V
VX to V <sub>SS</sub> (DC) .....	-0.3V to +23V	PWM, ISENSE, TS_FAULT to GND.....	-0.3V to V <sub>DD</sub> + 0.3V
VX to V <sub>SS</sub> (AC) (Notes 1, 2) .....	-10V to +23V	V <sub>SS</sub> to GND.....	-0.3V to +0.3V
V <sub>DDH</sub> to VX (DC).....	-0.3V to +23V	Peak VX Current (Note 3) .....	±100A
V <sub>DDH</sub> to VX (AC) (Notes 1, 2).....	-10V to +23V	Junction Temperature (T <sub>J</sub> ).....	+150°C
BST to V <sub>SS</sub> (DC) .....	-0.3V to +25.5V	Storage Temperature Range .....	-65°C to +150°C
BST to V <sub>SS</sub> (AC) (Note 2) .....	-7V to +25.5V	Peak Reflow Temperature Lead-Free .....	+260°C
BST to VX Differential .....	-0.3V to +2.5V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Operating Ratings**

V <sub>DD</sub> , V <sub>CC</sub> .....	1.71V to 1.98V	Junction Temperature (T <sub>J</sub> ).....	-40°C to +125°C
12V Supply (V <sub>DDH</sub> ) .....	8.5V to 14.0V	Frequency (f <sub>SW</sub> ) .....	300kHz to 1.3MHz

- Note 1:** Input HF capacitors placed not more than 40 mils away from the V<sub>DDH</sub> pin required to keep inductive-voltage spikes within Absolute Maximum limits.
- Note 2:** AC is limited to 25ns.
- Note 3:** Peak OCP clamp levels limit the application below the peak VX current rating.

**Package Information**

**16 FCQFN**

Package Code	P163A6F+2
Outline Number	<a href="#">21-0986</a>
Land Pattern Number	<a href="#">90-0490</a>
<b>THERMAL RESISTANCE</b>	
Junction to Case (θ <sub>JC</sub> ) VT1697SB	0.42°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

## Electrical Characteristics

( $V_{DD} = V_{CC} = 1.71V - 1.98V$ ,  $V_{DDH} = 12V$ . Specifications are for  $T_J = +25^\circ C$  unless otherwise noted. )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY VOLTAGES, SUPPLY CURRENT</b>						
Bias Supply Voltage	$V_{DD}, V_{CC}$		1.71		1.98	V
Power-Train Input Voltage	$V_{DDH}$		8.5	12.0	14.0	V
1.8V Bias Supply Current	$I_{CC} + I_{DD}$	Shutdown (Note 4)		0.5	2	$\mu A$
		Inactive, no switching (Note 5)		3.2	5.0	mA
		Load = 0A, $V_{OUT} = 1.8V$ , $f_{SW} = 1.5MHz$		43	61	mA
		Load = 0A, $V_{OUT} = 1.8V$ , $f_{SW} = 300kHz$		14	20	
12V Bias Supply Current	$I_{DDH}$	Shutdown (Note 4)		1.3	10	$\mu A$
		Inactive, no switching (Note 5)		6.5	20	
<b>I<sub>RECON</sub> SPECIFICATION</b>						
Current Gain ( $I_L$ to ISENSE)	$A_I$	$-70A < I_L < 70A$	95000	100000	105000	A/A
<b>TEMPERATURE-SENSOR SPECIFICATIONS</b>						
Temperature-Sensor Dynamic Range	$T_{RANGE}$		0		150	$^\circ C$
Temperature-Sensor Gain	$A_{TEMP}$			3.01		mV/ $^\circ C$
Temperature-Sensor Voltage	-	$T_J = 0^\circ C$		832		mV
<b>PROTECTION FEATURES</b>						
$V_{DD}$ UVLO Threshold (Rising)	$V_{DD\_UVLO}$		1.47	1.57	1.64	V
$V_{DD}$ UVLO Threshold (Falling)			1.41	1.5	1.58	
$V_{DDH}$ OVLO Threshold (Rising)	$V_{DDH\_OVLO}$		15.48	16	16.41	V
$V_{DDH}$ OVLO Threshold (Falling)			14.95	15.50	15.81	
$V_{DDH}$ UVLO Threshold (Rising)	$V_{DDH\_UVLO}$		4.05	4.27	4.40	V
$V_{DDH}$ UVLO Threshold (Falling)			3.90	4.09	4.25	
$V_{BST}$ UVLO Threshold (Rising)	$V_{BST\_UVLO}$	Note 6	1.39	1.52	1.66	V
$V_{BST}$ UVLO Threshold (Falling)		Note 6	1.32	1.45	1.57	

**Electrical Characteristics (continued)**(V<sub>DD</sub> = V<sub>CC</sub> = 1.71V - 1.98V, V<sub>DDH</sub> = 12V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak Positive-OCP Clamp Level	OCP	VT1697SB	59	67	80	A
Peak Positive-OCP Clamp Delay					63	ns
Peak Negative-OCP Clamp Level		VT1697SB	-79.1	-71.9	-64.7	A
Peak Negative-OCP Delay					110	ns
Overtemperature Shutdown	OTP	Rising threshold	140	150	165	°C
<b>PWM INPUT</b>						
Input Voltage, High State	V <sub>IH</sub>		V <sub>DD</sub> - 0.20			V
Input Voltage, Low State	V <sub>IL</sub>		0.20			V
Three-State Control Threshold (PWM Input Rising)	-		0.63			V
<b>TS_FAULT INPUT</b>						
TS_FAULT Digital Threshold V <sub>IH</sub>	V <sub>IH</sub>		0.41			V
TS_FAULT Digital Threshold V <sub>IL</sub>	V <sub>IL</sub>		0.17			V

**Note 4:** T<sub>SENSE</sub>: PWM and ISENSE pins of the slave are pulled low by the master. The slave is in this state before master OE is enabled.

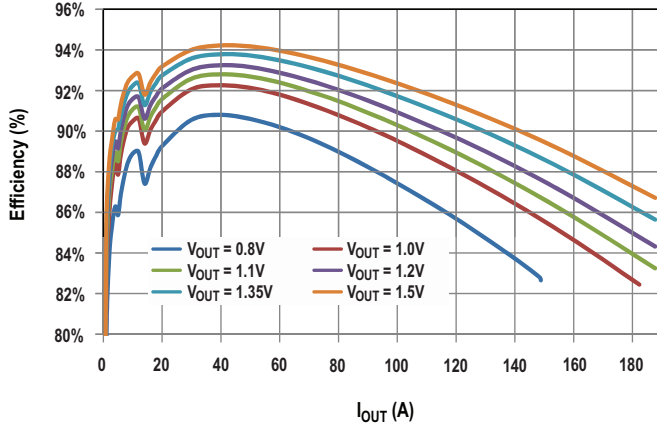
**Note 5:** Inactive, no switching: PWM signal is three stated by the master. The slave is in this mode when the master sheds a phase (temporarily disabling this slave) to save power at lighter loads.

**Note 6:** V<sub>BST\_UVLO</sub> is measured with respect to VX and not from ground.

**VT1697SB Typical Operating Characteristics**

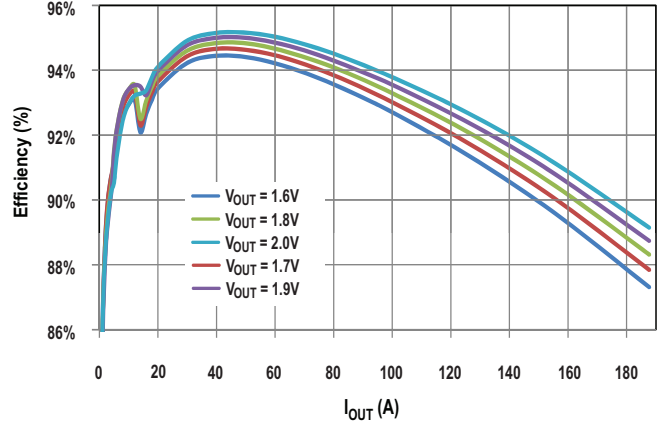
(Master:  $T_A = 25^\circ\text{C}$ ;  $f_{\text{SW}} = 600\text{kHz}$ .)

**Efficiency vs. Load Current  
4 VT1697SB (VR12.0)**



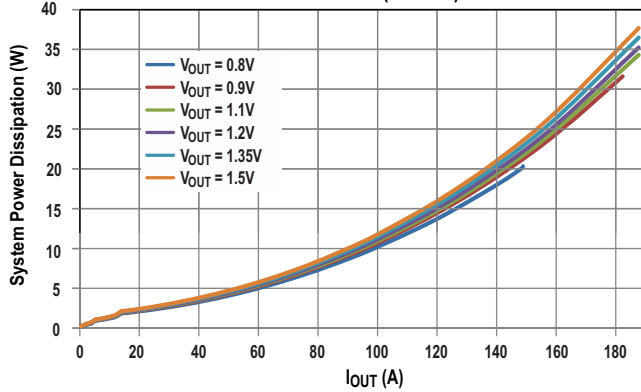
Conditions:  $V_{\text{IN}} = 12\text{V}$   
 $V_{\text{BIAS}} = 1.8\text{V}$   
 Inductor: CLB1108-4-50TR-R

**Efficiency vs. Load Current  
4 VT1697SB (VR12.5)**



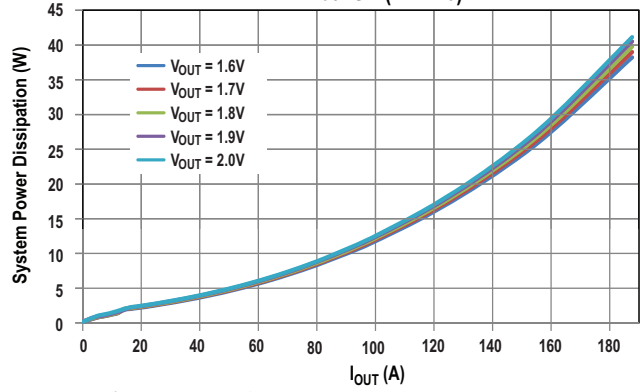
Conditions:  $V_{\text{IN}} = 12\text{V}$   
 $V_{\text{BIAS}} = 1.8\text{V}$   
 Inductor: CLB1108-4-50TR-R

**System Power Dissipation vs. Load Current  
4 VT1697SB (VR12.0)**



Conditions:  $V_{\text{IN}} = 12\text{V}$   
 $V_{\text{BIAS}} = 1.8\text{V}$   
 Inductor: CLB1108-4-50TR-R

**System Power Dissipation vs. Load Current  
4 VT1697SB (VR12.5)**

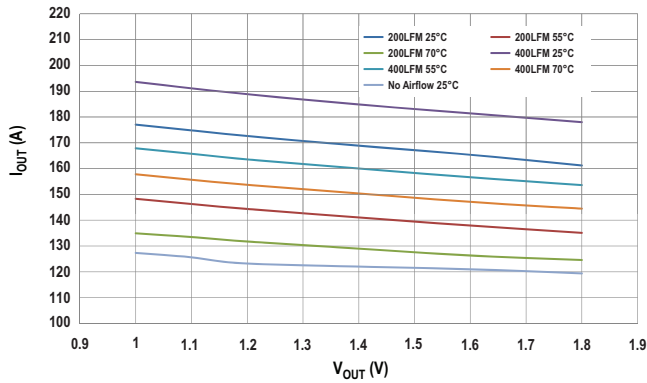


Conditions:  $V_{\text{IN}} = 12\text{V}$   
 $V_{\text{BIAS}} = 1.8\text{V}$   
 Inductor: CLB1108-4-50TR-R

**VT1697SB Typical Operating Characteristics (continued)**

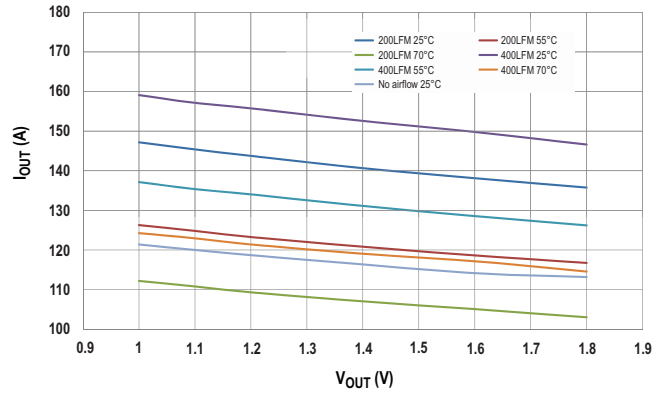
(Master:  $T_A = 25^\circ\text{C}$ ;  $f_{\text{SW}} = 600\text{kHz}$ .)

**VT1697SB 4-Phase Safe Operating Area (Heatsink)**



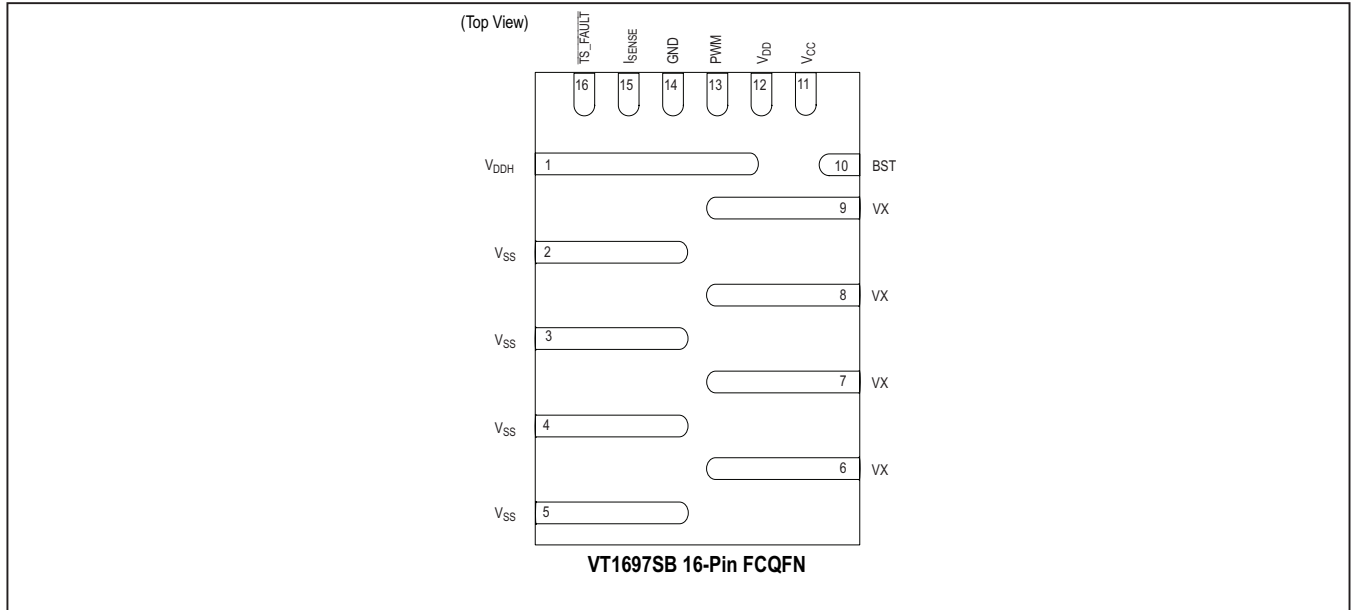
Conditions:  $V_{\text{IN}} = 12\text{V}$   
 $V_{\text{BIAS}} = 1.8\text{V}$   
 Inductor: CL1108-4-50TR-R

**VT1697SB 4-Phase Safe Operating Area (No Heatsink)**



Conditions:  $V_{\text{IN}} = 12\text{V}$   
 $V_{\text{BIAS}} = 1.8\text{V}$   
 Inductor: CL1108-4-50TR-R

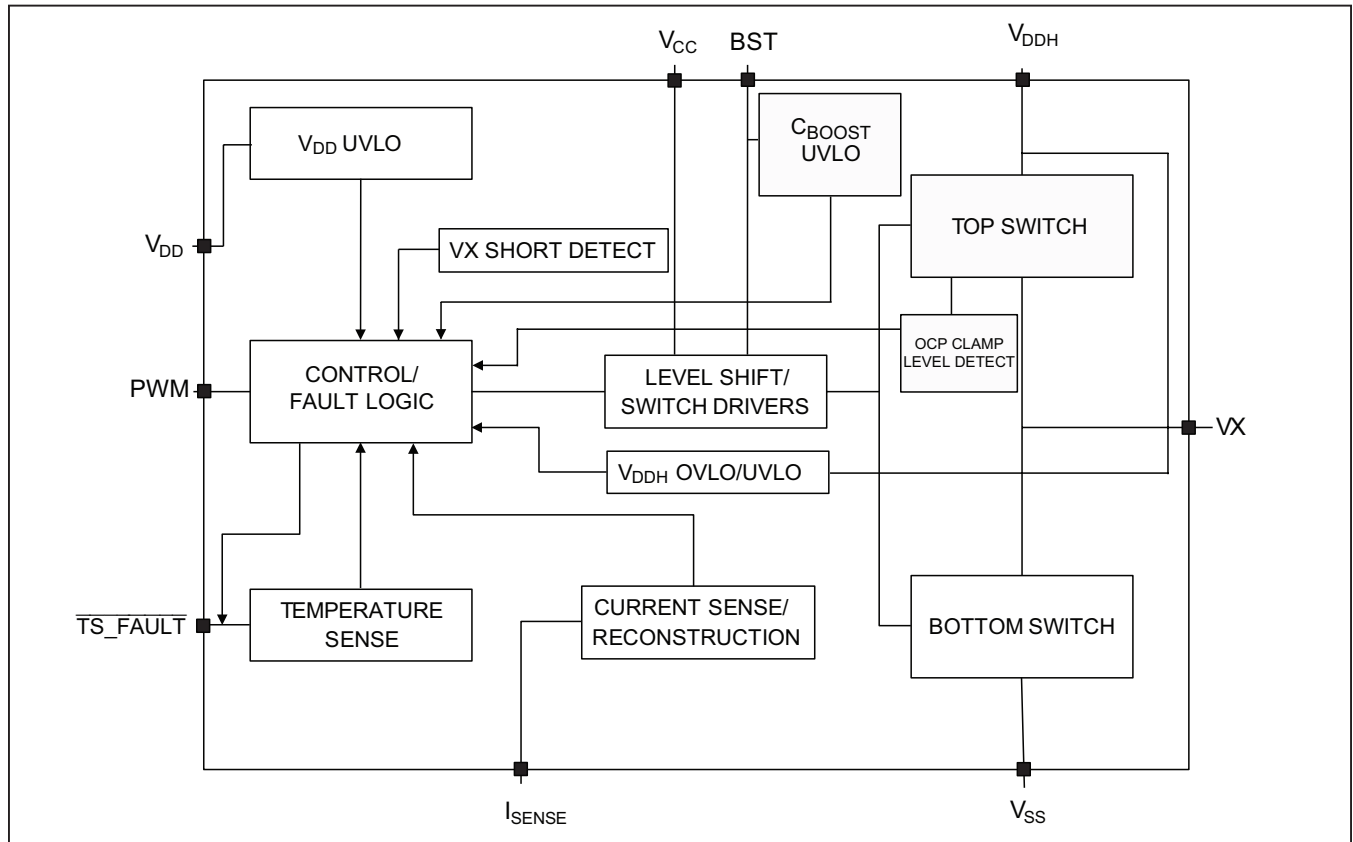
Pin Configuration (continued)



Pin Description (VT1697SB Smart Slave Device)

PIN	NAME	FUNCTION
1	V <sub>DDH</sub>	Drain of High-Side Power FET. Connect to the 12V input supply. See Table 2 for decoupling requirements.
2–5	V <sub>SS</sub>	Power Ground. Connect to the return path of the output load.
6–9	V <sub>X</sub>	Switching Node. Connect to the switching node of the output inductor.
10	BST	Boost Supply Input. Connect a 0.22µF ceramic capacitor placed 40 mils or closer to the IC between BST and V <sub>X</sub> .
11	V <sub>CC</sub>	Gate-Drive Supply. Connect to the 1.8V bias supply. See Table 2 for decoupling requirements.
12	V <sub>DD</sub>	Control Circuit Supply. Connect to the 1.8V bias supply. See Table 2 for decoupling requirements.
13	PWM	PWM Input. Connect to the appropriate PWM_ output of the controller. PWM Logic Levels: <ul style="list-style-type: none"> <li>• High: HS FET on, LS FET off</li> <li>• Mid: Diode emulation mode; both FETs are off when the current reaches zero</li> <li>• Low: LS FET on, HS FET off</li> </ul>
14	GND	Analog Ground. Connect to the ground plane using a single via placed 40 mils or closer to the IC.
15	I <sub>SENSE</sub>	Current-Sense Output. Connect to the appropriate ISENSE input pin of the controller through a simple passive filter. The ISENSE current is an attenuated replica of the V <sub>X</sub> current.
16	TS_FAULT	Smart Power-Stage Temperature and Fault Output. This dual-function pin is used to report the junction temperature and to communicate a fault condition to the controller. Connect TS_FAULT to the TSENSE input of the controller.

Block Diagram



Voltage Regulation

This Maxim smart slave IC provides control logic, drivers, monitoring circuits, and power semiconductors for a synchronous buck converter with fault protection, status monitoring and accurate lossless current sensing. Phases are controlled by the master IC independently by separate phase-control signals.

Power Switch Control and Drivers

The smart slave IC operates in conjunction with a Maxim master IC. The master controller configures the voltage regulator based on its configuration resistors and the number of phases populated. The smart slave device’s switching is controlled by the proprietary command signals on the phase-control lines. The phase-control signal has three defined states: high, low, and “three state.” Three state is used for phase shedding and DCM modes. An external boost capacitor is required to supply the voltage for the high-side switch driver.  $V_{DD}$  and  $V_{CC}$  are brought out separately to allow separate decoupling to improve noise immunity on the  $V_{DD}$  rail.

Current-Sense Output

The integrated lossless current sense (or “current reconstruction”) produces a precise ratiometric current-sense signal for both positive and negative currents which is sent to the master as an analog current signal. This current-sense technology provides accurate current information over load and temperature that is not affected by tolerances of passive elements such as the output inductor, resistors and capacitors.

Phase Configuration

The ability for the master to dynamically disable and reenable a phase is an integral part of the Maxim master/slave architecture. The master sets the phase-control signal to three state to disable a phase. The same state is used to control DCM operation. When using a coupled inductor, a proprietary mode (coupled-inductor mode) can be set by the master and communicated to the smart slave through the phase-control signal to minimize losses due to coupled currents in inactive phases.



## Protection Circuits

### Overcurrent Protection

The smart slave IC incorporates instantaneous overcurrent fault protection using the lossless current-sense/reconstruction. This overcurrent protection is separate from the system overcurrent protection, and is intended to operate only in extreme fault conditions to protect the IC and other components. The system overcurrent protection set by the master should be set with sufficient margin below the slave IC's threshold to ensure correct system operation.

For current sourcing operation, if the instantaneous current in the top switch (based on the current-sense/reconstruction circuit) exceeds the overcurrent-protection value shown in the *Electrical Characteristics* table, the slave regulates the period of the top-side switch to keep its peak current at a safe level. The protection threshold has been set to ensure that the IC's maximum allowable peak current is not exceeded when using the recommended inductors. The sourcing current limiting is not considered a hard fault condition for slave, and therefore  $\overline{\text{TS\_FAULT}}$  is not asserted. Since clamping is based on instantaneous reconstructed current, the ripple current must be considered when calculating the maximum average current per slave. The maximum average current before clamping can be calculated as shown in Equation 1. Note that the clamping is based on reconstructed current. Limits shown in the *Electrical Characteristics* table for Clamp Level reflect expected variations in application conditions and external component characteristics. Also note that the master (i.e., system) overcurrent protection should be set lower than the slave's maximum operating current as stated above.

#### Equation 1:

$$\text{Maximum Average DC Slave Current} = \text{OCP} - \frac{I_{\text{RIPPLE}}}{2}$$

where:

OCP = Peak OCP clamp level (A)

$I_{\text{RIPPLE}}$  = Peak-to-peak inductor ripple current (A)

For current-sinking protection, if the negative overcurrent-protection threshold is reached, the slave limits the current and  $\overline{\text{TS\_FAULT}}$  is not asserted.

The VT1697SB implements an additional OCP shutdown level (beyond the clamp levels). If the current in the top switch exceeds the OCP shutdown level (shown in the *Electrical Characteristics* table), the IC is turned off and fault is reported by asserting the  $\overline{\text{TS\_FAULT}}$  pin. The slave is then latched off until the power is cycled.

### $V_{\text{DD}}$ and $V_{\text{BOOST}}$ Undervoltage Lockout

The smart slave IC includes undervoltage-lockout circuits:  $V_{\text{DD}}$  and  $V_{\text{BOOST}}$ . For power-sequencing guidelines and operation with separate bias rails for master and slaves, refer to appropriate master data sheet.  $V_{\text{BOOST}}$  UVLO is active at all times after the initial system startup. It is not active during the initial system power-on state (before regulation is enabled) and is activated approximately 20 $\mu\text{s}$  after initial startup. If either of these UVLO circuits is tripped during operation, the smart slave stops switching and a fault signal ( $\overline{\text{TS\_FAULT}}$  pulled low) is sent to the master.

### $V_{\text{DDH}}$ ( $V_{\text{IN}}$ ) Undervoltage and Overvoltage Lockout

The slave includes protection circuits that shut down the slave and assert  $\overline{\text{TS\_FAULT}}$  if  $V_{\text{DDH}}$  is above or below the correct operating range. If either of these circuits is tripped during operation, the slave stops switching and a fault signal ( $\overline{\text{TS\_FAULT}}$  pulled low) is sent to the master.

### Temperature Sensing and Overtemperature Protection

The smart slave IC incorporates an accurate die temperature sensor. The temperature-sense signal is sent to the master as an analog signal through the temperature-sense pin. The actual temperature of the smart slave device is then made available through the SMBus of the master. The smart slave IC also includes overtemperature protection. If the trip point is reached, the IC immediately shuts down and the fault is reported to the master through the  $\overline{\text{TS\_FAULT}}$  pin.

### VX Short Protection

The smart slave IC includes a VX short detection to detect a local short circuit from the VX node to either  $V_{\text{DDH}}$  or ground. If such a fault is detected, the slave shuts down and communicates a fault to the master through the  $\overline{\text{TS\_FAULT}}$  pin.

### $\overline{\text{TS\_FAULT}}$ Signal

If a fault is detected, the smart slave sends a signal to the master by pulling the  $\overline{\text{TS\_FAULT}}$  pin to ground. Under normal conditions, this pin is used to send an accurate analog representation of the slave temperature. If a fault is detected, this pin is asserted low to indicate that a fault condition was detected by the slave IC. [Table 1](#) shows the faults that result in this signal being asserted. For a latching fault, the fault must be cleared and the  $V_{\text{DD}}$  power cycled to reenable the IC (for on-latching faults, see the note below the [Table 1](#)).

**Table 1. Fault Detection and Protection Circuits**

FAULT	DESCRIPTION	TYPE	FAULT FLAG ( $\overline{TS\_FAULT}$ )
Boost UVLO	Undervoltage Lockout on Boost Supply	Shutdown*	Asserted
V <sub>DDH</sub> UVLO	Undervoltage Lockout on V <sub>DDH</sub>	Shutdown*	Asserted
V <sub>DDH</sub> OVLO	Overvoltage Lockout Signal on V <sub>DDH</sub>	Shutdown*	Asserted
V <sub>DD</sub> UVLO	Undervoltage Lockout Signal on V <sub>DD</sub>	Shutdown*	Asserted
V <sub>X</sub> Short	V <sub>X</sub> Short-to-Ground or V <sub>DDH</sub>	Shutdown	Asserted
POCP (Sourcing)	Positive/Sourcing Overcurrent Protection	Cycle-by-Cycle Current Limit	Not Asserted
NOCP (Sinking)	Negative/Sinking Overcurrent Protection	Cycle-by-Cycle Current Limit	Not Asserted
OTP	Overtemperature Protection	Shutdown	Asserted

\*V<sub>DDH</sub> UVLO, V<sub>DDH</sub> OVLO, Boost UVLO and V<sub>DD</sub> UVLO are nonlatching faults. If a nonlatching fault is detected by the slave, it asserts  $\overline{TS\_FAULT}$  signal low and stops switching. The slave resumes switching and deasserts  $\overline{TS\_FAULT}$  around 37 $\mu$ s from when the fault condition is removed. Refer to the master data sheet for master response to  $\overline{TS\_FAULT}$  asserted low by the slave device.

## Design Considerations

### Phase Current Sharing and Steering Control

Maxim master/slave chipsets offer options for thermal balancing in applications where one or more phases have different thermal characteristics. The current sense and chipset regulation system offer the potential for current steering, where a percentage of current can be steered away from any phase, allowing that phase to operate at a different current than the other phases. This allows a precise scaling of current in any slave(s) to achieve proper thermal balance between phases. Refer to the applicable Maxim master IC data sheet for more information on how to program this feature.

### Thermal Path and PCB Design

The smart slave IC has an exposed pad on the top-side of the package that is designed as an additional thermal path. This pad is electrically connected to AGND/V<sub>SS</sub>, but is not intended for use as an electrical connection. Since there is normally sufficient airflow above the regulator, conducting heat from the top of the package results

in a low junction-to-ambient thermal impedance, and hence lower junction temperature. This method provides an additional thermal path to the heat flow from the die to the PCB to ambient, and also reduces the temperature of the PCB. Thermal performance is presented for various thermal conditions and airflow rates in the SOA plots.

### PCB Layout

PCB layout can significantly affect the performance of the regulator. Careful attention should be paid to the location of the input capacitors and the output inductor, which should be placed close to the IC. The V<sub>X</sub> traces include large voltage swings (greater than 12V) with dv/dt greater than 10V/ns. It is recommended that these traces are not only kept short, but also are shielded with a ground plane immediately beneath.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative. Also contact Maxim to obtain QFN layout guidelines for optimal design.

**Table 2. Typical Boost, Filtering, and Decoupling Capacitor Requirements**

DESCRIPTION	VALUE	TYPE	PACKAGE	QTY
V <sub>DD</sub> Capacitor	0.1μF/6.3V	X7R/125°C	0603	1
V <sub>CC</sub> Capacitor (Note 1)	1μF/6.3V	X7R/125°C	0603	1
Boost Capacitor	0.22μF/6.3V	X7R/125°C	0402	1
V <sub>DD</sub> RFILTER	10Ω	1/16W 1%	0402	1
V <sub>DDH</sub> HF Capacitor (Note 2)	1μF/16V	X7R/125°C	0603	2
V <sub>DDH</sub> HF Capacitor (Note 2)	0.1μF/16V	X7R/125°C	0402	2
V <sub>DDH</sub> Bulk Capacitor (Note 3)	10μF/16V	X5R	0805/1206	2

**Note 1:** V<sub>CC</sub> should be directly connected to bias supply.

**Note 2:** All V<sub>DDH</sub> high-frequency capacitors must be placed in close proximity to the slave IC and on the same side of the PCB as the slave IC. Refer to Maxim's layout guideline for component placement requirements and recommendations.

**Note 3:** For operation below 10.8V, two 22μF bulk capacitor are recommended instead of two 10μF capacitors.

## Ordering Information

PART	DESCRIPTION	PACKAGE	SHIPPING METHOD	PACKAGE MARKING
VT1697SBFQX*	55A Smart-Slave Device	16 FCQFN	2.5ku Tape & Reel	VT1697SBF

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES
0	1/14	Initial Release	—
1	4/14	Updated Operating Current Rating	1
2	5/14	Updated <i>Electrical Characteristics</i> table and <i>Overcurrent Protection</i> section	3
3	10/16	Updated <i>Absolute Maximum Ratings</i> section	2
4	3/17	Updated <i>Package Information</i> , <i>Absolute Maximum Ratings</i> sections, and <i>Electrical Characteristics</i> and <i>Pin Description</i> tables	2–3, 7

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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