Includes FLEX 8000A

FLEX 8000

Programmable Logic Device Family

March 1995, ver. 6 — Data Sheet

Features...

- Low-cost, high-density, register-rich CMOS programmable logic device family
  - 2,500 to 16,000 usable gates
  - 282 to 1,500 registers (see Table 1)
- FLEX 8000 devices fabricated on a 0.8-micron SRAM process
- Higher-speed FLEX 8000A devices fabricated on a 0.6-micron SRAM process
- Supports in-circuit reconfiguration
- FastTrack continuous routing structure for fast, predictable interconnect delays
- Dedicated carry chain that can implement fast adders and counters
- Dedicated cascade chain for efficient implementation of high-speed, high-fan-in logic functions
- Full compliance with the Peripheral Component Interconnect (PCI) standard for FLEX 8000A devices
- Low power consumption (less than 1 mA in standby mode)
- 3.3-V or 5.0-V operation
  - Full 3.3-V EPF8282V
  - 3.3-V or 5.0-V I/O for EPF8636A and larger devices

Table 1. FLEX 8000 Device Features

Feature	EPF8282 EPF8282V EPF8282A EPF8282AV	EPF8452 EPF8452A	EPF8636A	EPF8820 EPF8820A	EPF81188 EPF81188A	EPF81500 EPF81500A
Available gates	5,000	8,000	12,000	16,000	24,000	32,000
Usable gates	2,500	4,000	6,000	8,000	12,000	16,000
Flipflops	282	452	636	820	1,188	1,500
Logic Elements	208	336	504	672	1,008	1,296
Max. user I/O pins	78	120	136	152	184	208
JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes
Packages *Note (1)*	84-pin PLCC 100-pin TQFP	84-pin PLCC 160-pin PQFP 160-pin PGA 100-pin TQFP	84-pin PLCC 160-pin PQFP 192-pin PGA 208-pin RQFP	160-pin PQFP 192-pin PGA 208-pin RQFP 225-pin BGA	208-pin PQFP 232-pin PGA 240-pin RQFP	240-pin RQFP 280-pin PGA 304-pin RQFP

Note:
(1) Contact Altera for information on package availability.

...and More Features

- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry
- Programmable output slew-rate control to reduce switching noise
- Available in a variety of packages with 84 to 304 pins (see Table 1)
- Software design support provided by the Altera MAX+PLUS II development system for 486- and Pentium-based PCs and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations

General Description

Altera's Flexible Logic Element MatriX (FLEX) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The fine-grained architecture and high register count characteristic of FPGAs are combined with the high speed and predictable interconnect delays of EPLDs to make the FLEX 8000 device family ideal for a wide range of applications. Logic is implemented with compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing, wide data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 2 shows the performance of FLEX 8000 devices as shown in benchmarks of typical applications.

Table 2. FLEX 8000 Performance *Note (1)*

		FLEX 8000A Devices			FLEX 8000 Devices		
Application	**Logic Elements Used**	**A-2 Speed Grade**	**A-3 Speed Grade**	**A-4 Speed Grade**	**-2 Speed Grade**	**-3 Speed Grade**	**Unit**
16-bit loadable counter	16	125	95	83	71	45	MHz
16-bit up/down counter	16	125	95	83	71	45	MHz
16-bit prescaled counter	24	270	232	185	142	115	MHz
24-bit accumulator	24	87	67	58	50	32	MHz
16-bit address decode	4	4.2	4.9	6.3	7.8	12.0	ns
16-to-1 multiplexer	10	6.6	7.9	9.5	12.7	18.0	ns

Note:
(1) The A-6 speed grade yields the same results as the -3 speed grade.

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast Clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an Altera serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1213 and EPC1064 Configuration EPROMs, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32K × 8-bit or larger EPROM or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

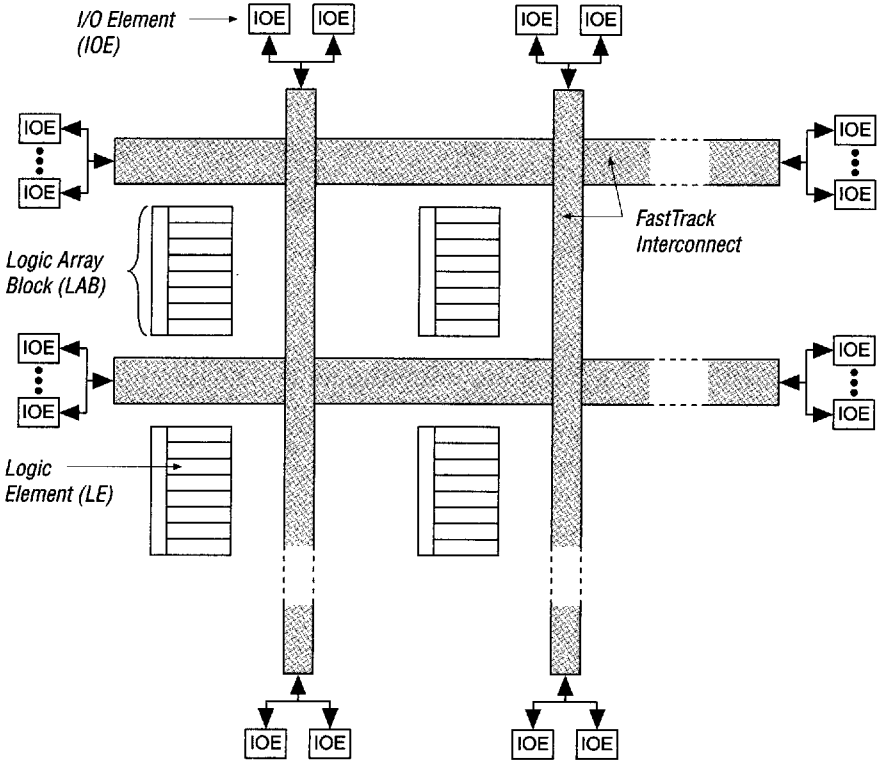
Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

LEs are grouped into sets of eight to create Logic Array Blocks (LABs). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

Figure 1. FLEX 8000 Device Block Diagram

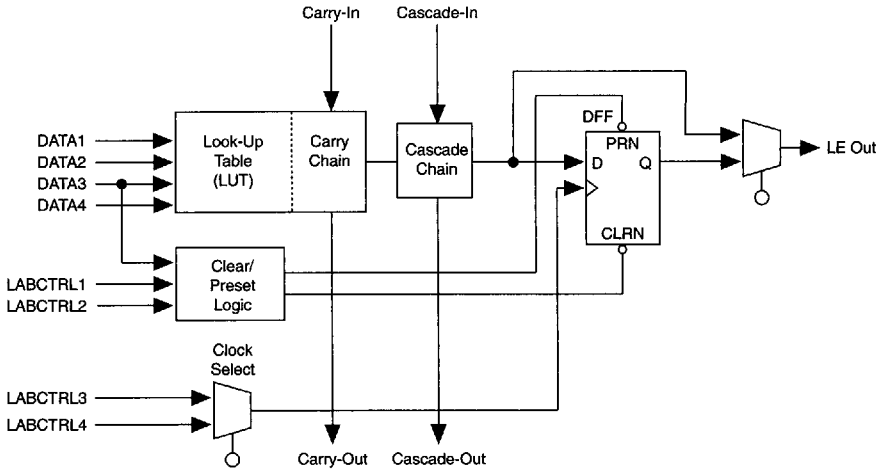


Signal interconnections within FLEX 8000 devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, a programmable flipflop, a carry chain, and a cascade chain. Figure 2 shows a block diagram of the LE.

Figure 2. FLEX 8000 Logic Element (LE)



The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The Clock, Clear, and Preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

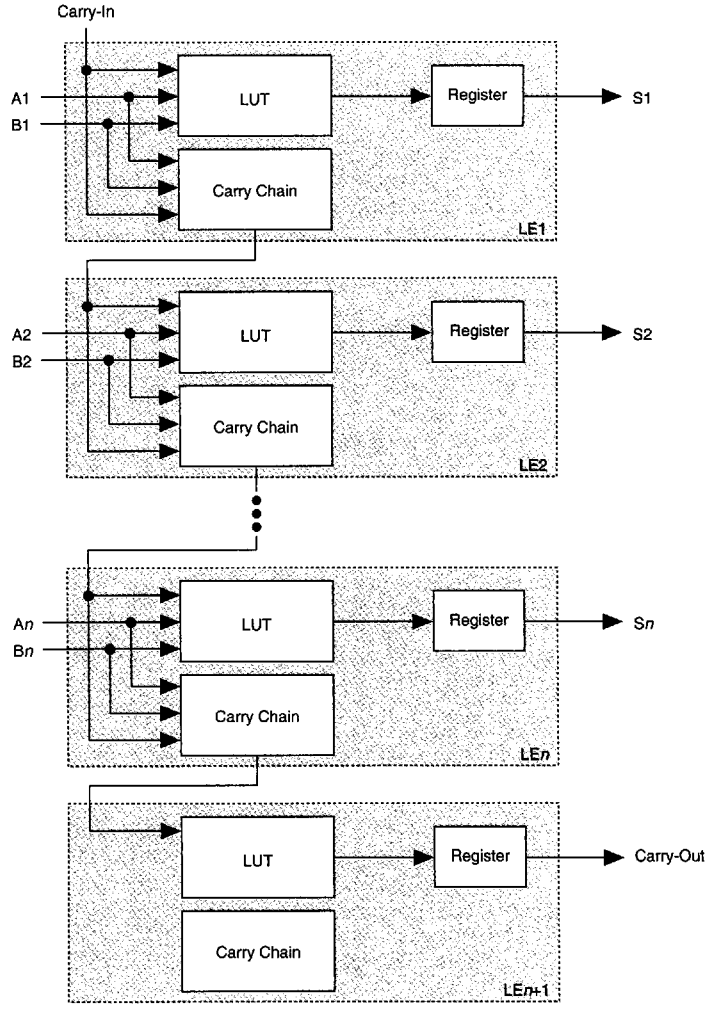
The FLEX 8000 architecture provides two dedicated high-speed data paths—carry chains and cascade chains—that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce the routing resources available for implementing other logic. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 3 shows how an *n*-bit full adder can be implemented in *n*+1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

Figure 3. Carry Chain Operation



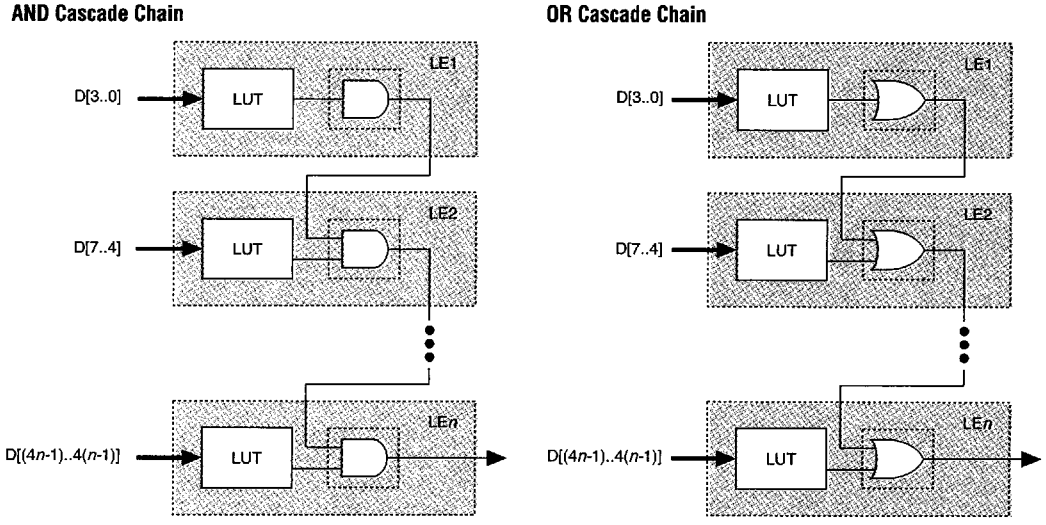
Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of

adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay of approximately 1 ns per LE. The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry.

Figure 4 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. For a device with an A-2 speed grade, the LUT delay is approximately 1.6 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

Figure 4. Cascade Chain Operation

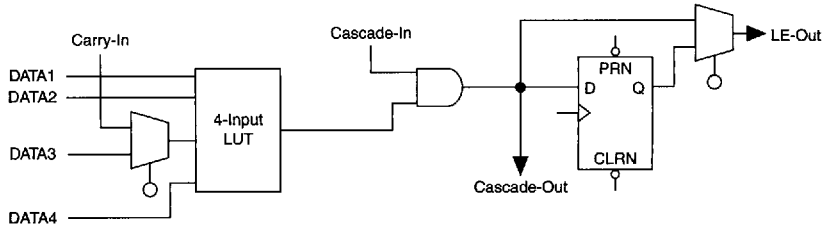


Logic Element Operating Modes

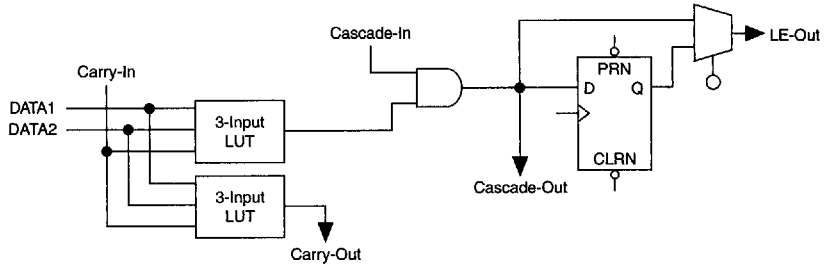
The FLEX 8000 logic element can operate in one of four modes, each of which uses LE resources differently. See Figure 5. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide Clock, Clear, and Preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Figure 5. FLEX 8000 Logic Element Operating Modes

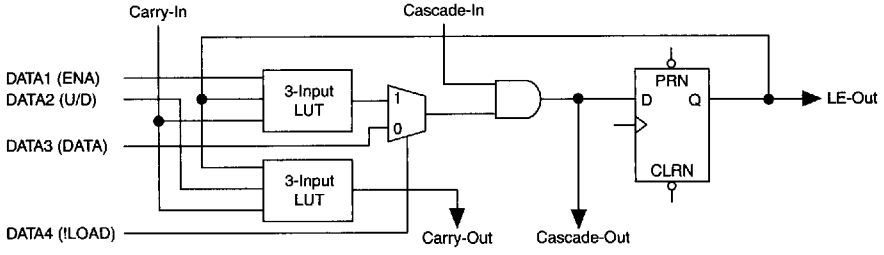
Normal Mode



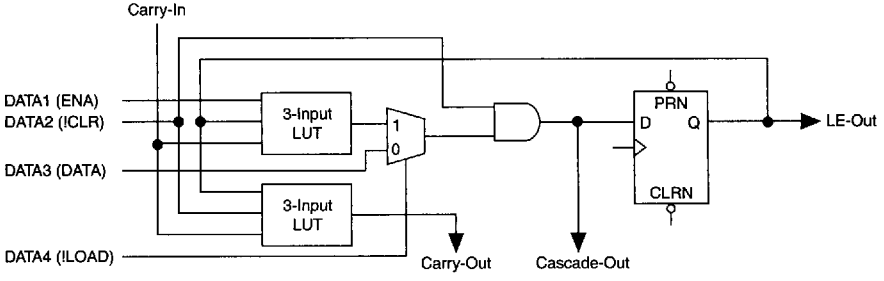
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The Normal mode is suitable for general logic applications and wide decode functions that can take advantage of a cascade chain. In Normal mode, four data inputs from the LAB local interconnect and the carry-in are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data (Q) output of the programmable register.

Arithmetic Mode

The Arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 5, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output would be the sum of three bits: A, B, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The Arithmetic mode also supports a cascade chain.

Up/Down Counter Mode

The Up/Down Counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the Clear and Preset register control signals, without using the LUT resources.

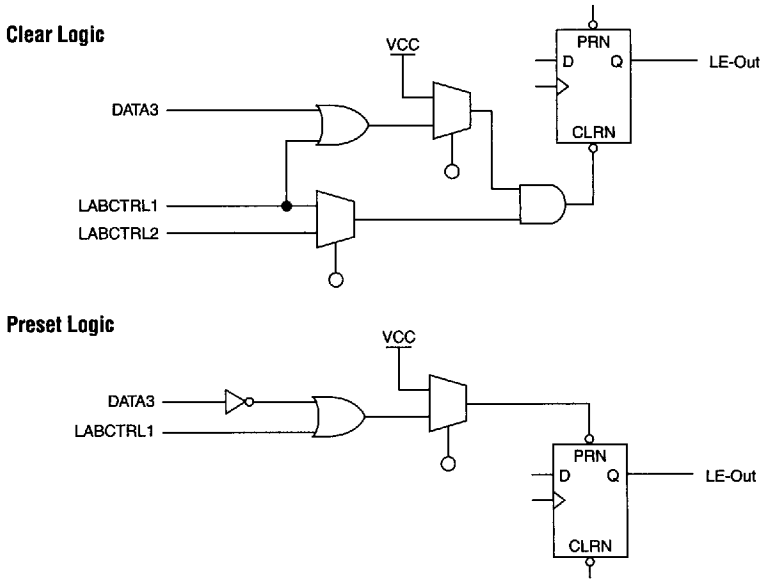
Clearable Counter Mode

The Clearable Counter mode is similar to the Up/Down Counter mode, but supports a synchronous Clear instead of the up/down control. The Clear function is substituted for the cascade-in signal in the Up/Down Counter mode. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, the output of which is ANDed with a synchronous Clear.

Clear/Preset Logic Control

Logic for the programmable register's Clear and Preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. See Figure 6.

Figure 6. Logic Element Clear & Preset Logic

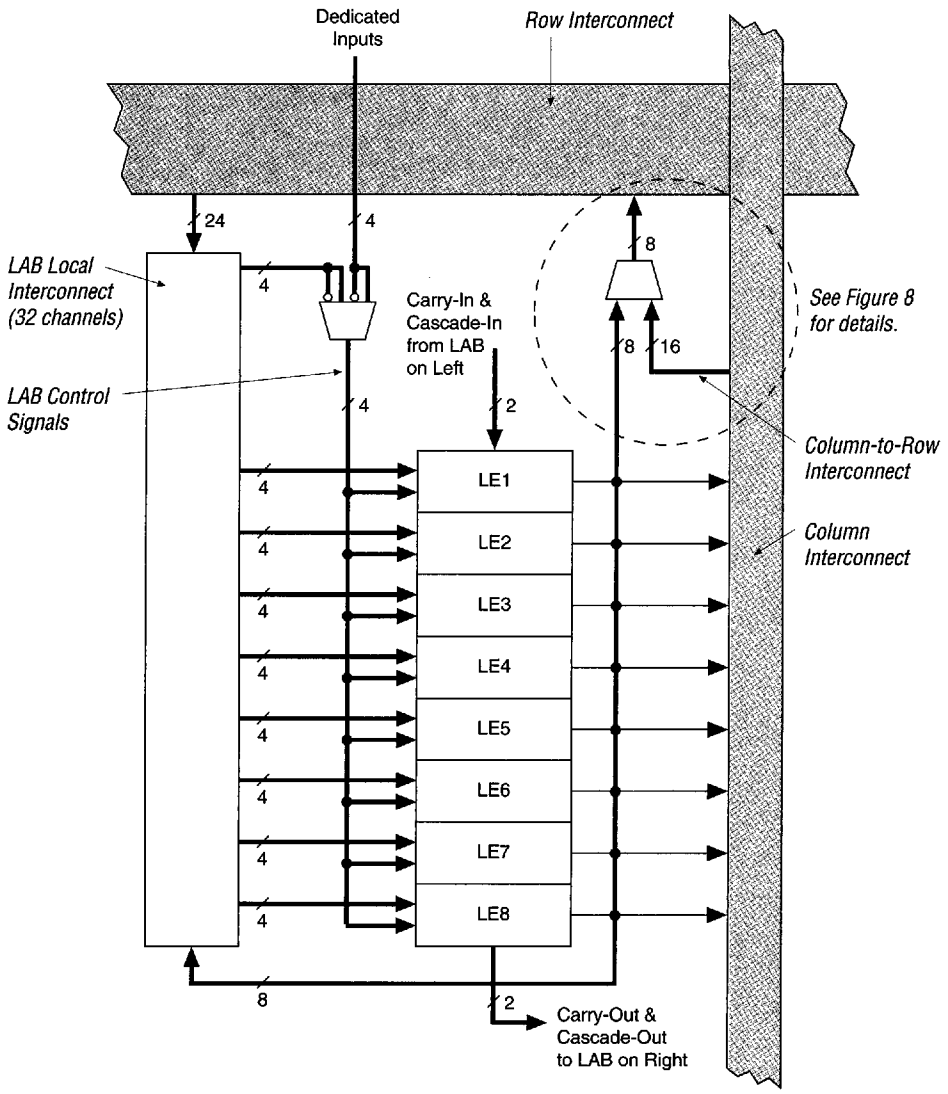


The Clear function is controlled by DATA3, LABCTRL1, and LABCTRL2; the Preset function is controlled by DATA3 and LABCTRL1. The MAX+PLUS II Compiler automatically selects the best control signal implementation during compilation. Since the Clear and Preset functions are active low, the Compiler automatically assigns a logic high to an unused Clear and/or Preset. Preset control can also be provided by using a Clear and inverting the output of the register. Inversion control is available for the inputs to both LEs and IOEs. If a register is cleared by only one of the two LABCTRL signals, the DATA3 input is not required and can be used for one of the LE operating modes.

Logic Array Block

A Logic Array Block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 7 shows a block diagram of the FLEX 8000 LAB.

Figure 7. Logic Array Block (LAB)



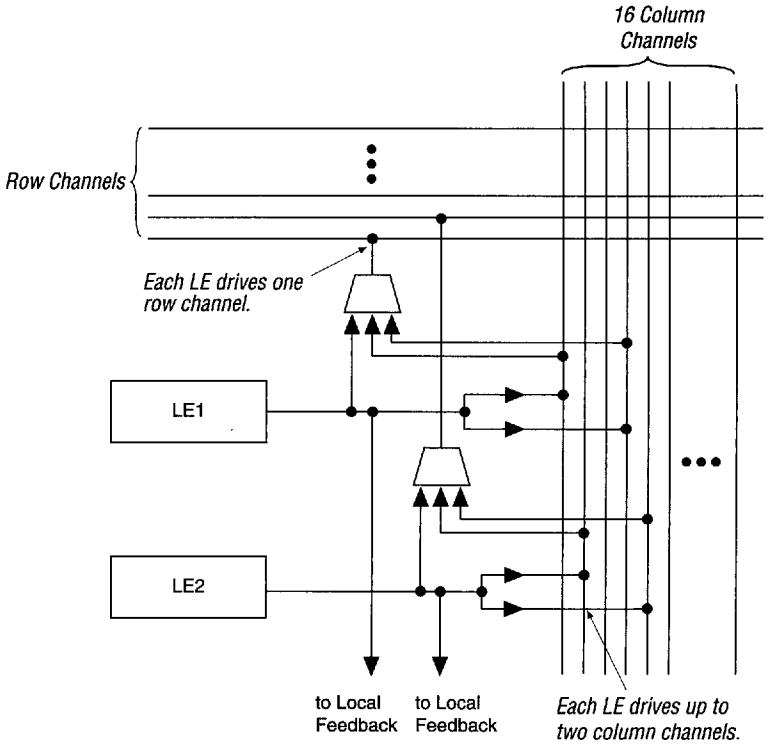
Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as Clocks, the other two for Clear/Preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global Clock, Clear, or Preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global Clock, Clear, or Preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. Programmable inversion is available for all four LAB control signals.

FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Figure 8 shows how an LE drives the row and column interconnect.

Figure 8. LAB Connections to Row & Column Interconnect



Each LE in an LAB can drive up to 2 separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by 2 column channels. These 3 signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 3 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

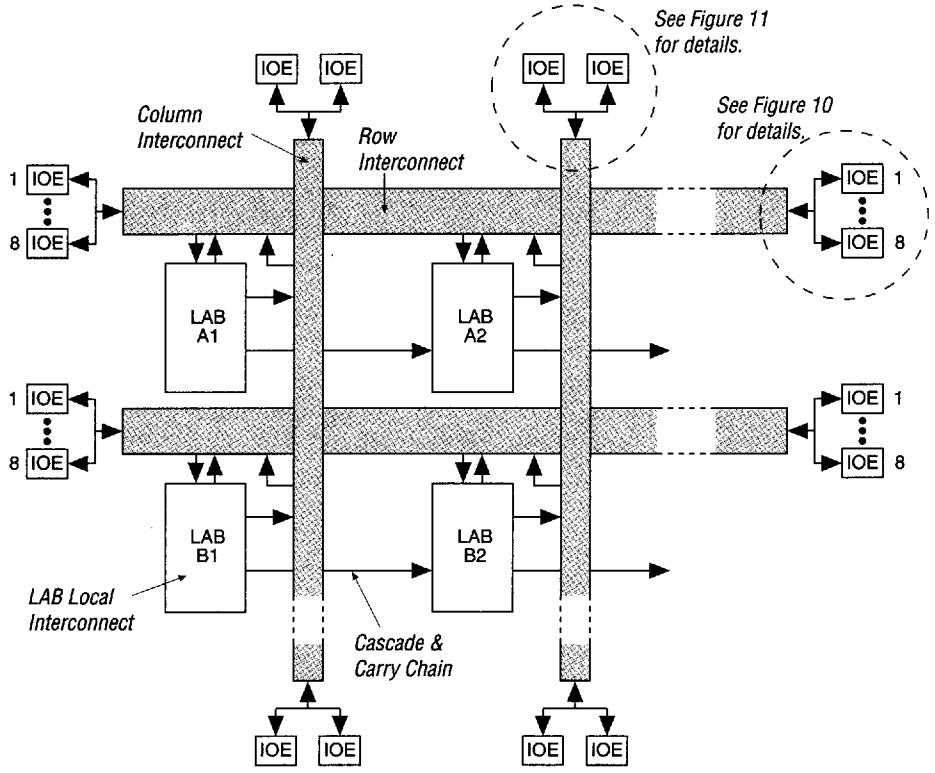
Table 3. FLEX 8000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282 EPF8282V EPF8282A EPF8282AV	2	168	13	16
EPF8452 EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820 EPF8820A	4	168	21	16
EPF81188 EPF81188A	6	168	21	16
EPF81500 EPF81500A	6	216	27	16

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 9. FLEX 8000 Device Interconnect Resources

Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.

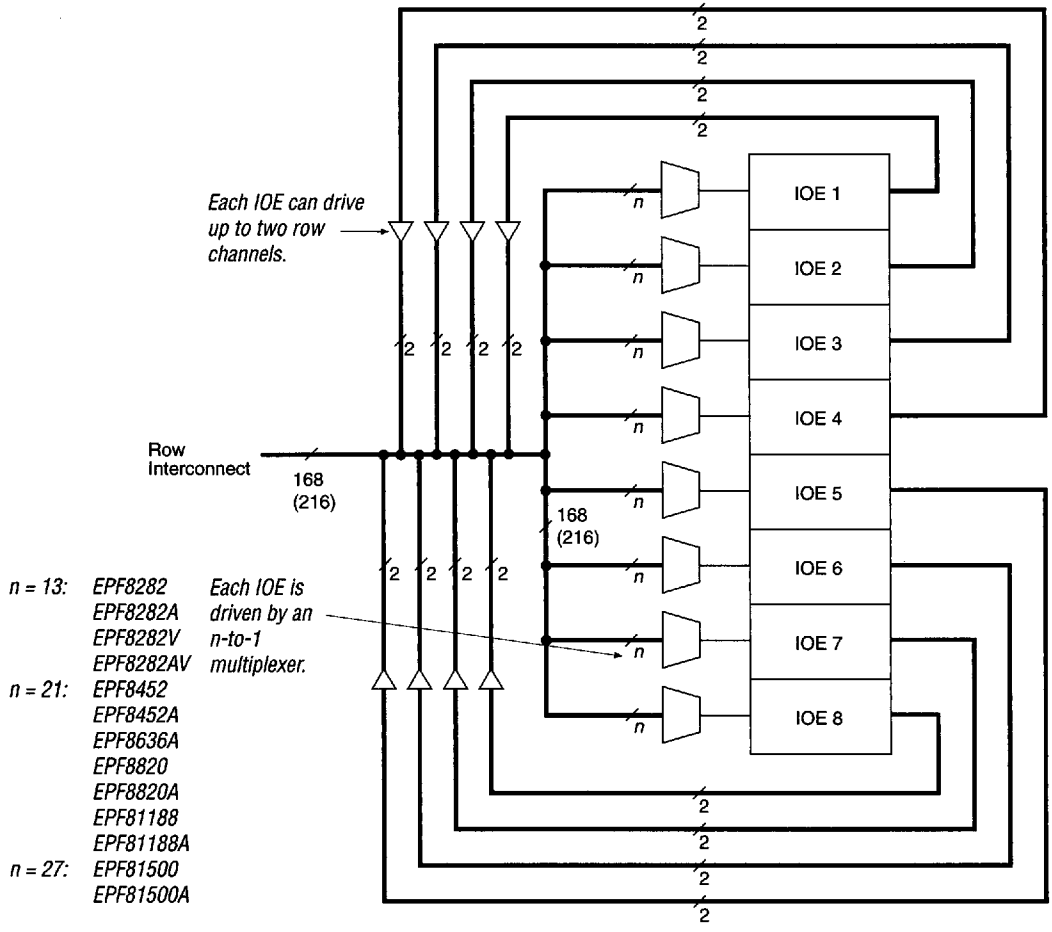


Row-to-IOE Connections

Figure 10 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an *n*-to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500 and EPF81500A devices use a 27-to-1 multiplexer; EPF81188, EPF81188A, EPF8820, EPF8820A, EPF8636A, EPF8452, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282, EPF8282A, EPF8282V and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

Figure 10. FLEX 8000 Row-to-IOE Connection

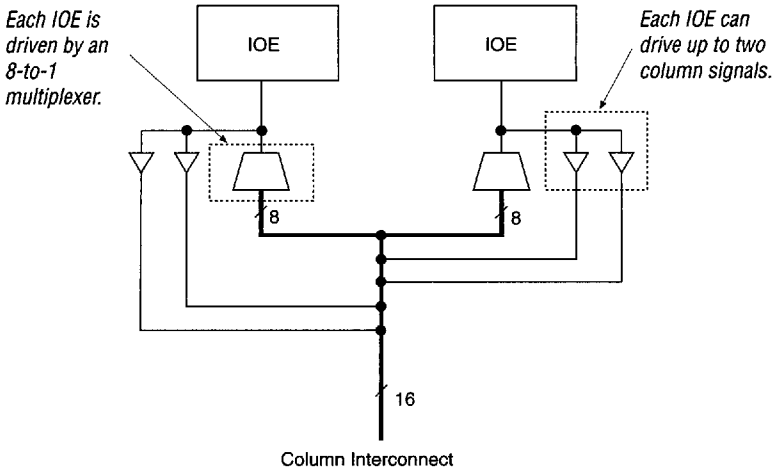
Numbers in parentheses are for EPF81500 & EPF81500A devices.



Column-to-IOE Connections

Two IOEs are located at the top and bottom of the column channels (see Figure 11). When an IOE is used as an input, it can drive up to 2 separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

Figure 11. FLEX 8000 Column-to-IOE Connection

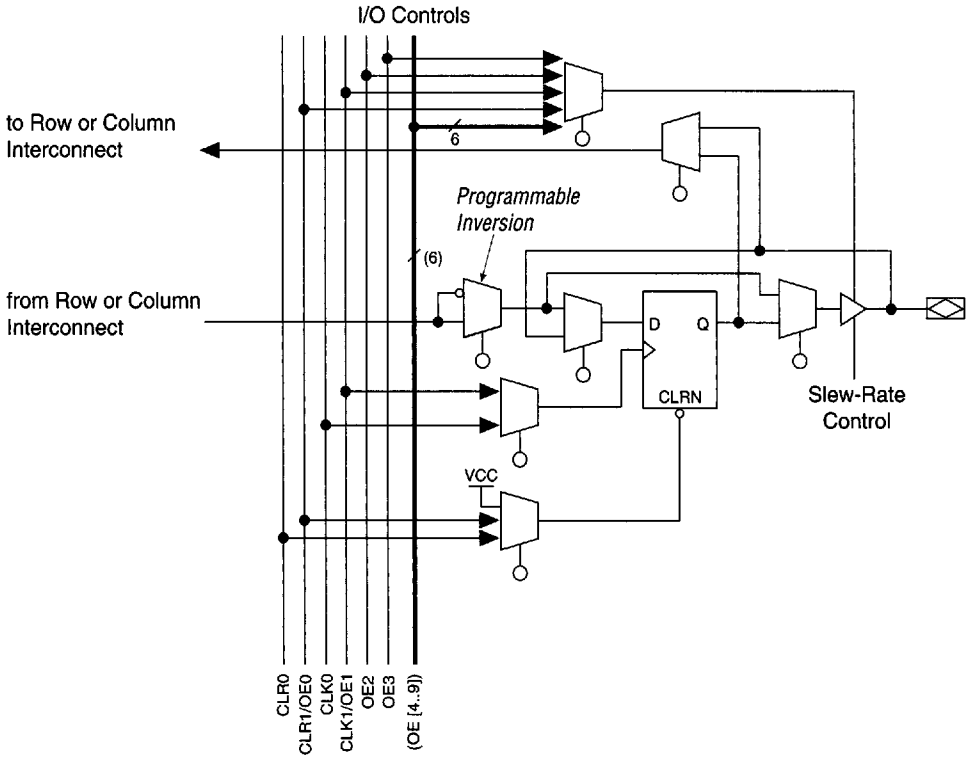


In addition to the general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global Clock, Clear, and Preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 12 shows the IOE block diagram. Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

Figure 12. I/O Element (IOE)

Numbers in parentheses are for EPF81500 and EPF81500A devices only.



I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast Clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect when appropriate.

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise and adds a maximum delay of 4 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

The Clock, Clear, and Output Enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four Output Enable signals (ten in the EPF81500 and EPF81500A), and up to two Clock or Clear signals. Figure 12 illustrates how two Output Enable signals are shared with one Clock (CLK1) and one Clear (CLR1) signal.

The signals for the peripheral bus can be generated by any of the 4 dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels used correlates to the number of columns in the FLEX 8000 device. EPF8282, EPF8282A, EPF8282V, and EPF8282AV devices, for example, use 13 channels; EPF8452, EPF8452A, EPF8636A, EPF8820, EPF8820A, EPF81188, and EPF81188A devices use 21 channels; and EPF81500 and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The 6 peripheral control signals (12 in EPF81500 and EPF81500A devices) can be accessed by every I/O element.

Figure 13. FLEX 8000 Peripheral Bus

Numbers in parentheses are for EPF81500 and EPF81500A devices.

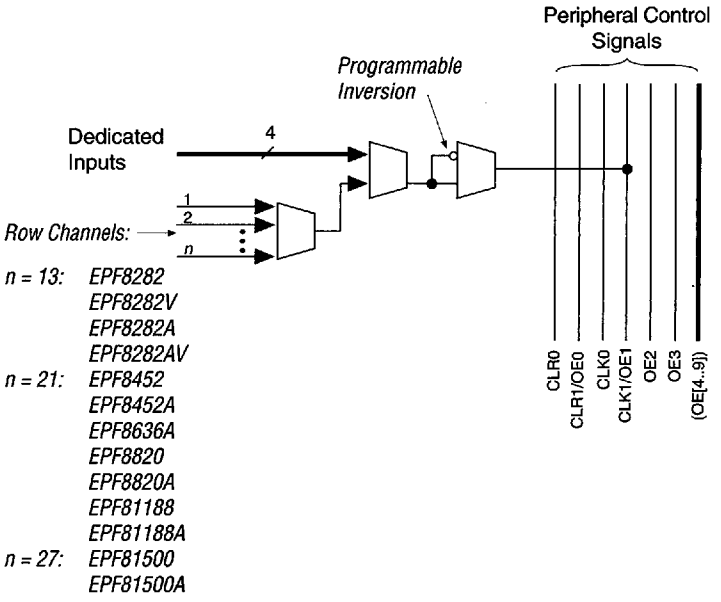


Table 4 lists the source of the peripheral control signal for each FLEX 8000 device by row.

Table 4. Row Sources of Peripheral Control Signals

Peripheral Control Signal	EPF8282 EPF8282V EPF8282A EPF8282AV	EPF8452 EPF8452A	EPF8636A	EPF8820 EPF8820A	EPF81188 EPF81188A	EPF81500 EPF81500A
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	–	–	–	–	–	Row B
OE5	–	–	–	–	–	Row C
OE6	–	–	–	–	–	Row D
OE7	–	–	–	–	–	Row D
OE8	–	–	–	–	–	Row E
OE9	–	–	–	–	–	Row F

3.3-V or 5.0-V I/O Operation

Many members of the FLEX 8000 family, including the EPF81500, EPF81500A, EPF81188, EPF81188A, EPF8820, EPF8820A, and EPF8636A devices (except the 84-pin PLCC EPF8636A), can be set for 3.3-V or 5.0-V operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with a V_{CCIO} levels lower than 4.75 V incur a nominal additional timing delay, therefore the t_{OD2} parameter is used in place of t_{OD1}.

JTAG Operation

The EPF8282, EPF8282A, EPF8282V, EPF8282AV, EPF8636A, EPF8820, EPF8820A, EPF81500, and EPF81500A devices provide Joint Test Action Group (JTAG) boundary-scan testing circuitry. For detailed information on JTAG operation in these FLEX 8000 devices, refer to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices).*

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and system-level performance analysis.

Tables 5 through 8 describe the FLEX 8000 timing parameters and their symbols.

Table 5. FLEX 8000 Internal Timing Parameters *Note (1)*

Symbol	Parameter
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF, *Note (2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF, *Note (3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on, C1 = 35 pF, *Note (4)*
t_{XZ}	Output buffer disable delay, C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF, *Note (3)*
t_{ZX3}	Output buffer enable delay, slow slew rate = on, C1 = 35 pF, *Note (4)*

Table 6. FLEX 8000 Logic Element Timing Parameters *Note (1)*	
Symbol	**Parameter**
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_{C}	LE register control signal delay
t_{CH}	Clock high time
t_{CL}	Clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 7. FLEX 8000 Interconnect Timing Parameters *Note (1)*	
Symbol	**Parameter**
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay, *Note (5)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay, *Note (5)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 8. FLEX 8000 External Reference Timing Characteristics *Note (6)*	
Symbol	**Parameter**
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects, *Note (7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and guaranteed external parameters. Internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) V_{CCIO} = 5.0 V ± 5% for commercial use.
V_{CCIO} = 5.0 V ± 10% for industrial and military use.
(3) V_{CCIO} = 3.3 V ± 10% for all temperature grades.
(4) For t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.
(5) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(6) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.
(7) Contact Altera Applications at (800) 800-EPLD for more information on test conditions.

The FLEX 8000 timing model in Figure 14 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 14 is expressed as a worst-case value in the "Timing Parameters" tables in this data sheet. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance.

Figure 14. FLEX 8000 Timing Model

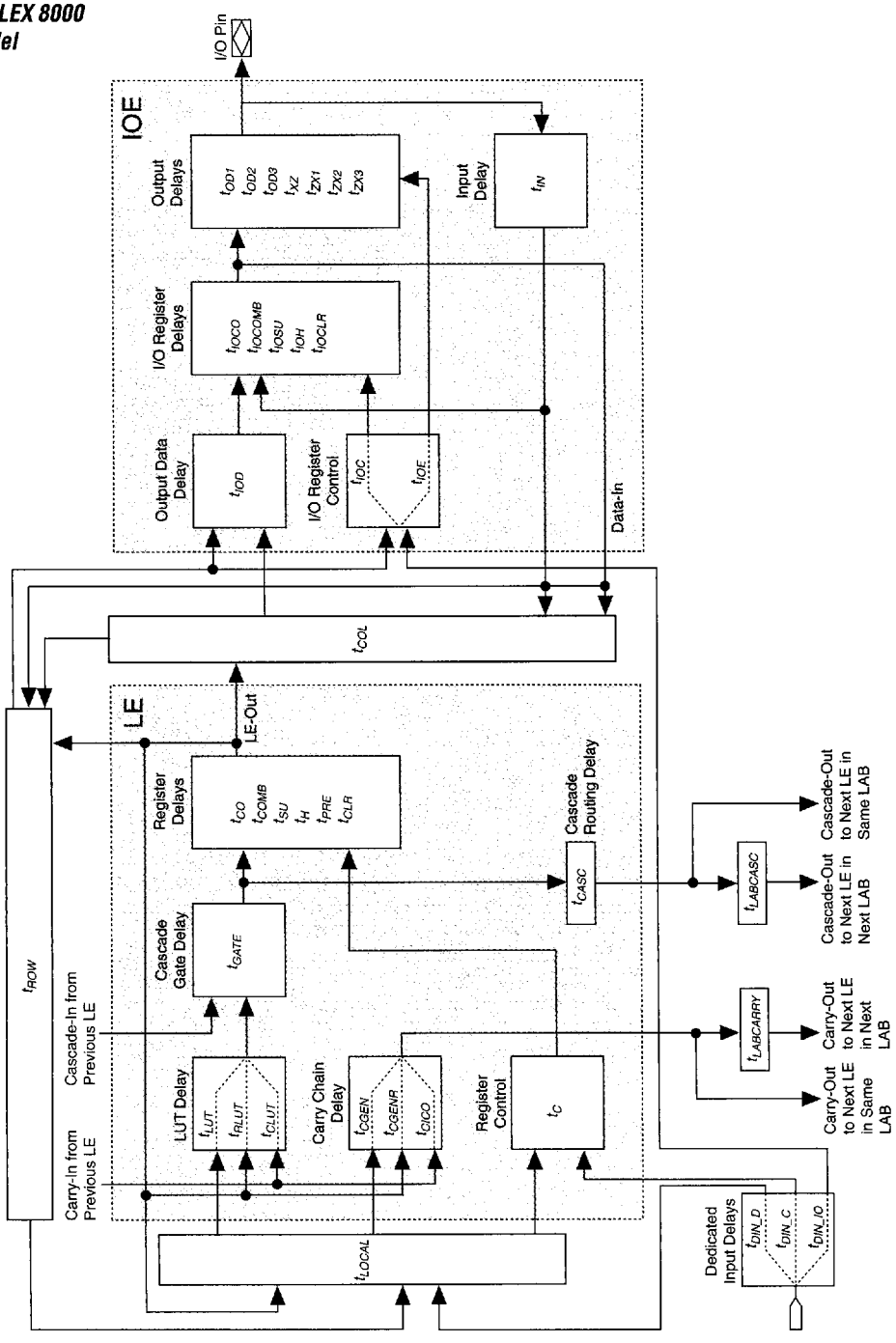


Table 9 summarizes the interconnect paths shown in Figure 14.

Table 9. FLEX 8000 Timing Model Interconnect Paths

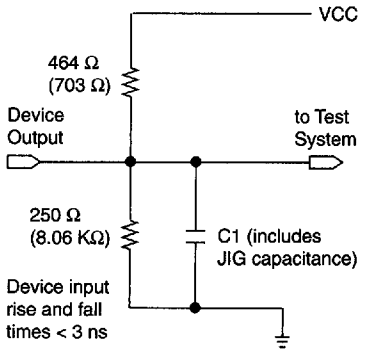
Source	Destination	Total Delay
LE-out	LE in same LAB	t_{LOCAL}
LE-out	LE in same row, different LAB	$t_{ROW} + t_{LOCAL}$
LE-out	LE in different row	$t_{COL} + t_{ROW} + t_{LOCAL}$
LE-out	IOE on column	t_{COL}
LE-out	IOE on row	t_{ROW}
IOE on row	LE in same row	$t_{ROW} + t_{LOCAL}$
IOE on column	Any LE	$t_{COL} + t_{ROW} + t_{LOCAL}$

Generic Testing

Each FLEX 8000 device is functionally tested and guaranteed. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 15. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices.



FLEX 8000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

FLEX 8000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*Note (3)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation		3.00	3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 8000 5.0-V Device DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V	2.4			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load		500		µA

FLEX 8000 5.0-V Device Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions.
(4) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(5) Operating conditions:
V_{CCINT} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CCINT} = 5 V ± 10%, T_A = –55° C to 125° C for military use.
(6) Capacitance is sample-tested only.

FLEX 8000 3.3-V Device Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

FLEX 8000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 8000 3.3-V Device DC Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = 0.1 mA DC	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (3)*		300		µA

FLEX 8000 3.3-V Device Capacitance *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Operating conditions:
V_{CCIO} = 3.3 V ± 10% for commercial use.
V_{CCIO} = 3.3 V ± 10% for industrial use.
V_{CCIO} = 3.3 V ± 10% for military use.
(3) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(4) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices with 5.0-V V_{CCIO}. The output driver is compatible with the PCI local bus specification.

Figure 16. Output Drive Characteristics for 5.0-V Devices, 5.0-V V_{CCIO}

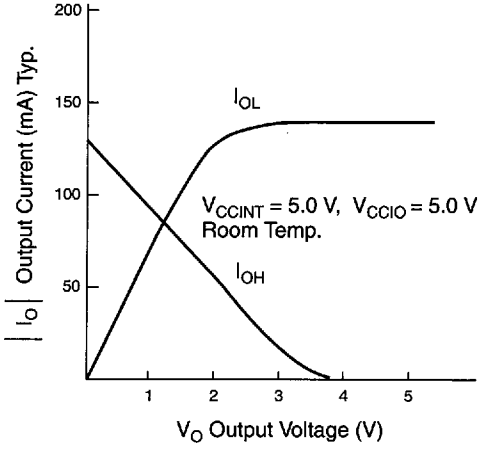


Figure 17 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices with 3.3-V V_{CCIO}. The output driver is compatible with the PCI local bus specification.

Figure 17. Output Drive Characteristics for 5.0-V Devices, 3.3-V V_{CCIO}

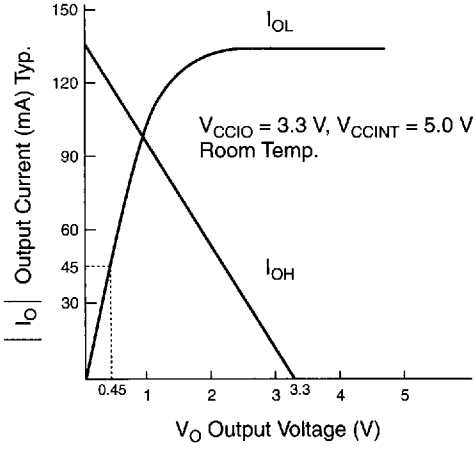
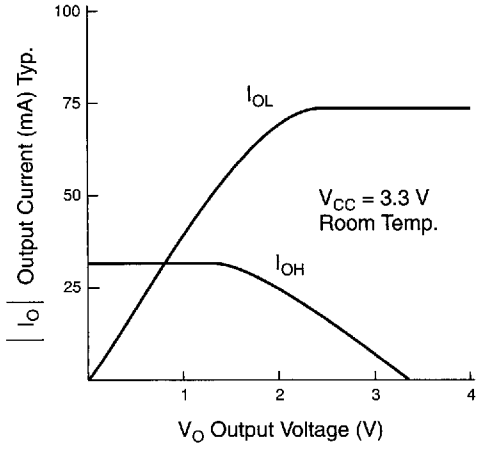


Figure 18 shows the typical output drive characteristics of EPF8282V I/O pins.

Figure 18. EPF8282V Typical Output Drive Characteristics



EPF8282 Internal Timing Parameters *Note (1)*

EPF8282 I/O Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.3		1.3	ns
t_{IN}		1.5		1.6		1.7		1.8		2.8	ns
t_{OD1}		1.1		1.4		1.7		2.5		3.0	ns
t_{OD2}		1.6		1.9		2.2		–		–	ns
t_{OD3}		4.6		4.9		5.2		6.5		7.0	ns
t_{XZ}		1.4		1.6		1.8		2.5		3.0	ns
t_{ZX1}		1.4		1.6		1.8		2.5		3.0	ns
t_{ZX2}		1.9		2.1		2.3		–		–	ns
t_{ZX3}		4.9		5.1		5.3		6.5		7.0	ns

EPF8282 Interconnect Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0	ns
t_{ROW}		4.2		4.2		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0	ns
t_{DIN_D}		7.2		7.2		7.2		7.2		8.2	ns
t_{DIN_IO}		5.0		5.0		5.5		7.0		8.0	ns

EPF8282 Logic Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.7		1.2	ns

EPF8282 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		15.8		19.8		24.8		29.3		35.5	ns

Note:
(1) Internal and external timing parameters for EPF8282A devices are preliminary.

EPF8282V Internal Timing Parameters

EPF8282V I/O Element Timing Parameters					
Parameter	-3 Speed Grade		-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		2.2		3.5	ns
t_{IOC}		2.0		3.4	ns
t_{IOE}		2.0		3.4	ns
t_{IOCO}		2.0		3.0	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	2.8		4.7		ns
t_{IOH}	0.2		0.1		ns
t_{IOCLR}		2.3		3.5	ns
t_{IN}		3.4		5.4	ns
t_{OD1}		4.1		5.6	ns
t_{OD2}		–		–	ns
t_{OD3}		7.1		9.6	ns
t_{XZ}		4.3		6.7	ns
t_{ZX1}		4.3		6.7	ns
t_{ZX2}		–			ns
t_{ZX3}		8.3			ns

EPF8282V Interconnect Timing Parameters					
Parameter	-3 Speed Grade		-4 Speed Grade		
	Max	**Min**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		1.3		2.0	ns
$t_{LABCARRY}$		0.8		1.2	ns
t_{LOCAL}		1.5		1.5	ns
t_{ROW}		6.3		6.3	ns
t_{COL}		3.8		3.8	ns
t_{DIN_C}		8.0		10.3	ns
t_{DIN_D}		10.8		12.3	ns
t_{DIN_IO}		9.0		12.3	ns

EPF8282V Logic Element Timing Parameters					
Parameter	-3 Speed Grade		-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		7.3		14.3	ns
t_{CLUT}		1.4		1.3	ns
t_{RLUT}		5.1		7.3	ns
t_{GATE}		0.0		0.0	ns
t_{CASC}		2.8		4.2	ns
t_{CICO}		1.5		2.2	ns
t_{CGEN}		2.2		4.5	ns
t_{CGENR}		3.7		6.0	ns
t_{C}		4.7		9.5	ns
t_{CH}		6.0		10.5	ns
t_{CL}		6.0		10.5	ns
t_{CO}		0.9		0.9	ns
t_{COMB}		0.9		0.9	ns
t_{SU}	2.4		4.4		ns
t_{H}	4.6		6.8		ns
t_{PRE}		1.3		1.6	ns
t_{CLR}		1.3		1.6	ns

EPF8282V External Reference Timing Characteristics

Parameter	-3 Speed Grade		-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		50.1		80.4	ns

EPF8452 Internal Timing Parameters *Note (1)*

EPF8452 I/O Element Timing Parameters													
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.8		0.9		1.0		2.0		1.0		2.0	ns
t_{IOC}		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOE}		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.2		0.1		0.0		0.0		0.0		0.0	ns
t_{IOSU}	1.6		1.8		2.0		2.0		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.6		1.7		1.8		2.8		1.8		2.8	ns
t_{OD1}		1.4		1.7		2.0		2.0		2.0		2.0	ns
t_{OD2}		1.9		2.2		2.5		3.0		3.0		3.0	ns
t_{OD3}		4.9		5.2		5.5		6.0		6.0		6.0	ns
t_{XZ}		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX1}		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX2}		2.1		2.3		2.5		3.0		3.0		3.0	ns
t_{ZX3}		5.1		5.3		5.5		6.0		6.0		6.0	ns

EPF8452 Interconnect Timing Parameters													
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.4		0.4		0.5		0.9		0.5		0.9	ns
$t_{LABCARRY}$		0.4		0.4		0.5		0.6		0.5		0.6	ns
t_{LOCAL}		0.5		0.7		0.9		1.0		1.0		1.0	ns
t_{ROW}		5.0		5.0		5.0		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.5		6.0		7.0		6.0		7.0	ns
t_{DIN_D}		7.0		7.5		8.0		9.0		8.0		9.0	ns
t_{DIN_IO}		5.0		5.5		6.0		9.0		8.0		9.0	ns

EPF8452 Logic Element Timing Parameters

Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.3		3.0		3.7		5.1		4.1		5.1	ns
t_{CLUT}		0.2		0.1		0.1		1.0		0.2		1.0	ns
t_{RLUT}		1.6		1.6		1.9		3.4		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.7		0.9		1.1		2.0		1.1		2.0	ns
t_{CICO}		0.5		0.6		0.7		1.1		0.7		1.1	ns
t_{CGEN}		0.9		0.8		0.9		1.4		0.7		1.4	ns
t_{CGENR}		1.4		1.5		1.8		2.4		1.7		2.4	ns
t_{C}		1.8		2.4		2.9		3.1		2.8		3.1	ns
t_{CH}	1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CL}	1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CO}		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{COMB}		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{SU}	1.0		1.1		1.2		1.7		1.5		1.7		ns
t_{H}	1.1		1.4		1.8		4.0		2.3		4.0		ns
t_{PRE}		0.7		0.8		0.9		1.2		0.7		1.2	ns
t_{CLR}		0.7		0.8		0.9		1.2		0.7		1.2	ns

EPF8452 External Reference Timing Characteristics *Note (1)*

Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		20.0		25.0		30.0		38.2		32.0		38.2	ns

Note:
(1) Internal and external timing parameters for EPF8452A devices are preliminary.

EPF8636A Internal Timing Parameters *Note (1)*

EPF8636A I/O Element Timing Parameters							
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.8		0.9		1.0	ns
t_{IOC}		1.8		1.9		2.0	ns
t_{IOE}		1.8		1.9		2.0	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.2		0.1		0.0	ns
t_{IOSU}	1.6		1.8		2.0		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.6		1.7		1.8	ns
t_{OD1}		1.4		1.7		2.0	ns
t_{OD2}		1.9		2.2		2.5	ns
t_{OD3}		4.9		5.2		5.5	ns
t_{XZ}		1.6		1.8		2.0	ns
t_{ZX1}		1.6		1.8		2.0	ns
t_{ZX2}		2.1		2.3		2.5	ns
t_{ZX3}		5.1		5.3		5.5	ns

EPF8636A Interconnect Timing Parameters							
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.4		0.4		0.5	ns
$t_{LABCARRY}$		0.4		0.4		0.5	ns
t_{LOCAL}		0.5		0.7		0.9	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.5		6.0	ns
t_{DIN_D}		7.0		7.5		8.0	ns
t_{DIN_IO}		5.0		5.5		6.0	ns

EPF8636A Logic Element Timing Parameters							
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.3		3.0		3.7	ns
t_{CLUT}		0.2		0.1		0.1	ns
t_{RLUT}		1.6		1.6		1.9	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.7		0.9		1.1	ns
t_{CICO}		0.5		0.6		0.7	ns
t_{CGEN}		0.9		0.8		0.9	ns
t_{CGENR}		1.4		1.5		1.8	ns
t_{C}		1.8		2.4		2.9	ns
t_{CH}	1.7		2.7		3.4		ns
t_{CL}	1.7		2.7		3.4		ns
t_{CO}		0.5		0.6		0.7	ns
t_{COMB}		0.5		0.6		0.7	ns
t_{SU}	1.0		1.1		1.2		ns
t_{H}	1.1		1.4		1.8		ns
t_{PRE}		0.7		0.8		0.9	ns
t_{CLR}		0.7		0.8		0.9	ns

EPF8636A External Reference Timing Characteristics *Note (1)*

Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		20.0		25.0		30.0	ns

Note:
(1) Internal and external timing parameters for EPF8636A devices are preliminary.

EPF8820 Internal Timing Parameters *Note (1)*

EPF8820 I/O Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7		1.8		2.8	ns
t_{OD1}		1.1		1.4		1.7		2.0		2.0	ns
t_{OD2}		1.6		1.9		2.2		3.0		3.0	ns
t_{OD3}		4.6		4.9		5.2		6.0		6.0	ns
t_{XZ}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX1}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX2}		1.9		2.1		2.3		3.0		3.0	ns
t_{ZX3}		4.9		5.1		5.3		6.0		6.0	ns

EPF8820 Interconnect Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0	ns
t_{ROW}		5.0		5.0		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0	ns
t_{DIN_D}		7.0		7.0		7.5		8.0		9.0	ns
t_{DIN_IO}		5.0		5.0		5.5		8.0		9.0	ns

EPF8820 Logic Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.7		1.2	ns

EPF8820 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0		32.0		38.2	ns

Note:
(1) Internal and external timing parameters for EPF8820A devices are preliminary.

EPF81188 Internal Timing Parameters *Note (1)*

EPF81188 I/O Element Timing Parameters															
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9		1.0		2.0		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7		1.8		2.8		1.8		2.8	ns
t_{OD1}		1.1		1.4		1.7		2.0		2.0		2.0		2.0	ns
t_{OD2}		1.6		1.9		2.2		2.5		3.0		3.0		3.0	ns
t_{OD3}		4.6		4.9		5.2		5.5		6.0		6.0		6.0	ns
t_{XZ}		1.4		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX1}		1.4		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX2}		1.9		2.1		2.3		2.5		2.5		3.0		3.0	ns
t_{ZX3}		4.9		5.1		5.3		5.5		5.5		6.0		6.0	ns

EPF81188 Interconnect Timing Parameters															
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0		1.0		1.0	ns
t_{ROW}		5.0		5.0		5.0		5.0		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0		6.0		7.0	ns
t_{DIN_D}		7.0		7.0		7.5		8.0		8.0		8.0		9.0	ns
t_{DIN_IO}		5.0		5.0		5.5		6.0		9.0		8.0		9.0	ns

EPF81188 Logic Element Timing Parameters															
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		3.9		5.1		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.0		1.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.8		3.4		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.8		1.4		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.8		2.4		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		3.0		3.1		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.3		1.7		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		1.9		4.0		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.9		1.2		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.9		1.2		0.7		1.2	ns

EPF81188 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0		30.0		38.2		32.0		38.2	ns

Note:
(1) Internal and external timing parameters for EPF81188A devices are preliminary.

EPF81500 Internal Timing Parameters *Note (1)*

EPF81500 I/O Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7		1.8		1.8	ns
t_{OD1}		1.1		1.4		1.7		2.0		2.0	ns
t_{OD2}		1.6		1.9		2.2		3.0		3.0	ns
t_{OD3}		4.6		4.9		5.2		6.0		6.0	ns
t_{XZ}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX1}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX2}		1.9		2.1		2.3		3.0		3.0	ns
t_{ZX3}		4.9		5.1		5.3		6.0		6.0	ns

EPF81500 Interconnect Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0	ns
t_{ROW}		6.2		6.2		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0	ns
t_{DIN_D}		8.2		8.2		8.7		9.2		10.20	ns
t_{DIN_IO}		5.0		5.0		5.5		8.0		9.0	ns

EPF81500 Logic Element Timing Parameters

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.7		1.2	ns

EPF81500 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.1		20.1		25.1		34.0		40.2	ns

Note:
(1) Internal and external timing parameters for EPF81500A devices are preliminary.

Calculating the Supply Current

The V_{CC} supply current for FLEX 8000 devices, I_{CC}, can be calculated with the following equation:

$$I_{CC} = I_{CCSTANDBY} + I_{CCOUTPUT} + I_{CCACTIVE}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 8000 5.0-V Device DC Operating Conditions" and "FLEX 8000 3.3-V Device DC Operating Conditions" tables earlier in this data sheet. The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Operating Requirements for Altera Devices* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times F \times N \times 0.125 \times \frac{\mu A}{MHz \times LE}$$

In this equation, F is the maximum operating frequency in MHz; N is the number of LEs used in the device. The total is multiplied by 0.125, which is based on a 16-bit counter in which 2 out of 16 (12.5%) of the output bits switch on each Clock edge.

Table 10 shows the value of the constant (K) for FLEX 8000 devices.

Table 10. Current Consumed per LE

Device	K
5.0-V FLEX 8000 devices	75
3.3-V FLEX 8000 devices	60
5.0-V FLEX 8000A devices	75 *Note (1)*

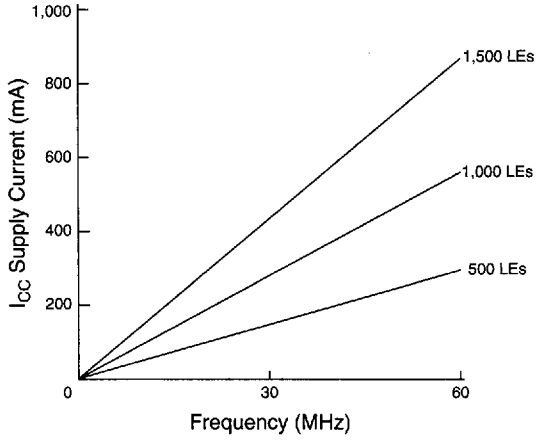
Note:
(1) This information is preliminary.

Figure 19 shows the relationship between I_{CC} and operating frequency for several LE utilization values.

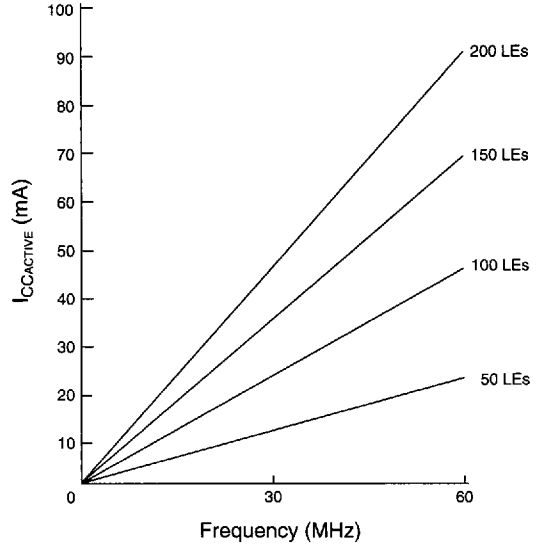
Figure 19. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000 Devices & 5.0-V FLEX 8000A Devices

Information on 5.0-V FLEX 8000A devices is preliminary.



3.3-V FLEX 8000 Devices



Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This data sheet summarizes the device operating modes and available device configuration schemes.

Go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* for detailed descriptions of device configuration options; device configuration pins; and information on configuring FLEX 8000 devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 8000 architecture uses SRAM elements that requires configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external EPROM devices, and completing the loading process. The Clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device, which operates as a slave. Table 11 shows the source of data for each of the six configuration schemes.

Table 11. Configuration Schemes

Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera Configuration EPROM
Active parallel up	APU	Parallel EPROM
Active parallel down	APD	Parallel EPROM
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Device Pin-Outs

Tables 12 through 14 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

Table 12. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	84-Pin PLCC EPF8452 EPF8452A EPF8636A	84-Pin PLCC EPF8282 EPF8282A	100-Pin TQFP EPF8282 EPF8282A	160-Pin PGA EPF8452 EPF8452A	160-Pin PQFP EPF8820A *Note (1)*	160-Pin PQFP EPF8452 EPF8452A
nSP *(1)*	75	75	75	R1	1	120
MSEL0 *(1)*	74	74	74	P2	2	117
MSEL1 *(1)*	53	53	51	A1	44	84
nSTATUS *(1)*	32	32	24	C13	82	37
nCONFIG *(1)*	33	33	25	A15	81	40
DCLK *(1)*	10	10	100	P14	125	1
CONF_DONE *(1)*	11	11	1	N13	124	4
nWS	30	30	22	F13	87	30
nRS	48	48	42	C6	89	71
RDCLK	49	49	45	B5	110	73
nCS	29	29	21	D15	118	29
CS	28	28	19	E15	121	27
RDYnBUSY	77	77	77	P3	100	125
CLKUSR	50	50	47	C5	107	76
ADD17	51	51	49	B4	40	78
ADD16	55	36	28	E2	39	91
ADD15	56	56	55	D1	38	92
ADD14	57	57	57	E1	37	94
ADD13	58	58	58	F3	36	95
ADD12	60	60	59	F2	32	96
ADD11	61	61	60	F1	30	97
ADD10	62	62	61	G2	28	98
ADD9	63	63	62	G1	26	99
ADD8	64	64	64	H1	22	101
ADD7	65	65	65	H2	20	102
ADD6	66	66	66	J1	18	103
ADD5	67	67	67	J2	16	104
ADD4	69	69	68	K2	11	105
ADD3	70	70	69	K1	10	106
ADD2	71	71	71	K3	8	109
ADD1	72	76	76	M1	7	110
ADD0	76	78	78	N3	6	123
DATA7	2	3	90	P8	140	144
DATA6	4	4	91	P10	139	150

Table 12. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	84-Pin PLCC EPF8452 EPF8452A EPF8636A	84-Pin PLCC EPF8282 EPF8282A	100-Pin TQFP EPF8282 EPF8282A	160-Pin PGA EPF8452 EPF8452A	160-Pin PQFP EPF8820A *Note (1)*	160-Pin PQFP EPF8452 EPF8452A
DATA5	6	6	92	R12	138	152
DATA4	7	7	95	R13	136	154
DATA3	8	8	97	P13	135	157
DATA2	9	9	99	R14	133	159
DATA1	13	13	4	N15	132	11
DATA0	14	14	5	K13	129	12
TDI *(2)*	45 *(3)*	55	54	–	17	–
TDO *(2)*	27 *(3)*	27	18	–	102	–
TCLK *(2)*	44 *(3)*	72	72	–	27	–
TMS *(2)*	43 *(3)*	20	11	–	29	–
nTRST *(1)*	52 *(4)*	52	50	–	45	–
Dedicated Inputs	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	C3, D14, N2, R15	14, 33, 94, 113	5, 36, 85, 116
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160
VCCIO	–	–	–	–	23, 47, 57, 69, 79, 104, 127, 137, 149, 159	–
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155
No Connect (N.C.)	–	–	–	–	–	2, 3, 38, 39, 70, 82, 83, 118, 119, 148
Total User I/O Pins	64	64	74	116	116	116

Table 13. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	160-Pin PQFP EPF8636A *Note (1)*	192-Pin PGA EPF8636A EPF8820 EPF8820A	208-Pin RQFP EPF8636A	208-Pin RQFP EPF8820 EPF8820A	208-Pin PQFP EPF81188A *Note (1)*	225-Pin BGA EPF8820 EPF8820A
nSP *(1)*	1	R15	207	207	5	A15
MSEL0 *(1)*	3	T15	4	4	21	B14
MSEL1 *(1)*	38	T3	49	49	33	R15
nSTATUS *(1)*	83	B3	108	108	124	P2
nCONFIG *(1)*	81	C3	103	103	107	R1
DCLK *(1)*	120	C15	158	158	154	B2
CONF_DONE *(1)*	118	B15	153	153	138	A1
nWS	89	C5	114	114	118	L4
nRS	50	B5	66	116	121	K5
RDCLK	48	C11	64	137	137	F1
nCS	91	B13	116	145	142	D1
CS	93	A16	118	148	144	C1
RDYnBUSY	155	A8	201	127	128	J3
CLKUSR	44	A10	59	134	134	G2
ADD17	43	R5	57	43	46	M14
ADD16	33	U3	43	42	45	L12
ADD15	31	T5	41	41	44	M15
ADD14	29	U4	39	40	39	L13
ADD13	27	R6	37	39	37	L14
ADD12	24	T6	31	35	36	K13
ADD11	23	R7	30	33	31	K15
ADD10	22	T7	29	31	30	J13
ADD9	21	T8	28	29	29	J15
ADD8	20	U9	24	25	26	G14
ADD7	19	U10	23	23	25	G13
ADD6	18	U11	22	21	24	G11
ADD5	17	U12	21	19	18	F14
ADD4	13	R12	14	14	17	E13
ADD3	11	U14	12	13	16	D15
ADD2	9	U15	10	11	10	D14
ADD1	7	R13	8	10	9	E12
ADD0	157	U16	203	9	8	C15
DATA7	137	H17	178	178	177	A7
DATA6	132	G17	172	176	175	D7

Table 13. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	160-Pin PQFP EPF8636A *Note (1)*	192-Pin PGA EPF8636A EPF8820 EPF8820A	208-Pin RQFP EPF8636A	208-Pin RQFP EPF8820 EPF8820A	208-Pin PQFP EPF81188A *Note (1)*	225-Pin BGA EPF8820 EPF8820A
DATA5	129	F17	169	174	172	A6
DATA4	127	E17	165	172	170	A5
DATA3	124	G15	162	171	168	B5
DATA2	122	F15	160	167	166	E6
DATA1	115	E16	149	165	163	D5
DATA0	113	C16	147	162	161	C4
TDI *(2)*	55	R11	72	20	–	F15
TDO *(2)*	95	B9	120	129	–	J2
TCLK *(2)*	57	U8	74	30	–	J14
TMS *(2)*	59	U7	76	32	–	J12
nTRST *(1)*	40	R3	54	54	–	P14
Dedicated Inputs	6, 35, 87, 116	A5, U5, U13, A13	7, 45, 112, 150	17, 36, 121, 140	13, 41, 116, 146	F4, L1, K12, E15
VCCINT (5.0 V)	4, 5, 26, 85, 106	C8, C9, C10, R8, R9, R10, R14	5, 6, 33, 110, 137,	5, 6, 27, 48, 119, 141	4, 20, 35, 48, 50, 102, 114, 131, 147	F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13
VCCIO (5.0 V or 3.3 V)	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14	32, 55, 78, 91, 102, 138, 159, 182, 193, 206	26, 55, 69, 87, 102, 131, 159, 173, 191, 206	3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192	H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2

Table 13. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	160-Pin PQFP EPF8636A *Note (1)*	192-Pin PGA EPF8636A EPF8820 EPF8820A	208-Pin RQFP EPF8636A	208-Pin RQFP EPF8820 EPF8820A	208-Pin PQFP EPF81188A *Note (1)*	225-Pin BGA EPF8820 EPF8820A
GND	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1
No Connect (N.C.)	2, 39, 82, 119	C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4, *Note (6)*	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208	–
Total User I/O Pins	114	132, *Note (7)*	132	148	144	148

Table 14. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	232-Pin PGA EPF81188 EPF81188A	240-Pin QFP EPF81188 EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500 EPF81500A
nSP *(1)*	C14	237	237	W1	304
MSEL0 *(1)*	G15	21	19	N1	26
MSEL1 *(1)*	L15	40	38	H3	51
nSTATUS *(1)*	L3	141	142	G19	178
nCONFIG *(1)*	R4	117	120	B18	152
CONF_DONE *(1)*	G3	160	161	M16	204
DCLK *(1)*	C4	184	183	U18	230
nWS	P1	133	134	F18	167
nRS	N1	137	138	G18	171
RDCLK	G2	158	159	M17	202
nCS	E2	166	167	N16	212
CS	E3	169	170	N18	215
RDYnBUSY	K2	146	147	J17	183
CLKUSR	H2	155	156	K19	199
ADD17	R15	58	56	E3	73
ADD16	T17	56	54	E2	71
ADD15	P15	54	52	F4	69
ADD14	M14	47	45	G1	60
ADD13	M15	45	43	H2	58
ADD12	M16	43	41	H1	56
ADD11	K15	36	34	J3	47
ADD10	K17	34	32	K3	45
ADD9	J14	32	30	K4	43
ADD8	J15	29	27	L1	34
ADD7	H17	27	25	L2	32
ADD6	H15	25	23	M1	30
ADD5	F16	18	16	N2	20
ADD4	F15	16	14	N3	18
ADD3	F14	14	12	N4	16
ADD2	D15	7	5	U1	8
ADD1	B17	5	3	U2	6
ADD0	C15	3	1	V1	4
DATA7	A7	205	199	W13	254
DATA6	D8	203	197	W14	252
DATA5	B7	200	196	W15	250

Table 14. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	232-Pin PGA EPF81188 EPF81188A	240-Pin QFP EPF81188 EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500 EPF81500A
DATA4	C7	198	194	W16	248
DATA3	D7	196	193	W17	246
DATA2	B5	194	190	V16	243
DATA1	A3	191	189	U16	241
DATA0	A2	189	187	V17	239
TDI *(8)*	–	–	63	B1	80
TDO *(8)*	–	–	117	C17	149
TCLK *(8)*	–	–	116	A19	148
TMS *(8)*	–	–	64	C2	81
nTRST *(8)*	–	–	115	A18	145
Dedicated Inputs	C1, C17, R1, R17	10, 51, 130, 171	8, 49, 131, 172	F1, F16, P3, P19	12, 64, 164, 217
VCCINT (5.0 V)	E4, H4, L4, P12, L14, H14, E14, R14, U1	20, 42, 64, 66, 114, 128, 150, 172, 236	18, 40, 60, 62, 91, 114, 129, 151, 173, 209	B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
VCCIO (5.0 V or 3.3 V)	N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13	19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300
GND	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 95, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291

Table 14. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	232-Pin PGA EPF81188 EPF81188A	240-Pin QFP EPF81188 EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500 EPF81500A
No Connect (N.C.)	–	61, 62, 119, 120, 181, 182, 239, 240	–	–	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins	180	180	204	204	204

Notes to Tables 12 through 14:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices* in this data book for more information.
(2) Dedicated pin (not available as a user I/O pin).
(3) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(4) Dedicated JTAG pins are available for EPF8636A devices only. No dedicated JTAG pins are available for EPF8452 and EPF8452A devices.
(5) Pin 52 is a V_{CC} pin on EPF8452 and EPF8452A devices only.
(6) These pins are No Connect pins for EPF8636A devices only.
(7) EPF8636A devices have 130 user I/O pins; EPF8820 devices have 148 user I/O pins.
(8) These pins are dedicated JTAG pins and are not available as user I/O pins.

EPF8050M

FLEX 8000M Programmable Logic Device

March 1995, ver. 3 | Data Sheet

Features

Preliminary Information

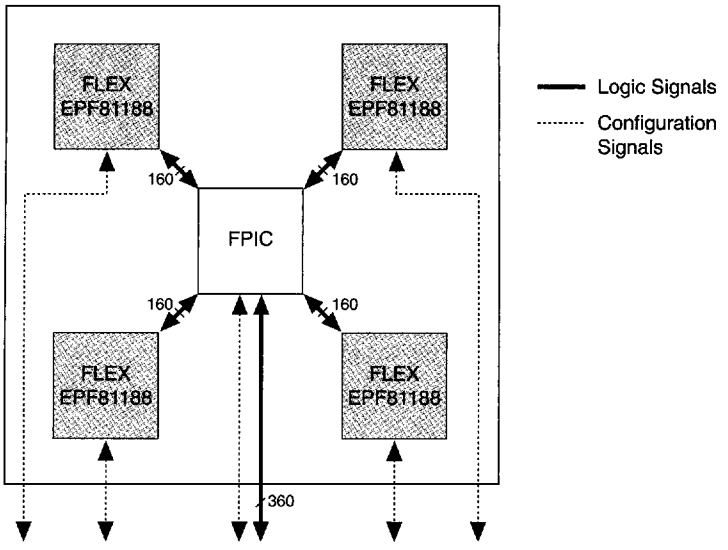
- Ideal for ASIC prototyping
  - Combination of four EPF81188 devices and one Field Programmable InterConnect (FPIC) device
  - 50,000 usable gates
  - 4,656 flipflops
  - 360 user I/O pins
  - Up to 30-MHz in-system operation
- Combination of three innovations
  - FLEX 8000 architecture
  - Programmable interconnect
  - Multi-Chip Module (MCM) packaging
- SRAM-based EPF81188 and FPIC devices
  - In-circuit reconfigurability
  - Incremental reconfiguration of each individual device within the EPF8050M
  - Low standby power
- Available in a 560-pin ceramic pin-grid array (PGA) package
  - 2.26-inch square
  - 50-mil staggered pin pitch
  - On-board decoupling capacitors (3.3 µF total)
  - Separate configuration pins for each EPF81188 and the FPIC device
- Software design support—including automatic partitioning, logic synthesis and place-and-route—with Altera's MAX+PLUS II development system for 486- and Pentium-based PCs and compatible computers, as well as for Sun SPARCstations

Architecture Description

The Altera EPF8050M device combines four EPF81188 devices and one Field Programmable Interconnect (FPIC) device to create a 50,000-gate programmable logic device (PLD). It is available in a 560-pin ceramic PGA package with 360 user I/O pins. The EPF8050M supports all FLEX 8000 architectural features. Figure 1 shows a block diagram for the EPF8050M, including connectivity between the EPF81188 devices and the I/O pins.

All logic signals for the EPF81188 devices are routed via the FPIC, providing a symmetric routing structure within the EPF8050M. The FPIC allows each EPF81188 I/O pin to be routed to any pin on any other EPF81188 device(s), or to any EPF8050M I/O pin. With this routing flexibility, the EPF8050M can be treated as four EPF81188 devices with 100% routable interconnect.

Figure 1. EPF8050M Architecture Block Diagram



A total of 1,000 pins are connected through the routing structure: 156 I/O pins and 4 dedicated inputs on each EPF81188, and 360 I/O pins on the EPF8050M. Each signal routed through the FPIC device is connected to a maximum of 5 pins (one pin for each EPF81188, and one pin for the EPF8050M).

☞ Normally, 180 I/O pins are available on each EPF81188. For the EPF8050M, 24 pins were removed from each EPF81188 to fit into the interconnect structure. MAX+PLUS II automatically limits each EPF81188 to 160 user pins (4 dedicated inputs and 156 I/O pins).

The EPF81188 and FPIC dedicated configuration pins are routed directly to dedicated EPF8050M pins. This feature allows independent configuration and testing of all active EPF8050M components, as well as in-circuit reconfiguration during system operation.

Go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for details on the FLEX 8000 architecture.

Package Description

The EPF8050M is available in a 2.26-inch square, 560-pin ceramic PGA package. The pins are spaced on 50-mil centers to allow for high pin density. For package dimensions, see "Pin-Out Information" on page 112 in this data sheet. For information on compatible zero-insertion-force (ZIF) sockets, see "Socket Information" on page 115 in this data sheet.

The EPF8050M contains six power planes that are routed to separate pins to help designers manage the power-supply switching effects in their system: V_{CCIO}, V_{CCINT}, GND_{IO}, and GND_{INT} for the EPF81188 devices, and V_{CC} and GND for the FPIC. V_{CCIO} and GND_{IO} are used for I/O switching planes; V_{CCINT} and GND_{INT} are used for internal quiet planes. If separate planes are available on the target system board, the user should connect them to the appropriate EPF8050M planes. If only two power planes are available on the target board, then all V_{CC} pins must be tied together and all GND pins must be tied together. Ten 0.33-µF decoupling capacitors are mounted on the MCM substrate (four each for the V_{CCIO}/GND_{IO} and V_{CCINT}/GND_{INT} power planes, and two for the FPIC power planes).

The EPF81188 devices are placed in ceramic ball-grid array (BGA) packages, mounted on the top of the MCM substrate, and covered with an anodized aluminum lid. The FPIC device is mounted to the bottom of the substrate with a controlled collapse chip connection (C4) or "bump-mount" process. The FPIC and passive components are covered with a ceramic lid. Standoffs on the MCM pins ensure that the bottom-side lid does not make contact with the PC board or socket.

Interconnect Description

The programmable interconnect used in the EPF8050M is a 1,000-point programmable switch. This switch provides routing between the EPF81188 devices and the EPF8050M pins.

The programmable interconnect is highly successful at routing designs and highly tolerant of internal pin changes. Whenever possible, external EPF8050M pin assignments are preserved when the design is recompiled.

The signal path through the interconnect uses pass transistors and is passive. This path is bidirectional, eliminating the need for complex logic for Output Enable and tri-state control circuitry. The resistive passive routing incurs a delay, and the worst-case delay for the interconnect (total delay for the FPIC and the EPF8050M package) is incorporated in the simulation model for the EPF8050M.

Applications

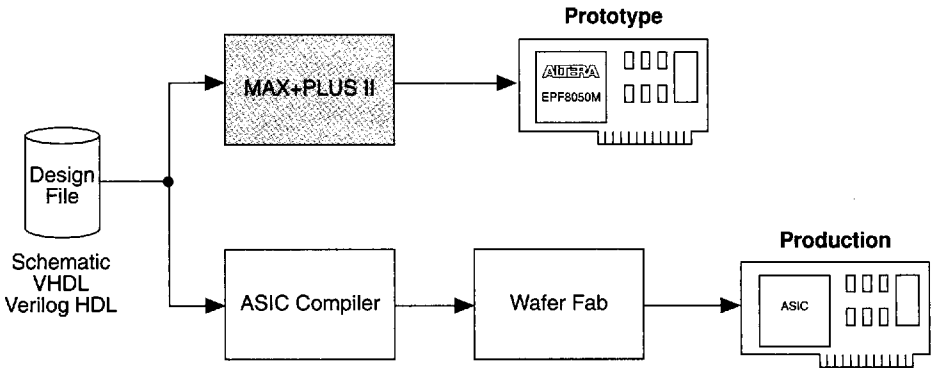
When designers use custom logic solutions such as gate arrays and ASICs to reduce cost and device count, they must ensure that designs are verified before committing them to silicon. The time required to develop and manufacture a second revision of a custom device often delays a product's market introduction.

Most designers use simulation to verify custom logic designs, analyzing a large number of test cases on a software model of the design. However, simulation is slow and typically does not exhaustively test the design. In contrast, hardware prototyping of a design is much faster than software simulation and can provide exhaustive coverage of in-circuit test conditions. Unfortunately, hardware prototyping tools are often expensive and have limited flexibility, preventing most designers from performing in-circuit prototyping of their custom logic circuits.

The EPF8050M is ideal for prototyping custom logic because it combines the best of both simulation and hardware prototyping. With MAX+PLUS II design tools, engineers can enter and simulate logic designs using either functional or timing simulation models. After simulation, the user can configure the EPF8050M and perform in-circuit hardware verification of the design.

With 50,000 usable gates, the EPF8050M is appropriate for more than 50% of today's gate array designs, and is ideally suited for gate array prototyping. The EPF8050M allows faster operating speeds than most hardware prototyping systems at a significantly reduced size and cost. It can be tested in-system, often at speeds comparable to the final system requirements. An ASIC manufactured after functional verification with an EPF8050M is more likely to function properly on first silicon. Figure 2 shows the design flow for EPF8050M and ASIC devices. The same source schematic, VHDL, or Verilog HDL file can be used for either branch of the design flow.

Figure 2. EPF8050M/ASIC Design Flow



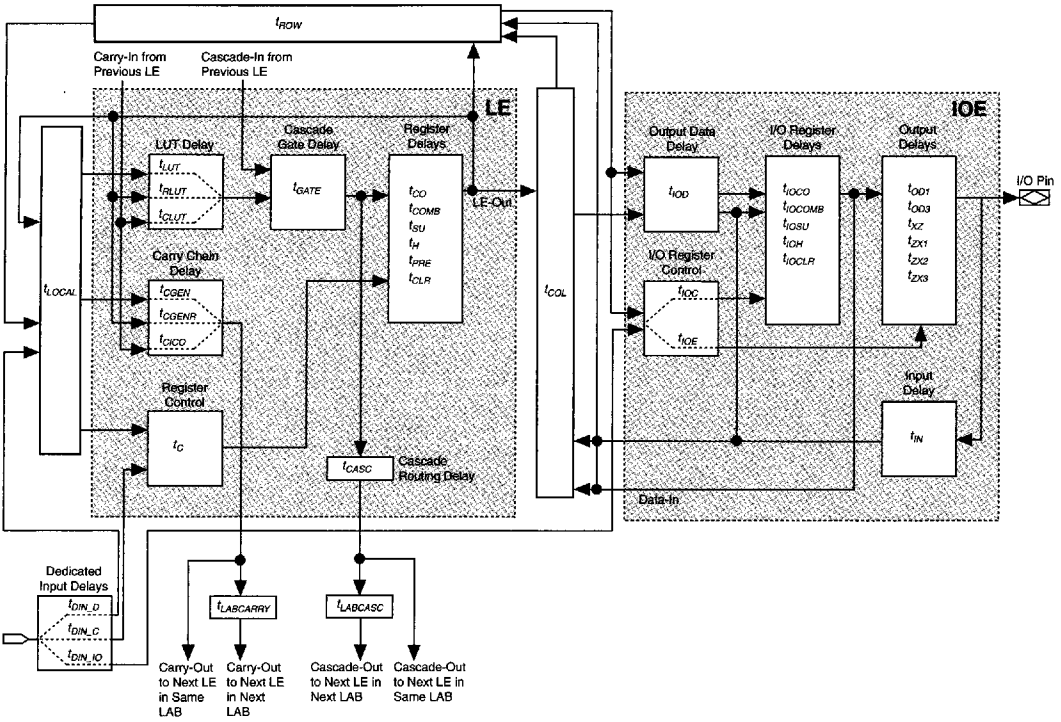
Reconfigurable hardware products (RHPs) can use the EPF8050M to pack the maximum programmable logic per square inch into advanced products that require in-circuit reconfigurability. Each EPF81188 and the FPIC can be reconfigured independently while in the target system.

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources in the EPF81188 devices ensure predictable performance and accurate simulation analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard CAE tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and system-level performance analysis.

The FLEX 8000 timing model in Figure 3 shows the delays that correspond to various paths and functions in the circuit.

Figure 3. FLEX 8000 Timing Model



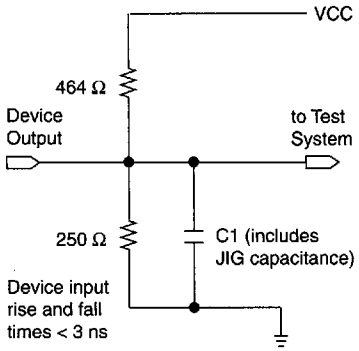
This model contains three distinct parts: the logic element (LE); the I/O element (IOE); and the interconnect, including the row and column FastTrack Interconnect, Logic Array Block (LAB) local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 3 is expressed as a worst-case value in the "EPF8050M Internal Timing Characteristics" tables that begin on page 102 in this data sheet. Delays through the interconnect and the MCM interconnect are included in the input and output delays. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate EPF8050M device performance. Timing simulation or timing analysis after compilation is required to determine final worst-case performance.

Generic Testing

The EPF8050M is fully tested and guaranteed. All EPF81188 devices and the FPIC device are fully tested before and after they are mounted into the EPF8050M package. This testing procedure ensures that each active component is tested individually, and as part of the entire system. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for the EPF81188 devices are made under conditions equivalent to those shown in Figure 4. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 4. EPF8050M AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND *Note (1)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–10	90	° C
T_{AMB}	Ambient temperature	Under bias	–10	90	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	With respect to GND	4.75	5.25	V
V_{CCIO}	Supply voltage for output buffers		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level TTL output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (3)*		4		mA

EPF8050M Internal Timing Characteristics *Note (4)*

EPF8050M I/O Element Timing Parameters			EPF8050M-3		
Symbol	Parameter	Conditions	Min	Max	Unit
t_{IOD}	IOE register data delay			2.0	ns
t_{IOC}	IOE register control signal delay			2.0	ns
t_{IOE}	Output enable delay			2.0	ns
t_{IOCO}	IOE register clock-to-output delay			1.0	ns
t_{IOCOMB}	IOE combinatorial delay			0.0	ns
t_{IOSU}	IOE register setup time before clock		2.0		ns
t_{IOH}	IOE register hold time after clock		0.0		ns
t_{IOCLR}	IOE register clear delay			1.2	ns
t_{IN}	Input pad and buffer delay			8.8	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	*Note (5)*		8.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V	*Note (5)*		12.0	ns
t_{XZ}	Output buffer disable delay			8.0	ns
t_{ZX}	Output buffer enable delay			8.0	ns

EPF8050M Logic Element Timing Parameters			EPF8050M-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{LUT}	LUT delay for data-in			5.1	ns
t_{CLUT}	LUT delay for carry-in			1.0	ns
t_{RLUT}	LUT delay for LE register feedback			3.4	ns
t_{GATE}	Cascade gate delay			0.0	ns
t_{CASC}	Cascade chain routing delay			2.0	ns
t_{CICO}	Carry-in to carry-out delay			1.1	ns
t_{CGEN}	Data-in to carry-out delay			1.4	ns
t_{CGENR}	LE register feedback to carry-out delay			2.4	ns
t_{C}	LE register control signal delay			3.1	ns
t_{CH}	Clock high time		4.3		ns
t_{CL}	Clock low time		4.3		ns
t_{CO}	LE register clock-to-output delay			0.9	ns
t_{COMB}	Combinatorial delay			0.9	ns
t_{SU}	LE register setup time before clock		1.7		ns
t_{H}	LE register hold time after clock		4.0		ns
t_{PRE}	LE register preset delay			1.2	ns
t_{CLR}	LE register clear delay			1.2	ns

EPF8050M Interconnect Timing Parameters			EPF8050M-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade delay between LEs in different LABs			0.9	ns
$t_{LABCARRY}$	Carry delay between LEs in different LABs			0.6	ns
t_{LOCAL}	LAB local interconnect delay			1.0	ns
t_{ROW}	Row interconnect routing delay	*Note (6)*		5.0	ns
t_{COL}	Column interconnect routing delay			3.0	ns
t_{DIN_C}	Dedicated input to LE control delay			13.0	ns
t_{DIN_D}	Dedicated input to LE data delay	*Note (6)*		15.0	ns
t_{DIN_IO}	Dedicated input to IOE control delay			15.0	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Operating conditions: $V_{CC} = 5.0\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.

(3) Unconfigured devices draw approximately 1 A.

(4) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) Operating conditions: $V_{CCIO} = 5.0\ V \pm 5\%$ for commercial use.

(6) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

Software Support

The EPF8050M device is supported by the Altera MAX+PLUS II development system. Designing with the EPF8050M requires the EPF8050M migration product (PLSM-8KM) and a MAX+PLUS II system that supports FLEX 8000 devices and multi-device partitioning.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

Go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

MAX+PLUS II fits cleanly into an ASIC design flow. MAX+PLUS II and the target ASIC silicon compiler can share the same source file, minimizing the time required for design entry and processing. Designs entered with a specific ASIC library do not need to be modified because they can be directly mapped into MAX+PLUS II using Library Mapping Files (**.lmf**).

Go to *ApplicationBrief 96* (*Generating Library Mapping Files*) for more information.

During design processing, MAX+PLUS II automatically partitions an EPF8050M design into the four EPF81188 devices. Functional hardware emulation of the ASIC design can then be performed with the EPF8050M. Once the design is validated, the source file can be targeted at an ASIC technology library with a high level of confidence that the first silicon will work as expected.

Device Configuration

The FLEX 8000 architecture uses SRAM cells to store the configuration data for the device. These SRAM cells must be loaded each time the circuit powers up and begins operation. The process of physically loading data into the device is called *configuration*. After configuration, the device resets its registers, enables its I/O pins, and begins operation as a logic device. This reset operation is called *initialization*. Together, the configuration and initialization processes are called *command mode*; normal in-circuit device operation is called *user mode*.

The EPF8050M contains five SRAM-based devices, each of which must be loaded with configuration data. The EPF8050M supports both active and passive configuration schemes. In an active scheme, the devices receive their data from a parallel EPROM. In a passive scheme, an external host provides the data and Clock cycles to the EPF81188 and FPIC devices.

The configuration data for the EPF81188 devices is approximately 180K bits long; the configuration data for the FPIC is approximately 64K bits long. Since configuration data for the FPIC has a shorter bitstream than for the EPF81188 devices, the FPIC data is pre-padded with 1's so that all five devices complete configuration simultaneously.

Go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* for complete information on configuring FLEX 8000 devices. Go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* for more information on FLEX 8000 architecture.

Active Configuration

An active configuration circuit uses a stand-alone configuration controller (typically a small PLD) to manage the configuration process and a parallel EPROM to store the configuration data. The serial configuration data for each of the EPF81188 devices and the FPIC device in the EPF8050M are stored in the bits in the parallel EPROM's 8-bit data word. The serial configuration data used to program the EPROM is stored in a Hexadecimal (Intel-format) File (**.hex**) that is created by the MCMFIT software. The first 6 bits in each EPROM word contain configuration data, as shown in Table 1.

Table 1. Configuration Bit Patterns

Data Bit	EPF8050M Destination		
	Device	Pin Name	Pin Number
Bit 0	FPIC	DIN	BC35
Bit 1	EPF81188 #1	DATA0	B4
Bit 2	EPF81188 #2	DATA0	D42
Bit 3	EPF81188 #3	DATA0	BB40
Bit 4	EPF81188 #4	DATA0	AY2
Bit 5	FPIC	PROGRAM	BC37
Bits 6 & 7	Unused	–	–

The multi-device active serial bit-slice (MD-ASB) configuration circuit is shown in Figure 5. In this scheme, one of the EPF81188 devices (EPF81188 #1 in Figure 5) is configured in the active serial (AS) configuration scheme. This device clocks the circuit and controls the configuration process. An EPM7032 support PLD controls the configuration process, generating the addresses for the parallel EPROM. The remaining EPF81188 devices and the FPIC device are configured in the passive serial (PS) configuration scheme, and latch the configuration data from the parallel EPROM on the rising edge of the active EPF81188 device's Clock signal.

Figure 5. EPF8050M Multi-Device Active Serial Bit-Slice (MD-ASB) Configuration Circuit

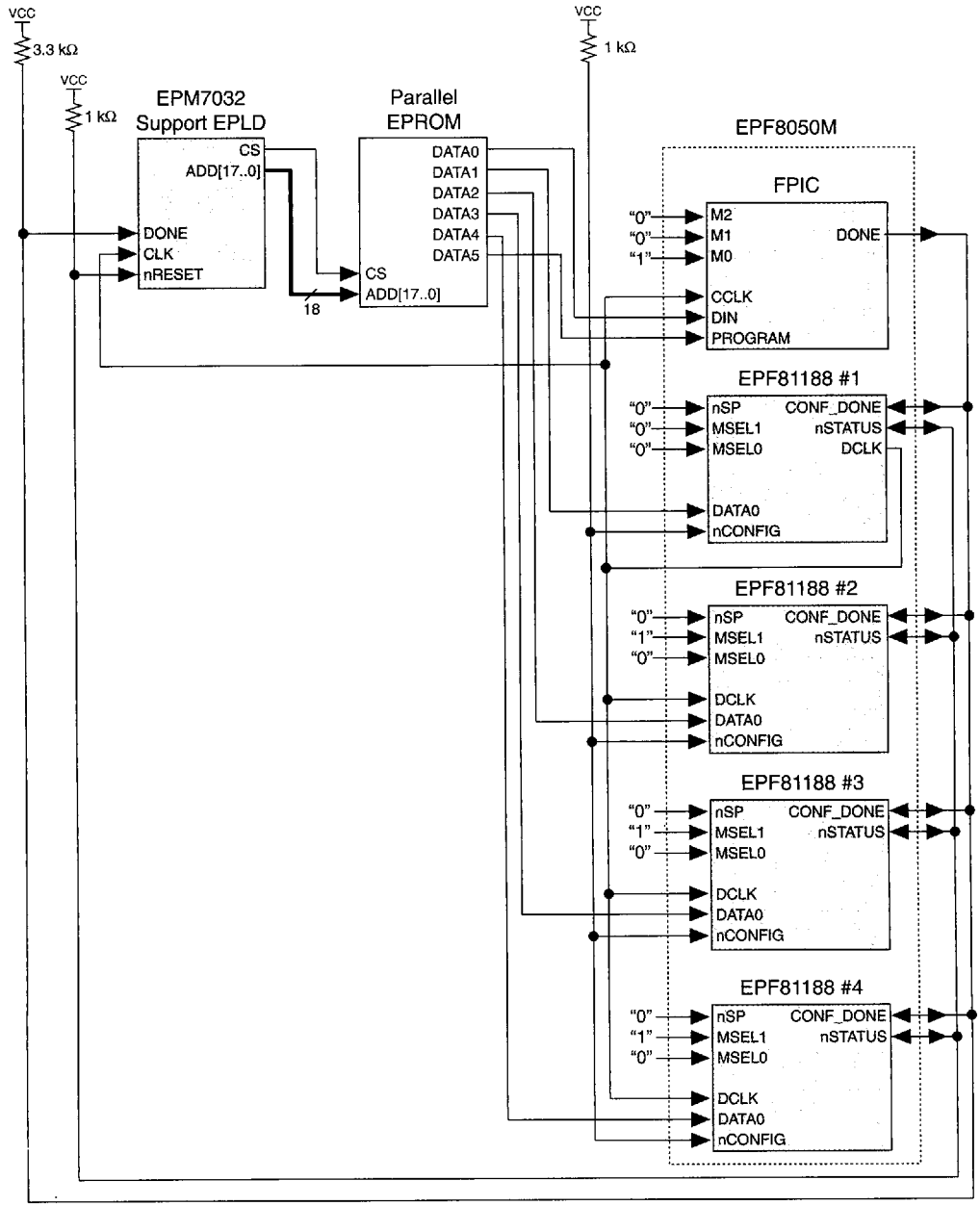


Figure 6 shows an AHDL Text Design File (.tdf) that implements the functions required in the EPM7032 support device.

Figure 6. AHDL Text Design File for EPM7032 Support Device (ascontrl.tdf)

```
TITLE "Active Serial 7032 Controller for EPF8050M Designs";
SUBDESIGN ascontrl
(
      clk, done, nreset   : INPUT;
      cs, add[17..0]      : OUTPUT;
)
VARIABLE
      count[17..0] : DFF;
BEGIN
      count[].clk  = global(clk);
      count[].clrn = nreset;
      count[].d    = count[].q + 1;
      add[]        = count[];
      cs           = !done;
END;
```

If one of the EPF81188 devices encounters an error during configuration, it pulls the nSTATUS net low. When the nRESET input to the EPM7032 is pulled low, the address counter in the EPM7032 is reset. When nRESET pulls high again, configuration restarts. Since all nSTATUS pins are tied together, a configuration error on any of the EPF81188 devices causes the EPF8050M to reset. Since the FPIC does not have a "configuration error" output, it is not part of the nSTATUS net. The CONF_DONE and DONE pins are tied together and pulled to V_{CC} via a 3.3-kΩ resistor. If the DONE net is high, configuration is complete and the EPF8050M is in user mode.

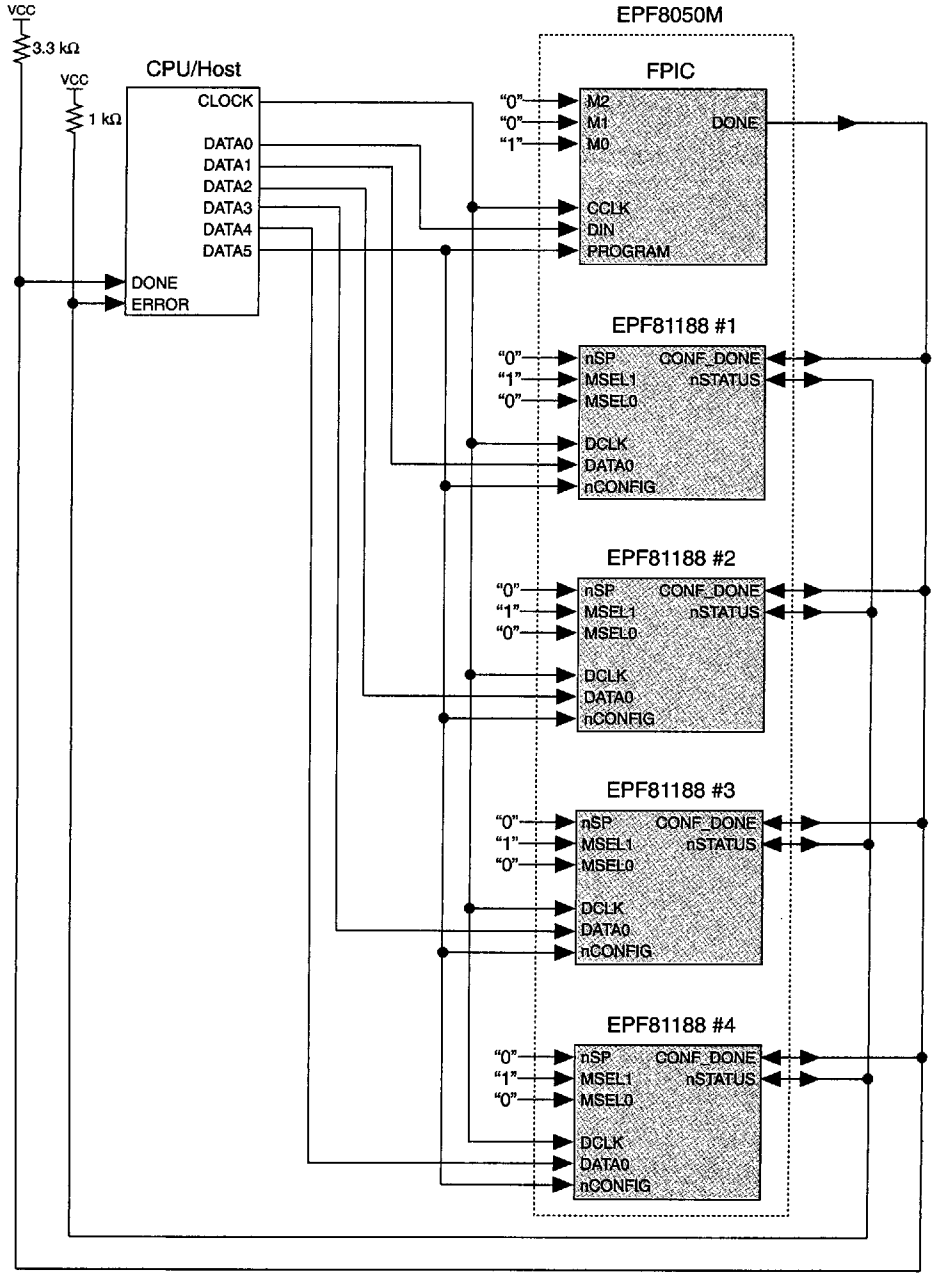
Passive Configuration

In systems with an intelligent host, configuration data is stored in memory or on a hard disk, and is loaded into the devices under control of the host. The individual devices in the EPF8050M can be configured simultaneously or individually, thereby allowing in-circuit reconfiguration. The intelligent host generates the control signals necessary to initiate and complete configuration, typically using a data port on the host and a parallel data path. The serial configuration data for each of the five configurable devices in the EPF8050M are stored in an ASCII-format Tabular Text File (**.ttf**). The first 6 bits in each byte of the TTF contain configuration data, as shown in Table 1.

Figure 7 shows the multi-device passive serial bit-slice (MD-PSB) configuration scheme. All four EPF81188 devices and the FPIC are configured with the PS configuration scheme. The intelligent host provides the configuration Clock.

The nSTATUS pins are pulled low by the EPF81188 devices during the first 64 configuration bits when the EPF8050M is reset. After the 64th bit, the nSTATUS pins are released and pulled to V_{CC} via a pull-up register. If one of the EPF81188 devices encounters an error after the 64th Clock cycle, it pulls the nSTATUS net low again. When the intelligent host detects a low level on the nSTATUS net during configuration, it restarts configuration. Since all nSTATUS pins are tied together, a configuration error on any of the EPF81188 devices causes the EPF8050M to reset. Since the FPIC does not have a "configuration error" output, it is not part of the nSTATUS net. The CONF_DONE and DONE pins are tied together and pulled to V_{CC} via a 3.3-kΩ resistor. A high level on the DONE net indicates that the configuration data has been successfully loaded. The intelligent host must then provide 10 more Clock cycles to initialize the EPF8050M.

Figure 7. EPF8050M Multi-Device Passive Serial Bit-Slice (MD-PSB) Configuration Circuit



Configuration Pins

The configuration scheme for the EPF81188 devices is selected with the nSP, MSEL1, and MSEL0 configuration pins; the configuration scheme for the FPIC is selected with the M2, M1, and M0 configuration pins. Table 2 shows valid selection patterns for the two configuration schemes for the individual EPF81188 and FPIC devices.

Table 2. Valid Selection Patterns for EPF81188 & FPIC Devices

Configuration Scheme	EPF81188 #1 nSP:MSEL1:MSEL0	EPF81188 #2, #3, #4 nSP:MSEL1:MSEL0	FPIC M2:M1:M0
MD-PSB	010	010	001
MD-ASB	000	010	001

nCONFIG & PROGRAM Pins

The nCONFIG (EPF81188) and PROGRAM (FPIC) input pins initiate configuration cycles. A high-to-low transition resets the device; a subsequent low-to-high transition starts the configuration process.

The FLEX 8000 architecture allows the user to tie the nCONFIG pin to V_{CC}, causing the EPF81188 devices to be configured immediately upon power-up. In contrast, a high-low-high pulse is required on the FPIC's PROGRAM pin for every configuration cycle.

nSTATUS Pin

The EPF81188 bidirectional open-drain nSTATUS pins are all connected to the nSTATUS net. The nSTATUS net is pulled to V_{CC} via a 1-kΩ resistor. If an error occurs during configuration, the device that detects the error pulls and holds the nSTATUS net low.

CONF_DONE & DONE Pins

The CONF_DONE (EPF81188) and DONE (FPIC) pins are open-drain "configuration complete" indicators. These pins are tied together and pulled to V_{CC} via a 3.3-kΩ resistor. After the configuration data has been loaded, each device releases its CONF_DONE or DONE pin. Once all five devices are completely configured, the DONE net is pulled to V_{CC}, indicating that the EPF8050M is in user mode. Holding an EPF81188 CONF_DONE pin low prevents the EPF81188 from entering the user mode. In contrast, holding the FPIC's DONE pin low does not prevent the FPIC from entering user mode.

Configuration File Formats

In active configuration schemes, the configuration data for all five devices (four EPF81188 devices and one FPIC device) is combined into a Hexadecimal (Intel-format) File (**.hex**) for device programming. This conversion is automatically performed by the Altera-provided MCMFIT software. The Hex File contains the address information necessary to program a standard 256K × 8 bit parallel EPROM with the configuration data.

In passive configuration schemes, the MCMFIT software automatically converts the configuration data into a Tabular Text File (**.ttf**), an ASCII text file that contains decimal values for each byte. The intelligent host reads an ASCII word from the TTF, converts it to a binary pattern, and provides the six low-order bits to the corresponding devices in the EPF8050M.

Pin-Out Information

Tables 3, 4, and 5 show the device pin-outs for EPF8050M configuration pins, power pins, and I/O pins, respectively.

Table 3. EPF8050M Configuration Pin-Outs

Pin Name	FPIC	EPF81188 #1	EPF81188 #2	EPF81188 #3	EPF81188 #4
nSP	–	D4	D40	AY40	AY4
MSEL0	–	A1	A43	BC43	BC1
MSEL1	–	A3	C43	BC41	BA1
nCONFIG	–	C1	A41	BA43	BC3
DCLK	–	C5	B38	AV42	AW5
nSTATUS	–	B2	B42	BB42	BB2
CONF_DONE	–	A5	E43	BC39	AW1
DATA0	–	B4	D42	BB40	AY2
M0	AW3	–	–	–	–
M1	AV2	–	–	–	–
M2	AU1	–	–	–	–
PROGRAM	BC37	–	–	–	–
DIN	BC35	–	–	–	–
CCLK	BC7	–	–	–	–
DONE	AW41	–	–	–	–

Table 4. EPF8050M VCC and GND Pin-Outs

Pin Name	EPF8050M Pin-Outs
VCCIO	E37, F14, F8, F20, F26, F32, H16, H38, J39, K6, K42, P38, T6, Y38, AB6, AF38, AH6, AM38, AT16, AU7, AU37, AV14, AV20, AV26, AV32, AV40, BA37, BB18, BB38
GNDIO	B18, C39, E41, G9, G15, G17, G21, G27, G33, J37, L7, N37, U7, W37, AC7, AE37, AJ5, AJ7, AL37, AT8, AT18, AT36, AU13, AU19, AU25, AU31, AU41, AW37, BA39
VCCINT	A39, B10, B16, B22, B28, B36, C3, C41, E1, G5, H12, J43, M2, M42, T42, V2, AB42, AD2, AH42, AK2, AP42, AT12, AU5, AW39, AW43, BA3, BA41, BB14, BB20, BB26, BB32, BC5
GNDINT	B40, C11, C17, C23, C29, C37, D2, H6, H14, H42, L43, N3, R41, W3, AA41, AE3, AG41, AL3, AN41, AT14, AV6, AY38, AY42, BA13, BA19, BA25, BA31, BB4
VCCFPIC	B6, B14, B20, B26, B32, G1, G43, P2, P42, Y2, Y42, AF2, AF42, AM2, AM42, AY36, BB6, BB16, BB22, BB28
GNDFPIC	A7, C7, C15, C21, C27, C33, F42, H2, N41, R3, W41, AA3, AE41, AG3, AL41, AN3, AW35, BA5, BA15, BA21, BA27
No Connect (N.C.)	AU43, BC9

Table 5. EPF8050M I/O Pins

A9	D26	F34	K2	T8	AB8	AH8	AP8	AU33	AY18
A11	D28	F36	K4	T36	AB36	AH36	AP36	AU35	AY20
A13	D30	F38	K8	T38	AB38	AH38	AP38	AU39	AY22
A15	D32	F40	K36	T40	AB40	AH40	AP40	AV4	AY24
A17	D34	G3	K38	U1	AC1	AJ1	AR1	AV8	AY26
A19	D36	G7	K40	U3	AC3	AJ3	AR3	AV10	AY28
A21	D38	G11	L1	U5	AC5	AJ37	AR5	AV12	AY30
A23	E3	G13	L3	U37	AC37	AJ39	AR7	AV16	AY32
A25	E5	G19	L5	U39	AC39	AJ41	AR37	AV18	AY34
A27	E7	G23	L37	U41	AC41	AJ43	AR39	AV22	BA7
A29	E9	G25	L39	U43	AC43	AK4	AR41	AV24	BA9
A31	E11	G29	L41	V4	AD4	AK6	AR43	AV28	BA11
A33	E13	G31	M4	V6	AD6	AK8	AT2	AV30	BA17
A35	E15	G35	M6	V8	AD8	AK36	AT4	AV34	BA23
A37	E17	G37	M8	V36	AD36	AK38	AT6	AV36	BA29
B8	E19	G39	M36	V38	AD38	AK40	AT10	AV38	BA33
B12	E21	G41	M38	V40	AD40	AK42	AT20	AW7	BA35
B24	E23	H4	M40	V42	AD42	AL1	AT22	AW9	BB8
B30	E25	H8	N1	W1	AE1	AL5	AT24	AW11	BB10
B34	E27	H10	N5	W5	AE5	AL7	AT26	AW13	BB12
C9	E29	H18	N7	W7	AE7	AL39	AT28	AW15	BB24
C13	E31	H20	N39	W39	AE39	AL43	AT30	AW17	BB30
C19	E33	H22	N43	W43	AE43	AM4	AT32	AW19	BB34
C25	E35	H24	P4	Y4	AF4	AM6	AT34	AW21	BB36
C31	E39	H26	P6	Y6	AF6	AM8	AT38	AW23	BC11
C35	F2	H28	P8	Y8	AF8	AM36	AT40	AW25	BC13
D6	F4	H30	P36	Y36	AF36	AM40	AT42	AW27	BC15
D8	F6	H32	P40	Y40	AF40	AN1	AU3	AW29	BC17
D10	F10	H34	R1	AA1	AG1	AN5	AU9	AW31	BC19
D12	F12	H36	R5	AA5	AG5	AN7	AU11	AW33	BC21
D14	F16	H40	R7	AA7	AG7	AN37	AU15	AY6	BC23
D16	F18	J1	R37	AA37	AG37	AN39	AU17	AY8	BC25
D18	F22	J3	R39	AA39	AG39	AN43	AU21	AY10	BC27
D20	F24	J5	R43	AA43	AG43	AP2	AU23	AY12	BC29
D22	F28	J7	T2	AB2	AH2	AP4	AU27	AY14	BC31
D24	F30	J41	T4	AB4	AH4	AP6	AU29	AY16	BC33

Socket Information

Zero-insertion-force sockets are available from AMP:

25 × 25 Socket Assembly (Proposal Number: 94-3409-025-002)