

## 74LVT32374 • 74LVTH32374

### Low Voltage 32-Bit D-Type Flip-Flop with 3-STATE Outputs

#### General Description

The LVT32374 and LVTH32374 contain thirty-two non-inverting D-type flip-flops with 3-STATE outputs and are intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ( $\overline{OE}$ ) are common to each byte and can be shorted together for full 32-bit operation.

The LVTH32374 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These flip-flops are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT32374 and LVTH32374 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH32374)
- Also available without bushold feature (74LVT32374)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- ESD performance:  
Human-body model > 2000V  
Machine model > 200V  
Charged-device model > 1000V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

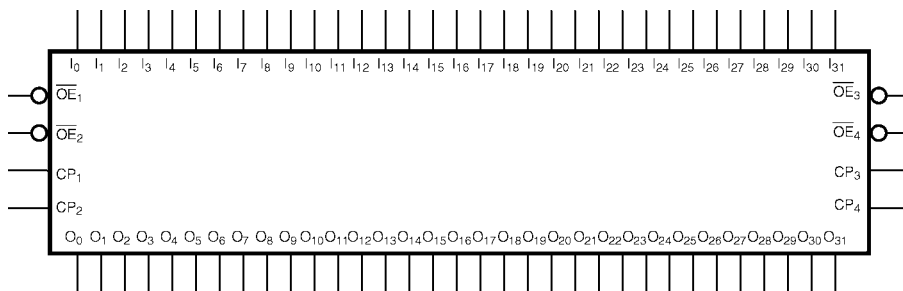
#### Ordering Code:

Order Number	Package Number	Package Description
74LVT32374G (Note 1)(Note 2)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH32374G (Note 1)(Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

**Note 1:** Ordering code "G" indicates Trays.

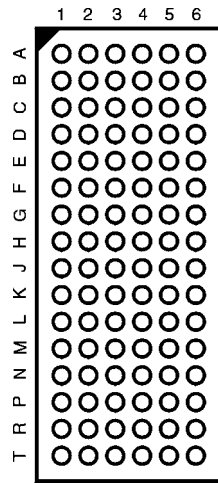
**Note 2:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol



74LVT32374 • 74LVTH32374 Low Voltage 32-Bit D-Type Flip-Flop with 3-STATE Outputs

### Connection Diagram



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$CP_n$	Clock Pulse Input
$I_0-I_{31}$	Inputs
$O_0-O_{31}$	3-STATE Outputs

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_1$	$O_0$	$\overline{OE}_1$	$CP_1$	$I_0$	$I_1$
<b>B</b>	$O_3$	$O_2$	GND	GND	$I_2$	$I_3$
<b>C</b>	$O_5$	$O_4$	$V_{CC1}$	$V_{CC1}$	$I_4$	$I_5$
<b>D</b>	$O_7$	$O_6$	GND	GND	$I_6$	$I_7$
<b>E</b>	$O_9$	$O_8$	GND	GND	$I_8$	$I_9$
<b>F</b>	$O_{11}$	$O_{10}$	$V_{CC1}$	$V_{CC1}$	$I_{10}$	$I_{11}$
<b>G</b>	$O_{13}$	$O_{12}$	GND	GND	$I_{12}$	$I_{13}$
<b>H</b>	$O_{14}$	$O_{15}$	$\overline{OE}_2$	$CP_2$	$I_{15}$	$I_{14}$
<b>J</b>	$O_{17}$	$O_{16}$	$\overline{OE}_3$	$CP_3$	$I_{16}$	$I_{17}$
<b>K</b>	$O_{19}$	$O_{18}$	GND	GND	$I_{18}$	$I_{19}$
<b>L</b>	$O_{21}$	$O_{20}$	$V_{CC2}$	$V_{CC2}$	$I_{20}$	$I_{21}$
<b>M</b>	$O_{23}$	$O_{22}$	GND	GND	$I_{22}$	$I_{23}$
<b>N</b>	$O_{25}$	$O_{24}$	GND	GND	$I_{24}$	$I_{25}$
<b>P</b>	$O_{27}$	$O_{26}$	$V_{CC2}$	$V_{CC2}$	$I_{26}$	$I_{27}$
<b>R</b>	$O_{29}$	$O_{28}$	GND	GND	$I_{28}$	$I_{29}$
<b>T</b>	$O_{30}$	$O_{31}$	$\overline{OE}_4$	$CP_4$	$I_{31}$	$I_{30}$

### Functional Description

The LVT32374 and LVTH32374 consist of thirty-two edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 32-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock ( $CP_n$ ) transition. With the Output Enable ( $\overline{OE}_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}_n$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}_n$  input does not affect the state of the flip-flops.

### Truth Tables

Inputs			Outputs
$CP_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

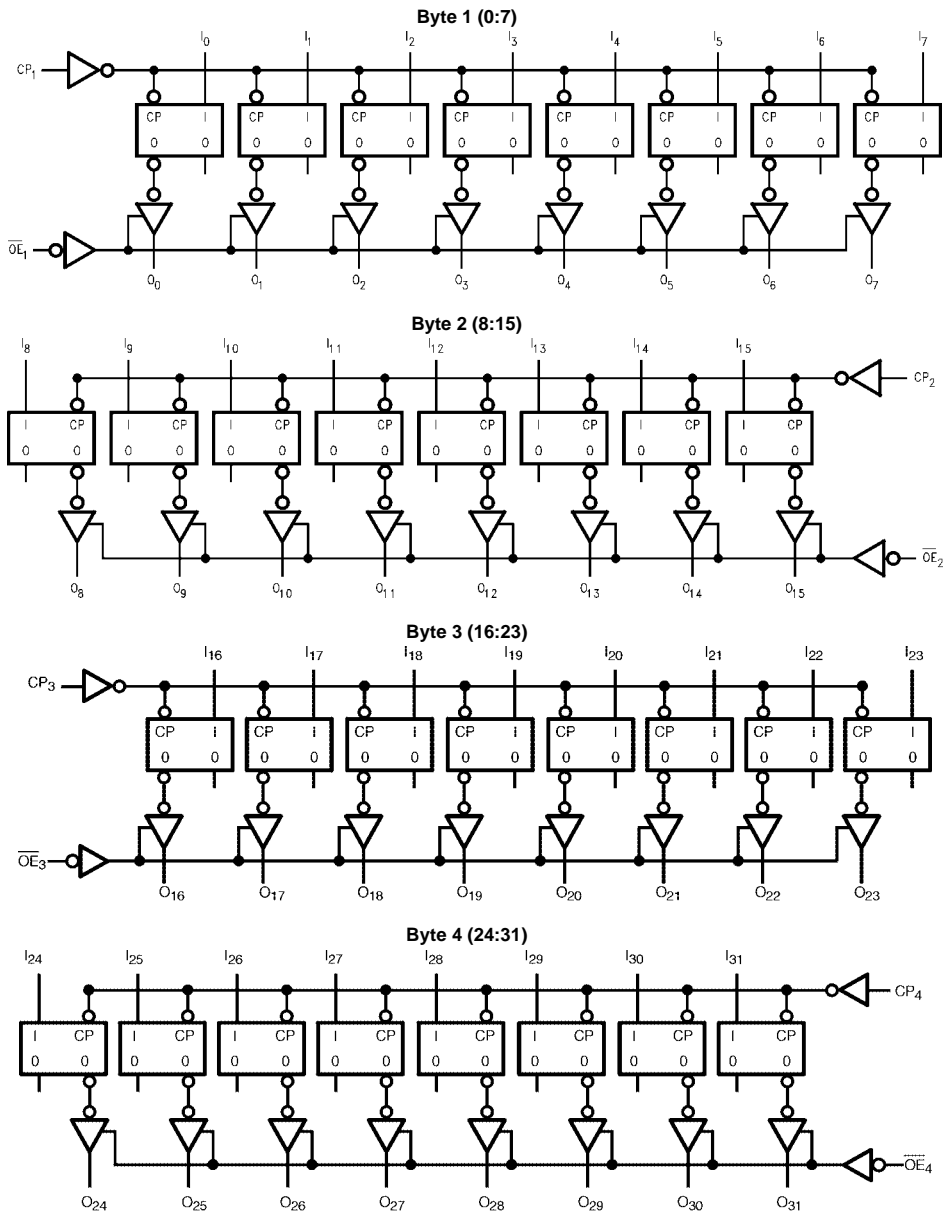
Inputs			Outputs
$CP_3$	$\overline{OE}_3$	$I_{16}-I_{23}$	$O_{16}-O_{23}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_4$	$\overline{OE}_4$	$I_{24}-I_{31}$	$O_{24}-O_{31}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

Z = HIGH Impedance  
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW of CP

Logic Diagrams



$V_{CC1}$  is associated with Bytes 1 and 2.

$V_{CC2}$  is associated with Bytes 3 and 4.

**Note:** Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 3)

Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +4.6		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
$I_{IK}$	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
$I_O$	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 64$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 128$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}\text{C}$

**Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	HIGH Level Output Current		-32	mA
$I_{OL}$	LOW Level Output Current		64	mA
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8\text{V}-2.0\text{V}$ , $V_{CC} = 3.0\text{V}$	0	10	ns/V

**Note 3:** Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 4:**  $I_O$  Absolute Maximum Rating must be observed.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Units	Conditions	
			Min	Max			
$V_{IK}$	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18 \text{ mA}$	
$V_{IH}$	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1\text{V}$ or $V_O \geq V_{CC} - 0.1\text{V}$	
$V_{IL}$	Input LOW Voltage	2.7-3.6		0.8	V		
$V_{OH}$	Output HIGH Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu\text{A}$	
		2.7	2.4			$I_{OH} = -8 \text{ mA}$	
		3.0	2.0			$I_{OH} = -32 \text{ mA}$	
$V_{OL}$	Output LOW Voltage	2.7		0.2	V	$I_{OL} = 100 \mu\text{A}$	
		2.7		0.5		$I_{OL} = 24 \text{ mA}$	
		3.0		0.4		$I_{OL} = 16 \text{ mA}$	
		3.0		0.5		$I_{OL} = 32 \text{ mA}$	
		3.0		0.55		$I_{OL} = 64 \text{ mA}$	
$I_{I(\text{HOLD})}$ (Note 5)	Bushold Input Minimum Drive	3.0	75		$\mu\text{A}$	$V_I = 0.8\text{V}$	
			-75			$V_I = 2.0\text{V}$	
$I_{I(\text{OD})}$ (Note 5)	Bushold Input Over-Drive Current to Change State	3.0	500		$\mu\text{A}$	(Note 6)	
			-500			(Note 7)	
$I_I$	Input Current	3.6		10	$\mu\text{A}$	$V_I = 5.5\text{V}$	
		Control Pins	3.6			$\pm 1$	$V_I = 0\text{V}$ or $V_{CC}$
			Data Pins	3.6			-5
				1		$V_I = V_{CC}$	
$I_{OFF}$	Power Off Leakage Current	0		$\pm 100$	$\mu\text{A}$	$0\text{V} \leq V_I$ or $V_O \leq 5.5\text{V}$	
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current	0-1.5V		$\pm 100$	$\mu\text{A}$	$V_O = 0.5\text{V}$ to $3.0\text{V}$ $V_I = \text{GND}$ or $V_{CC}$	
$I_{OZL}$	3-STATE Output Leakage Current	3.6		-5	$\mu\text{A}$	$V_O = 0.5\text{V}$	
$I_{OZH}$	3-STATE Output Leakage Current	3.6		5	$\mu\text{A}$	$V_O = 3.0\text{V}$	
$I_{OZH+}$	3-STATE Output Leakage Current	3.6		10	$\mu\text{A}$	$V_{CC} < V_O \leq 5.5\text{V}$	

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Max		
I <sub>CCH</sub>	Power Supply Current (V <sub>CC1</sub> or V <sub>CC2</sub> )	3.6		0.19	mA	Outputs HIGH
I <sub>CCL</sub>	Power Supply Current (V <sub>CC1</sub> or V <sub>CC2</sub> )	3.6		5	mA	Outputs LOW
I <sub>CCZ</sub>	Power Supply Current (V <sub>CC1</sub> or V <sub>CC2</sub> )	3.6		0.19	mA	Outputs Disabled
I <sub>CCZ+</sub>	Power Supply Current (V <sub>CC1</sub> or V <sub>CC2</sub> )	3.6		0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (V <sub>CC1</sub> or V <sub>CC2</sub> ) (Note 8)	3.6		0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND

**Note 5:** Applies to bushold version only (74LVTH32374).

**Note 6:** An external driver must sink at least the specified current to switch from LOW-to-HIGH.

**Note 7:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 8:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

**Dynamic Switching Characteristics** (Note 9)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 10)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 10)

**Note 9:** Characterized in SSOP package. Guaranteed parameter, but not tested.

**Note 10:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω				Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		
		Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	160		160		MHz
t <sub>PHL</sub>	Propagation Delay	1.9	4.3	1.9	4.6	ns
t <sub>PLH</sub>	CP to O <sub>n</sub>	1.6	4.5	1.6	5.2	ns
t <sub>PZL</sub>	Output Enable Time	1.3	4.4	1.3	5.0	ns
t <sub>PZH</sub>		1.0	4.5	1.0	5.4	ns
t <sub>PLZ</sub>	Output Disable Time	1.5	4.6	1.5	4.8	ns
t <sub>PHZ</sub>		2.0	5.0	2.0	5.4	ns
t <sub>S</sub>	Setup Time	1.8		2.0		ns
t <sub>H</sub>	Hold Time	0.8		0.1		ns
t <sub>W</sub>	Pulse Width	3.0		3.0		ns

**Capacitance** (Note 11)

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN, V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.0V, V <sub>O</sub> = 0V or V <sub>CC</sub>	8	pF

**Note 11:** Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

