



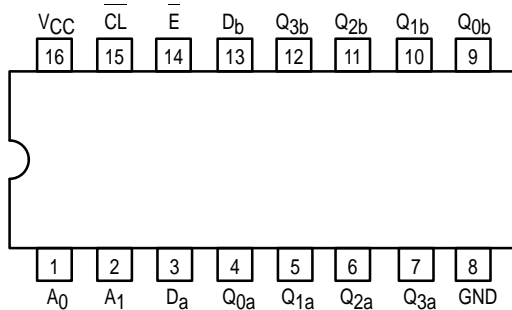
# DUAL 4-BIT ADDRESSABLE LATCH

The SN54/74LS256 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs ( $A_0, A_1$ ), an active LOW Enable input ( $\bar{E}$ ) and an active LOW Clear input ( $\bar{CL}$ ). Each latch has a Data input ( $D$ ) and four outputs ( $Q_0-Q_3$ ).

When the Enable ( $\bar{E}$ ) is HIGH and the Clear input ( $\bar{CL}$ ) is LOW, all outputs ( $Q_0-Q_3$ ) are LOW. Dual 4-channel demultiplexing occurs when the ( $\bar{CL}$ ) and  $\bar{E}$  are both LOW. When  $\bar{CL}$  is HIGH and  $\bar{E}$  is LOW, the selected output ( $Q_0-Q_3$ ), determined by the Address inputs, follows  $D$ . When the  $\bar{E}$  goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ( $\bar{E}=\text{LOW}, \bar{CL}=\text{HIGH}$ ), changing more than one bit of the Address ( $A_0, A_1$ ) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ( $\bar{E}=\bar{CL}=\text{HIGH}$ ).

- Serial-to-Parallel Capability
- Output From Each Storage Bit Available
- Random (Addressable) Data Entry
- Easily Expandable
- Active Low Common Clear
- Input Clamp Diodes Limit High Speed Termination Effects

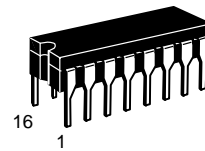
### CONNECTION DIAGRAM DIP (TOP VIEW)



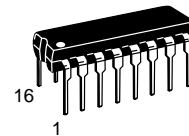
NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

## SN54/74LS256

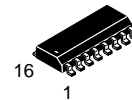
### DUAL 4-BIT ADDRESSABLE LATCH LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08



**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

SN54LSXXXJ Ceramic  
SN74LSXXXN Plastic  
SN74LSXXXD SOIC

### PIN NAMES

$A_0, A_1$  Address Inputs  
 $\bar{D}_a, \bar{D}_b$  Data Inputs  
 $\bar{E}$  Enable Input (Active LOW)  
 $\bar{CL}$  Clear Input (Active LOW)  
 $Q_{0a}-Q_{3a}$   
 $Q_{0b}-Q_{3b}$  Parallel Latch Outputs (Note b)

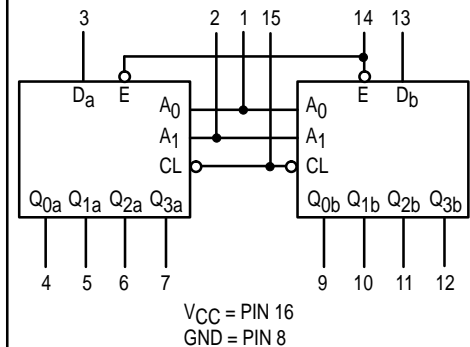
### NOTES:

- a) 1 TTL Unit Load (U.L.) = 40  $\mu\text{A}$  HIGH/1.6 mA LOW.  
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

### LOADING (Note a)

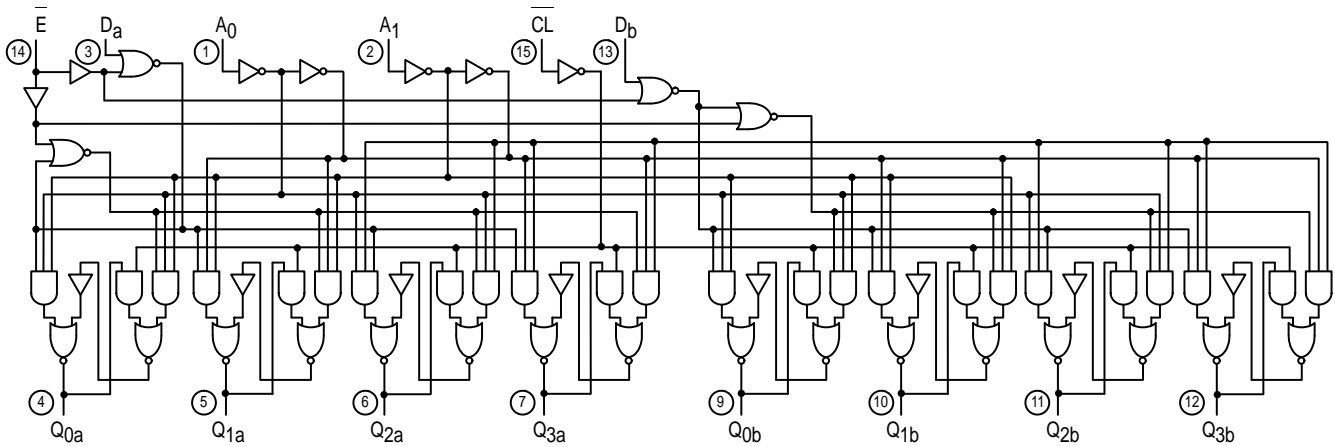
	HIGH	LOW
$A_0, A_1$	0.5 U.L.	0.25 U.L.
$\bar{D}_a, \bar{D}_b$	0.5 U.L.	0.25 U.L.
$\bar{E}$	1.0 U.L.	0.5 U.L.
$\bar{CL}$	0.5 U.L.	0.25 U.L.
$Q_{0a}-Q_{3a}$ $Q_{0b}-Q_{3b}$	10 U.L.	5 (2.5) U.L.

### LOGIC SYMBOL



# SN54/74LS256

## LOGIC DIAGRAM



V<sub>CC</sub> = PIN 16  
 GND = PIN 8  
 ○ = PIN NUMBERS

## TRUTH TABLE

CL	E	D	A <sub>0</sub>	A <sub>1</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	MODE
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Memory
H	L	L	L	L	L	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Addressable Latch
H	L	H	L	L	H	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Q <sub>N-1</sub>	
H	L	L	H	L	Q <sub>N-1</sub>	L	Q <sub>N-1</sub>	Q <sub>N-1</sub>	
H	L	H	H	L	Q <sub>N-1</sub>	H	Q <sub>N-1</sub>	Q <sub>N-1</sub>	
H	L	L	L	H	Q <sub>N-1</sub>	Q <sub>N-1</sub>	L	Q <sub>N-1</sub>	
H	L	H	L	H	Q <sub>N-1</sub>	Q <sub>N-1</sub>	H	Q <sub>N-1</sub>	
H	L	L	H	H	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Q <sub>N-1</sub>	L	
H	L	H	H	H	Q <sub>N-1</sub>	Q <sub>N-1</sub>	Q <sub>N-1</sub>	H	

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

## MODE SELECTION

E	CL	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4-Channel Demultiplexer
H	L	Clear

# SN54/74LS256

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54, 74	2.4	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current Others E Input			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
	Others E Input			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current Others E Input			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			30	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

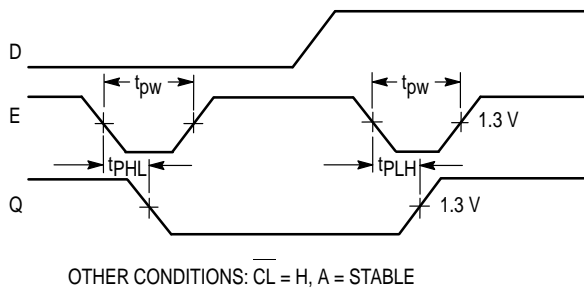
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		20 16	27 24	ns ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	30 20	ns ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		20 14	30 24	ns ns	
t <sub>PHL</sub>	Turn-On Delay, Clear to Output		12	23	ns	

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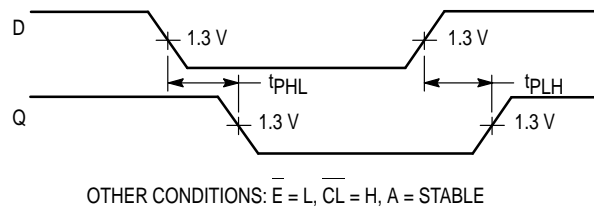
## AC SET-UP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_s$	Data Setup Time	20			ns	Figures 4 & 6 $V_{CC} = 5.0\text{ V}$
$t_s$	Address Setup Time	0			ns	
$t_h$	Data Hold Time	0			ns	
$t_h$	Address Hold Time	15			ns	
$t_W$	Enable Pulse Width	15			ns	

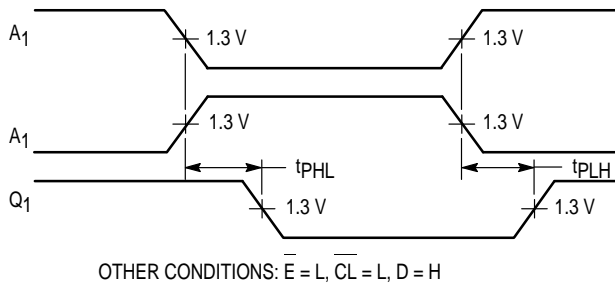
### AC WAVEFORMS



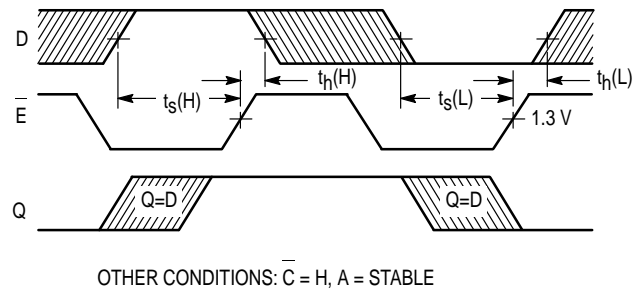
**Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width**



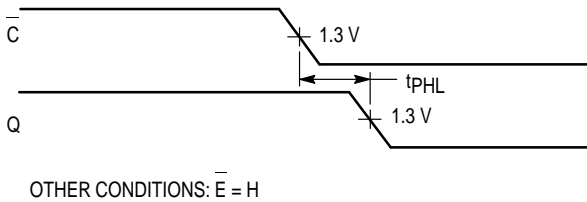
**Figure 2. Turn-on and Turn-off Delays, Data to Output**



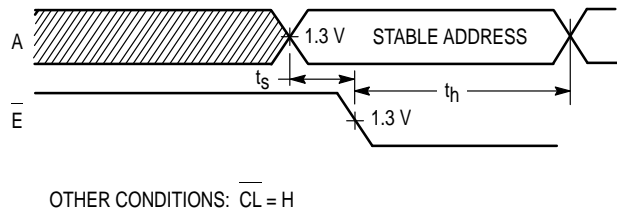
**Figure 3. Turn-on and Turn-off Delays, Address to Output**



**Figure 4. Setup and Hold Time, Data to Enable**



**Figure 5. Turn-on Delay, Clear to Output**



**Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)**

#### NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.