DUAL J-K FLIP-FLOP

MTTL III MC3100/3000 series

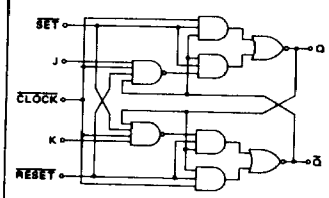
# MC3161F • MC3061F
# MC3161L • MC3061L,P

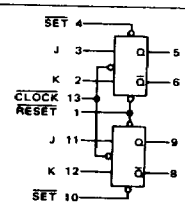
This dual JK flip-flop triggers on the negative edge of clock. Each flip-flop is provided with a separate direct $\overline{SET}$ input in addition to the common direct $\overline{RESET}$ input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the $\overline{SET}$ input. In addition, both flip-flops may be reset simultaneously by using the common $\overline{RESET}$ in a similar manner.

## LOGIC DIAGRAM

1/2 OF DEVICE SHOWN,
$\overline{RESET}$ AND $\overline{CLOCK}$ COMMON TO BOTH




Input Loading Factors:
$\overline{SET}$ = 1.75
$\overline{RESET}$, $\overline{CLOCK}$ = 3.7
J, K = 0.75

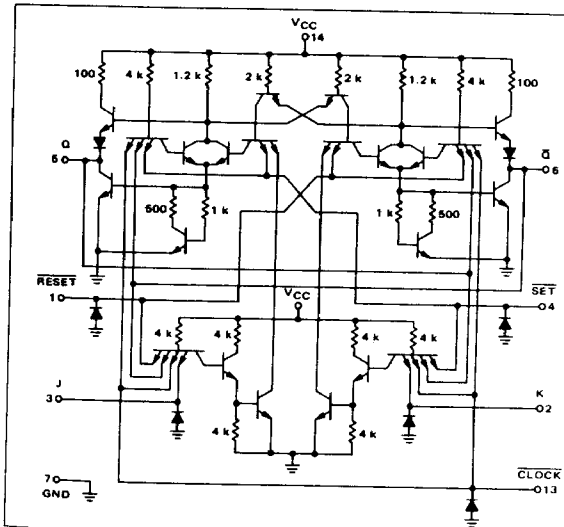
Output Loading Factor = 10

## J-K TRUTH TABLE

| J | K | $Q^n$ | $Q^{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Typical Characteristics
($V_{CC}$ = 5.0 V; $T_A$ = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz typ
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
$t_{pd-}$ = 12 ns
$t_{pd+}$ = 12 ns




1/2 OF CIRCUIT
SHOWN ($\overline{RESET}$ AND $\overline{CLOCK}$
COMMON TO BOTH)

See General Information section for packaging.

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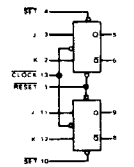
## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop plus the inputs common to both flip-flops. To complete testing, sequence through the remaining inputs in the same manner.




| | @ Test Temperature | TEST CURRENT/VOLTAGE VALUES mA $I_{OL}$ | $I_{OH}$ | $I_{in}$ | $I_D$ | Volts $V_{IL}$ | $V_{IH}$ | $V_F$ | $V_R$ | $V_{RH}$ | $V_{max}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MC3161 | −55°C | 2.0 | -2.0 | - | - | 1.1 | 2.0 | 0.4 | 2.4 | 4.0 | - | 5.0 | 4.5 | 5.5 |
| | +25°C | 2.0 | -2.0 | 1.0 | -10 | 1.1 | 1.8 | 0.4 | 2.4 | 4.0 | 7.0 | 5.0 | 4.5 | 5.5 |
| | +125°C | 2.0 | -2.0 | - | - | 0.8 | 1.8 | 0.4 | 2.4 | 4.0 | - | 5.0 | 4.5 | 5.5 |
| MC3061 | 0°C | 2.0 | -2.0 | - | - | 1.1 | 2.0 | 0.4 | 2.5 | 4.0 | - | 5.0 | 4.75 | 5.25 |
| | +25°C | 2.0 | -2.0 | 1.0 | -10 | 1.1 | 1.8 | 0.4 | 2.5 | 4.0 | 7.0 | 5.0 | 4.75 | 5.25 |
| | +75°C | 2.0 | -2.0 | - | - | 0.9 | 1.8 | 0.4 | 2.5 | 4.0 | - | 5.0 | 4.75 | 5.25 |

| Characteristic | Symbol | Pin Under Test | MC3161 Test Limits −55°C Min | −55°C Max | +25°C Min | +25°C Max | +125°C Min | +125°C Max | MC3061 Test Limits 0°C Min | 0°C Max | +25°C Min | +25°C Max | +75°C Min | +75°C Max | Unit | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL}$ | $I_{OH}$ | $I_{in}$ | $I_D$ | $V_{IL}$ | $V_{IH}$ | $V_F$ | $V_R$ | $V_{RH}$ | $V_{max}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ | $P_1$* | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Forward Current | $I_{FJ}$ | 3 | - | +1.5 | - | -1.5 | - | -1.5 | - | -1.5 | - | -1.5 | - | -1.5 | mAdc | - | - | - | - | - | - | 3 | - | 1,4,13 | - | - | - | 14 | 1 | 2,7,10 |
| | $I_{FK}$ | 2 | - | -1.5 | - | -1.5 | - | -1.5 | - | -1.5 | - | -1.5 | - | -1.5 | mAdc | - | - | - | - | - | - | 2 | - | 1,4,13 | - | - | - | 14 | 4 | 3,7,10 |
| | $I_{F\overline{R}}$ | 1 | - | -6.4 | - | -6.4 | - | -6.4 | - | -6.4 | - | -6.4 | - | -6.4 | mAdc | - | - | - | - | - | - | 1,5,9 | - | 3,4,10,13 | - | - | - | 14 | - | 2,7 |
| | $I_{F\overline{S}}$ | 4 | - | -4.0 | - | -4.0 | - | -4.0 | - | -4.0 | - | -4.0 | - | -4.0 | mAdc | - | - | - | - | - | - | 4,6 | - | 1,2,10,13 | - | - | - | 14 | - | 3,7 |
| | $I_{F\overline{C}}$ | 13 | - | -9.2 | - | -9.2 | - | -9.2 | - | -9.2 | - | -9.2 | - | -9.2 | mAdc | - | - | - | - | - | - | 6,8,13 | - | 1,2,3,11,12 | - | - | - | 14 | 4,10 | 7 |
| Leakage Current | $I_{RJ}$ | 3 | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | μAdc | - | - | - | - | - | - | - | 3 | 2,4 | - | - | - | 14 | - | 1,7,10,13 |
| | $I_{RK}$ | 2 | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | μAdc | - | - | - | - | - | - | - | 2 | 1,3 | - | - | - | 14 | - | 4,7,10,13 |
| | $I_{R\overline{R}}$ | 1 | - | 200 | - | 200 | - | 200 | - | 200 | - | 200 | - | 200 | μAdc | - | - | - | - | - | - | - | 1 | 2 | - | - | - | 14 | 1 | 3,4,7,11,13 |
| | $I_{R\overline{S}}$ | 4 | - | 150 | - | 150 | - | 150 | - | 150 | - | 150 | - | 150 | μAdc | - | - | - | - | - | - | - | 4 | 3 | - | - | - | 14 | 4 | 1,2,7,10,13 |
| | $I_{R\overline{C}}$ | 13 | - | 300 | - | 300 | - | 300 | - | 300 | - | 300 | - | 300 | μAdc | - | - | - | - | - | - | - | 13 | - | - | - | - | 14 | - | 1,2,3,4,7,10,11,12 |
| Breakdown Voltage | $BV_{in}$ | 3 | - | - | 5.5 | - | - | - | - | - | 5.5 | - | - | - | Vdc | - | - | 3 | - | - | - | - | - | 2,4 | - | - | - | 14 | - | 1,7,10,13 |
| | | 2 | - | - | ↓ | - | - | - | - | - | ↓ | - | - | - | ↓ | - | - | 2 | - | - | - | - | - | 1,3 | - | - | - | ↓ | - | 4,7,10,13 |
| | | 1 | - | - | | - | - | - | - | - | | - | - | - | | - | - | 1 | - | - | - | - | - | 2 | - | - | - | | 1 | 3,4,7,11,13 |
| | | 4 | - | - | | - | - | - | - | - | | - | - | - | | - | - | 4 | - | - | - | - | - | 3 | - | - | - | | 4 | 1,2,7,10,13 |
| | | 13 | - | - | | - | - | - | - | - | | - | - | - | | - | - | 13 | - | - | - | - | - | - | - | - | - | | - | 1,2,3,4,7,10,11,12 |
| Clamp Voltage | $V_D$ | 3 | - | - | - | -1.5 | - | - | - | - | - | -1.5 | - | - | Vdc | - | - | - | 3 | - | - | - | - | - | - | - | - | 14 | - | - | 7,10 |
| | | 2 | - | - | - | ↓ | - | - | - | - | - | ↓ | - | - | ↓ | - | - | - | 2 | - | - | - | - | - | - | - | - | ↓ | - | - | ↓ |
| | | 1 | - | - | - | | - | - | - | - | - | | - | - | | - | - | - | 1 | - | - | - | - | - | - | - | - | | - | - | |
| | | 4 | - | - | - | | - | - | - | - | - | | - | - | | - | - | - | 4 | - | - | - | - | - | - | - | - | | - | - | |
| | | 13 | - | - | - | | - | - | - | - | - | | - | - | | - | - | - | 13 | - | - | - | - | - | - | - | - | | - | - | |
| **Output** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Output Voltage | $V_{OL}$ | 5 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | Vdc | 5 | - | - | - | 1 | 4 | - | - | - | - | - | 14 | - | 1 | 7,10 |
| | | 6 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | Vdc | 6 | - | - | - | 4 | 1 | - | - | - | - | - | 14 | - | 4 | 7,10 |
| | $V_{OH}$ | 5 | 2.4 | - | 2.4 | - | 2.4 | - | 2.5 | - | 2.5 | - | 2.5 | - | Vdc | - | 5 | - | - | 4 | 1 | - | - | - | - | - | 14 | - | 4 | 7,10 |
| | | 6 | 2.4 | - | 2.4 | - | 2.4 | - | 2.5 | - | 2.5 | - | 2.5 | - | Vdc | - | 6 | - | - | 1 | 4 | - | - | - | - | - | 14 | - | 1 | 7,10 |
| Short-Circuit Current | $I_{SC}$ | 5 | -20 | -65 | -20 | -65 | -20 | -65 | -20 | -65 | -20 | -65 | -20 | -65 | mAdc | - | - | - | - | - | - | - | - | - | - | 14 | - | - | - | 4,5,7,10 |
| | | 6 | -20 | -65 | -20 | -65 | -20 | -65 | -20 | -65 | -20 | -65 | -20 | -65 | mAdc | - | - | - | - | - | - | - | - | - | - | 14 | - | - | - | 1,6,7,10 |
| **Power Requirements (Total Device)** Maximum Power Supply Current | $I_{max}$ | 14 | - | - | - | 42 | - | - | - | - | - | 42 | - | - | mAdc | - | - | - | - | - | - | - | - | - | 14 | - | - | - | - | 4,7,10 |
| Power Supply Drain | $I_{PD}$ | 14 | - | 30 | - | 30 | - | 30 | - | 30 | - | 30 | - | 30 | mAdc | - | - | - | - | - | - | - | - | - | - | 14 | - | - | - | 1,7 |

*Momentarily ground pin prior to taking measurement. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

## OPERATING CHARACTERISTICS

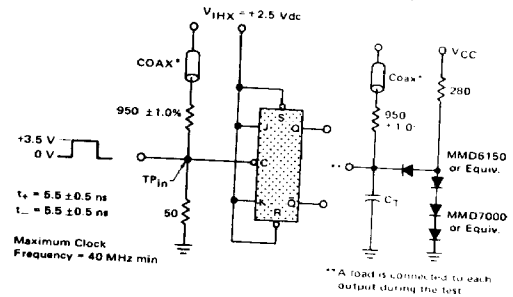
High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The direct $\overline{SET}$ (individual) inputs and $\overline{RESET}$ (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{SET}$ input or reset to the Q = 0 state by applying a low level to the $\overline{RESET}$ input. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering. The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

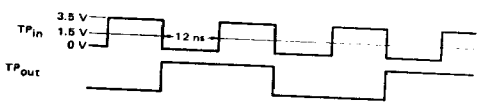
### MAXIMUM CLOCK FREQUENCY TEST CIRCUIT




*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T$ = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

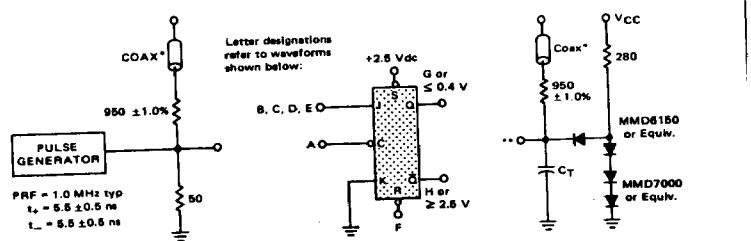
### VOLTAGE WAVEFORMS AND DEFINITIONS



## OPERATING CHARACTERISTICS (continued)

### SWITCHING TIME TEST CIRCUIT

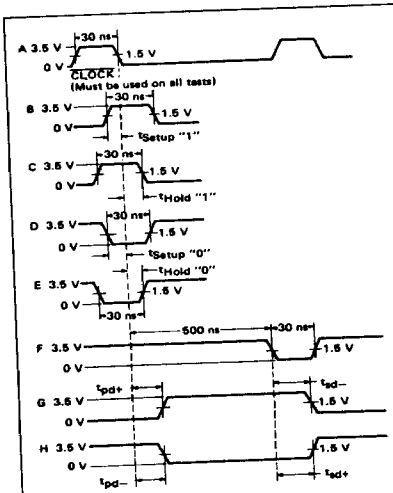
(For J Inputs and $\overline{\text{RESET}}$ Input; to test other inputs, refer to Test Procedures Chart)




*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedence constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T$ = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

### VOLTAGE WAVEFORMS AND DEFINITIONS




### TEST PROCEDURES CHART

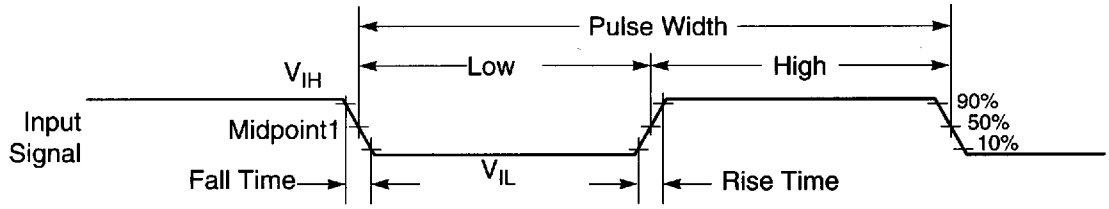
| TEST | INPUT J* | INPUT SET* | INPUT $\overline{\text{RESET}}$* | INPUT K* | INPUT Q* | INPUT Q̄* | LIMITS (ns) Max |
|---|---|---|---|---|---|---|---|
| $t_{Setup}$ "1" J | B | 2.5 V | F | Gnd | G | H | 10 |
| $t_{Hold}$ "1" J | C | 2.5 V | F | Gnd | G | H | 0** |
| $t_{Setup}$ "0" J | D | 2.5 V | F | Gnd | ≤0.4 V | ≥2.5 V | 10 |
| $t_{Hold}$ "0" J | E | 2.5 V | F | Gnd | ≤0.4 V | ≥2.5 V | 0** |
| $t_{Setup}$ "1" K | Gnd | F | 2.5 V | E | H | G | 10 |
| $t_{Hold}$ "1" K | Gnd | F | 2.5 V | C | H | G | 0** |
| $t_{Setup}$ "0" K | Gnd | F | 2.5 V | D | ≥2.5 V | ≤0.4 V | 10 |
| $t_{Hold}$ "0" K | Gnd | F | 2.5 V | E | ≥2.5 V | ≤0.4 V | 0** |
| $t_{pd+}$ | Delay from CLOCK to Q during $t_{Setup}$ "1" J test.<br>Delay from CLOCK to Q̄ during $t_{Setup}$ "1" K test. | | | | | | 10 |
| $t_{pd-}$ | Delay from CLOCK to Q̄ during $t_{Setup}$ "1" J test.<br>Delay from CLOCK to Q during $t_{Setup}$ "1" K test. | | | | | | 10 |
| $t_{sd+}$ | Delay from SET to Q during $t_{Setup}$ "1" K test.<br>Delay from RESET to Q̄ during $t_{Setup}$ "1" J test. | | | | | | 10 |
| $t_{sd-}$ | Delay from SET to Q̄ during $t_{Setup}$ "1" K test.<br>Delay from RESET to Q during $t_{Setup}$ "1" J test. | | | | | | 10 |

*Letters shown in these columns refer to waveforms shown at the left.

**$t_{Hold}$ is typically a negative number.

# AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a $V_{IL}$ maximum of 0.5 V and a $V_{IH}$ minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine $V_{OL}$ and $V_{OH}$ reference levels set at 0.8 V and 2.0 V, respectively.




Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

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**Figure 2-1** Signal Measurement Reference