

**SPEED/PACKAGE AVAILABILITY**

54 F,W      74 A,F

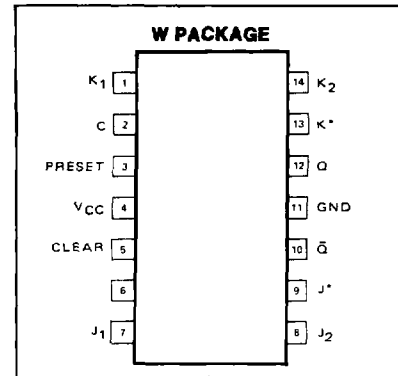
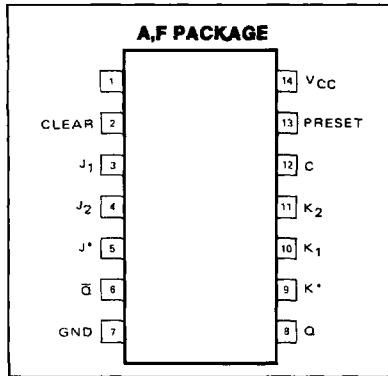
**PIN CONFIGURATION**

**TRUTH TABLE**

**LOGIC**

J <sub>n</sub>	K <sub>n</sub>	Q <sub>n+1</sub>	PRESET	CLEAR	Q
0	0	Q <sub>n</sub>	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\bar{Q}_n$	1	1	0

J = J<sub>1</sub>J<sub>2</sub>J<sub>3</sub>...    K = K<sub>1</sub>K<sub>2</sub>K<sub>3</sub>...  
 n is time prior to clock  
 n+1 is time following clock  
 † both outputs in 0 state



**SWITCHING CHARACTERISTICS** V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

TEST CONDITIONS			54/74			UNIT
			C <sub>L</sub> = 15pF R <sub>L</sub> = 400Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	
f <sub>Clock</sub> Clock frequency			15	35		MHz
t <sub>Setup</sub> Input setup time				10	20	ns
t <sub>Hold</sub> Input hold time				0	5	ns
Propagation delay time						
t <sub>PLH</sub> Low-to-high	Clear, Preset				50	ns
t <sub>PHL</sub> High-to-low					50	ns
t <sub>PLH</sub> Low-to-high	Clock		10	27	50	ns
t <sub>PHL</sub> High-to-low			10	18	50	ns

Load circuit and typical waveforms are shown at the front of section.

**SPEED/PACKAGE AVAILABILITY**

54H F,W      74H A,F

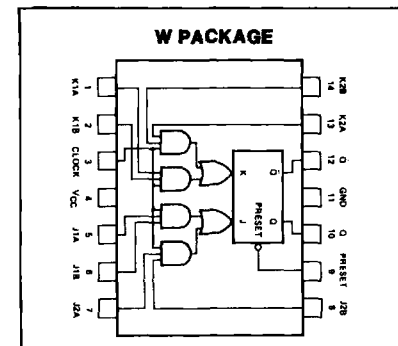
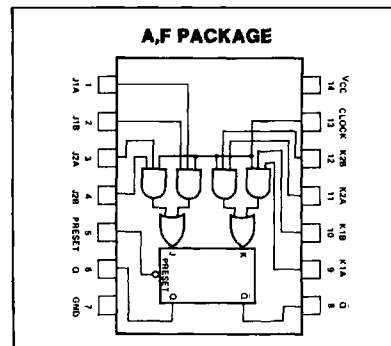
**PIN CONFIGURATION**

**TRUTH TABLE**

t <sub>n</sub>		t <sub>n+1</sub>
J	K	Q
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	$\bar{Q}_n$

**NOTES:**

- J = (J1A-J1B) + (J2A-J2B)
- K = (K1A-K1B) + (K2A-K2B)
- t<sub>n</sub> = bit time before clock pulse.
- t<sub>n+1</sub> = bit time after clock pulse.



**SWITCHING CHARACTERISTICS**  $V_{CC} = 5V, T_A = 25^\circ C$

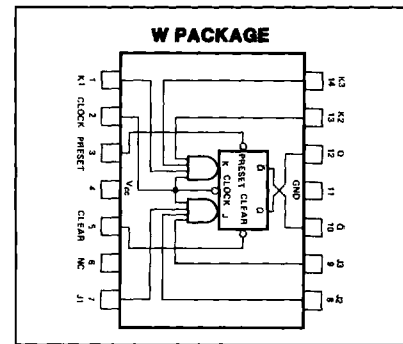
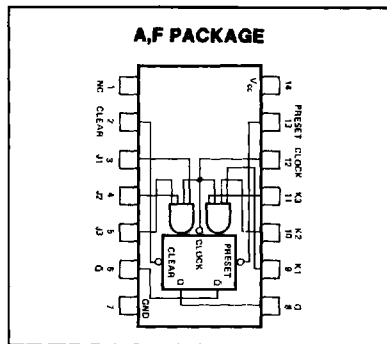
TEST CONDITIONS			54/74H			UNIT
			$C_L = 15pF$ $R_L = 280\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	
$f_{Clock}$ Clock frequency			25	30		MHz
Propagation delay time						
$t_{PLH}$ Low-to-high	Preset			6	13	ns
$t_{PHL}$ High-to-low				12	24	
$t_{PLH}$ Low-to-high	Clock		6	14	21	ns
$t_{PHL}$ High-to-low			10	22	27	

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**PIN CONFIGURATION**



**TRUTH TABLE**

$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES:  
1. J = J1 · J2 · J3      3.  $t_n$  = bit time before clock pulse.  
2. K = K1 · K2 · K3    4.  $t_{n+1}$  = bit time after clock pulse.  
5. NC = no internal connection.

**SWITCHING CHARACTERISTICS**  $V_{CC} = 5V, T_A = 25^\circ C$

TEST CONDITIONS			54/74			54/74H			UNIT
			$C_L = 15pF$ $R_L = 400\Omega$			$C_L = 25pF$ $R_L = 280\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{Clock}$ Clock frequency			15	20		25	30		MHz
Propagation delay time									
$t_{w(Clock)}$ Width of clock input pulse									
		Clock high	20			12			ns
		Clock low	47			28			
$t_{w(Clear)}$ Width of clear input pulse			25			16			ns
$t_{Setup}$ Input setup time			0↑			0↑			ns
$t_{Hold}$ Input hold time			0↓			0↓			ns
Propagation delay time									
$t_{PLH}$ Low-to-high	Clear			16	25	6	13		ns
$t_{PHL}$ High-to-low				25	40	12	24		
$t_{PLH}$ Low-to-high	Clock		10	16	25	16	21		ns
$t_{PHL}$ High-to-low			10	25	40	22	27		

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