National Semiconductor

MM54HCT273/MM74HCT273
Octal D Flip-Flop with Clear

General Description

The MM54HCT273/MM74HCT273 utilizes advanced silicon-gate CMOS technology. It has an input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These positive edge-triggered flip-flops have a common clock and clear-independent Q outputs. Data on a D input, having the specified set-up and hold time, is transferred to the corresponding Q output on the positive-going transition of the clock pulse. The asynchronous clear forces all outputs low when it is low.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

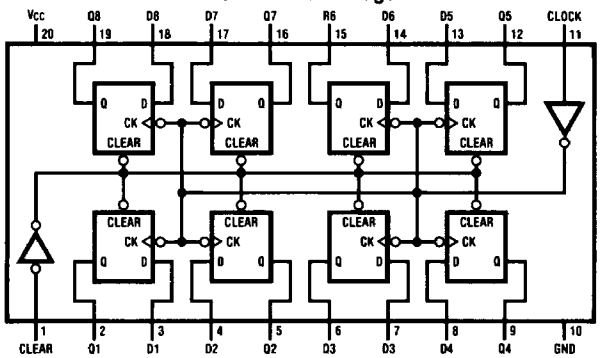
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. These parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



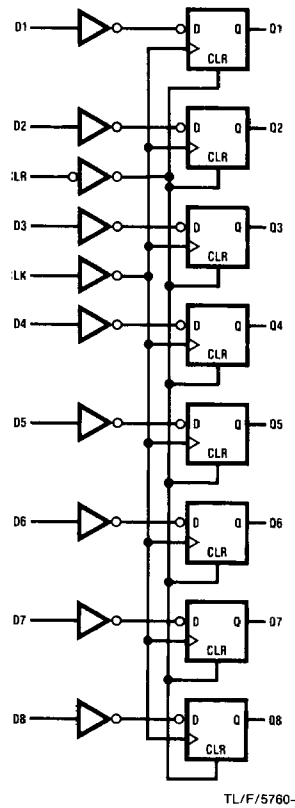
TL/F/5760–1

Top View

Order Number MM54HCT273* or MM74HCT273*

*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



TL/F/5760–2

Truth Table (Each Flip-Flop)

Inputs			Outputs
Clear	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = high level (steady-state)

L = low level (steady-state)

X = don't care

↑ = transition from low to high level

Q0 = the level of Q before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to + 150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Minimum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.6	0.8	0.9	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		68	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		21	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−1	5	ns
t_S	Minimum Set-Up Time D to Clock		6	20	ns
t_H	Minimum Hold Time Clock to D		−3	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics V_{CC} = 5.0V ± 10%, C_L = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C		54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		68	27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		22	37	46	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		25	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock		−1	5	6	7	ns
t_S	Minimum Set-Up Time D to Clock		6	20	25	30	ns
t_H	Minimum Hold Time Clock to D		−3	5	5	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	25	30	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		11	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)	50				pF
C_{IN}	Maximum Input Capacitance		6	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC}^2 f + I_{CC}$.