

"OR" J-K FLIP-FLOP

MTTL II MC2100/2000 series

MC2126 • MC2176
MC2026 • MC2076

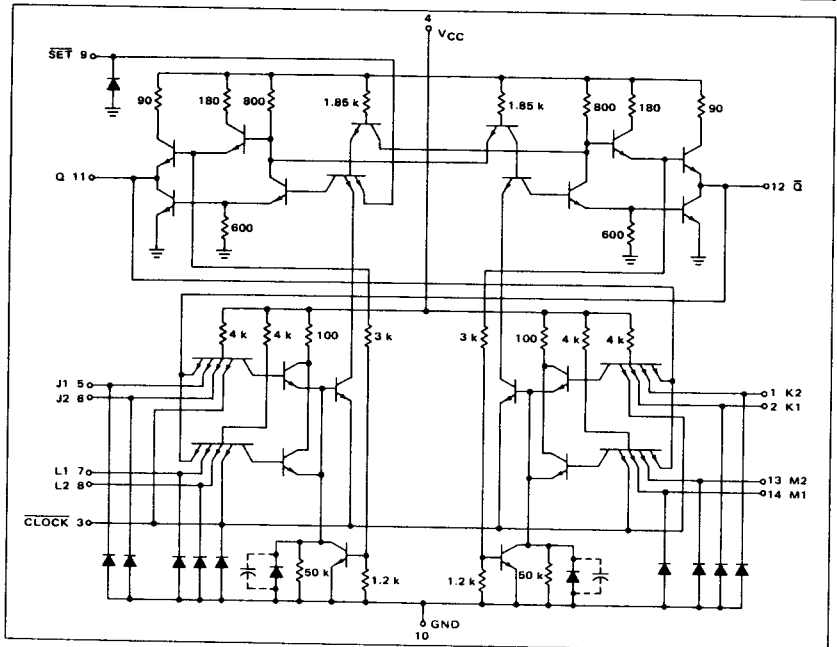
The MC2026, MC2076, MC2126, and MC2176 are clocked flip-flops that toggle at 50 MHz, trigger on the negative edge of the clock input pulse, and perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and L inputs are ORed together and the K and M inputs are ORed together. A direct SET input is also available. These devices are pin compatible with the MC2110 series of devices. Electrical differences include the input loading factor for the SET input, which is approximately twice that of the MC2110 series.

Information is changed on the clocked inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is transferred into a temporary memory through the AND-OR input gating when the clock goes to the high state. When the clock returns low, the information in the temporary memory is transferred to the bistable section and the Q and \bar{Q} outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

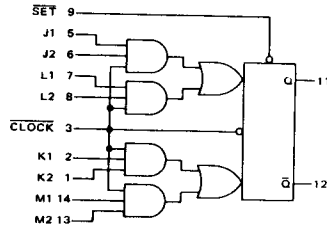
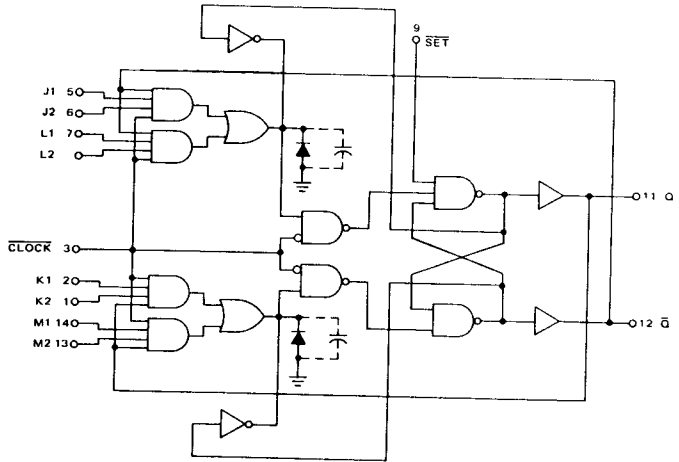
Each flip-flop can be set directly by applying a low state to the direct SET input. Since these flip-flops are charge-storage devices, there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it useful for shift right/shift left registers and for up/down counters.

TYPE NO.	INPUT LOADING FACTOR (i _p)						OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
	CLOCK	SET	J, K, L, M	CLOCK	SET	J, K, L, M			
MC2126 MC2176	2.0	1.2	0.67	(-2.66 mA)	(-2.4 mA)	(-1.33 mA)	11 MC2100 series Gates 6 MC2100 series Gates	(22.0 mA) (12.0 mA)	-55°C to +125°C
MC2026 MC2076	2.0	1.2	0.67	(-3.32 mA)	(-2.8 mA)	(-1.66 mA)	9 MC2000 series Gates 5 MC2000 series Gates	(22.5 mA) (12.5 mA)	0°C to +75°C



LOGIC DIAGRAM



J	L	K	M	Q _n	Q _{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care Where J = J1 • J2
 L = L1 • L2
 K = K1 • K2
 M = M1 • M2

Total Power Dissipation - 60 mW typ/pkg
 Switching Times
 t_{pd} - 11 ns typ
 t_{pd1} - 9.0 ns typ
 Operating Frequency - 70 MHz typ

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 10 ns.

The application of a "0" state to the SET will cause Q to go to the "1" state. The clock must be in the low state when this function is performed. Since there is almost no post time associated with these devices, the direct input can be applied 15 ns after the clock signal has fallen.

Data at the clocked inputs must be present before the clock goes to the high state. If the information on the clocked inputs is changed while the clock is in the high state, the flip-flop will require typically $1.0 \mu\text{s}$ to recognize a "1" state to "0" state change. The flip-flop typically requires 10 ns to recognize a "0" state to "1" state change.

By using an internally cross-coupled network and buffered outputs, the propagation delays (t_{pd-} and t_{pd+}) are nearly symmetrical.

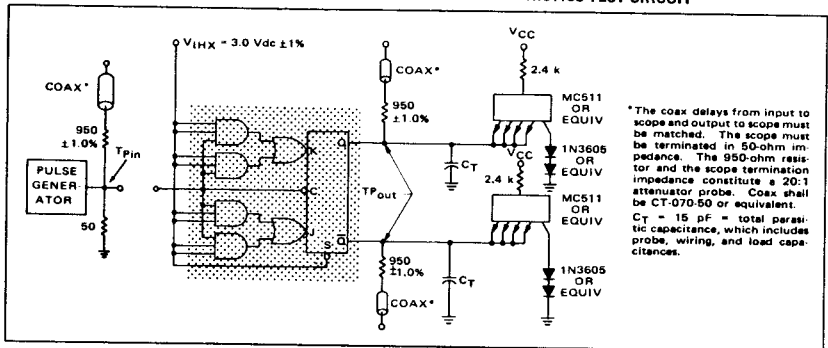
The outputs are capable of driving high capacitive loads without degrading the frequency of operation.

Negative edge triggering - When the clock goes from the high state to the low state, the information in the temporary storage section is transferred to the bistable network and the data appears at the Q and \bar{Q} outputs. While the clock is in a low state, the clocked terminals are inhibited.

Unused J, K, L, and M inputs should be tied to the clock or to a voltage between 2.0 and 5.0 Vdc. Other unused inputs should be tied to a voltage between 2.0 and 5.0 Vdc.

The maximum allowable clock skew time is 9.0 ns. This is the total of the minimum time to recognize a "0" to "1" logic state change (4.0 ns) and the minimum propagation delay (5.0 ns).

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



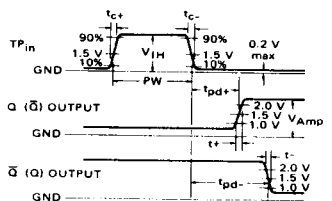
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{pd+}	V	-	15	ns
Delay Time On	t_{pd-}	V	-	15	ns
Rise Time	t_r	V	-	4.0	ns
Fall Time	t_f	V	-	2.5	ns
Amplitude	V_{Amp}	V	3.0	-	Volt

WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	50 MHz max	W
Pulse Width	PW	10 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	100 ns max	Z

VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	V	W	X	Y	Z	UNIT
PRF	5.0	50	5.0	5.0	1.0	MHz
PW	10	10	10	10	200	ns
t_r	≤ 5.0	≤ 2.0	≤ 5.0	≤ 5.0	≤ 50	ns
t_f	≤ 5.0	≤ 2.0	≤ 5.0	≤ 5.0	≤ 100	ns
V_{IH}	3.0	3.0	3.0	2.4	3.0	Volt

FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

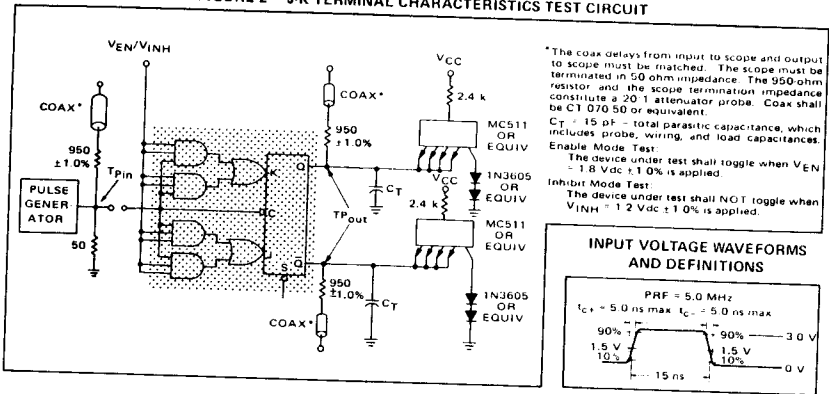
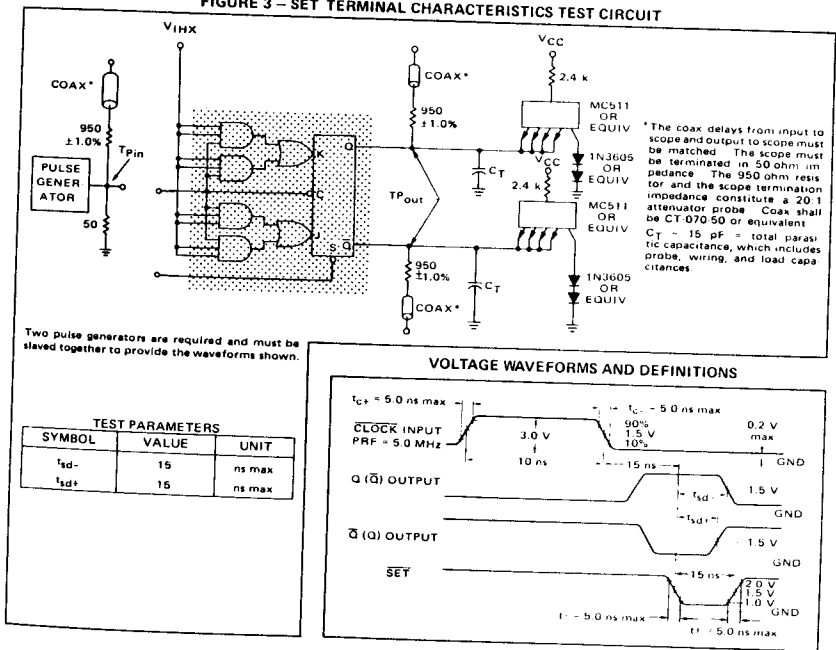


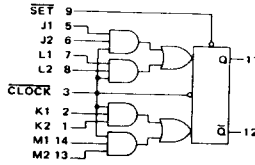
FIGURE 3 - SET TERMINAL CHARACTERISTICS TEST CIRCUIT



MC2126, MC2176/MC2026, MC2076 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, as well as the SET and CLOCK inputs. The remaining J, K, L, and M inputs are tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC2126, MC2176 Test Limits						MC2026, MC2076 Test Limits						Unit
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		
Input Forward Current	I_F	J	5	-	-1.33	-1.33	-1.33	-	-1.66	-1.66	-1.66	-	-1.66	-1.66	mA
		K	1	-	-1.33	-1.33	-1.33	-	-1.66	-1.66	-1.66	-	-1.66	-1.66	
		Set	9	-	-2.4	-2.4	-2.4	-	-2.8	-2.8	-2.8	-	-2.8	-2.8	
		Clock	3	-	-2.66	-2.66	-2.66	-	-3.32	-3.32	-3.32	-	-3.32	-3.32	
Leakage Current	I_R	J	5	-	70	70	70	-	70	70	70	-	70	70	μ A
		K	1	-	70	70	70	-	70	70	70	-	70	70	
		Set	9	-	280	280	280	-	280	280	280	-	280	280	
		Clock	3	-	280	280	280	-	280	280	280	-	280	280	
Inverse Beta Current	I_L	J	5	-	70	70	70	-	70	70	70	-	70	70	μ A
		K	1	-	70	70	70	-	70	70	70	-	70	70	
		Set	9	-	280	280	280	-	280	280	280	-	280	280	
		Clock	3	-	280	280	280	-	280	280	280	-	280	280	
Breakdown Voltage	$BV_{in}^{(0)}$	J	5	5.5	-	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	Vdc	
		K	1	-	-	-	-	-	-	-	-	-	-		
		Set	9	-	-	-	-	-	-	-	-	-	-		
	$BV_{in}^{(1)}$	J	5	5.5	-	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	Vdc	
		K	1	-	-	-	-	-	-	-	-	-	-		
		Set	9	-	-	-	-	-	-	-	-	-	-		
Output Output Voltage	$V_{out}^{(0)}$	Q	11	-	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	Vdc	
		\bar{Q}	12	2.5	-	2.4	2.5	2.5	2.5	2.4	2.5	2.5	2.5		
Leakage Current	I_{OLK}	Q	11	-	1.25	1.25	1.25	1.25	1.25	1.25	1.25	1.25	1.25	mA	
		\bar{Q}	12	-	1.25	1.25	1.25	1.25	1.25	1.25	1.25	1.25	1.25		
Short-Circuit Current	I_{SC}	Q	11	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	mA	
		\bar{Q}	12	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90		
Output Voltage	V_{OL}	Q	11	-	0.40	0.40	0.45	0.45	0.40	0.40	0.40	0.40	0.45	Vdc	
		\bar{Q}	12	2.8	-	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0		
Power Requirements	I_{PD}	Prime Fan-Out	4	-	18	18	18	18	19	19	19	19	19	mA	
		Monomentarily apply -0.5 V prior to taking measurement to set flip-flop in desired state. Return pin to specified voltage or current for measurement. Release ground on pin 9 prior to taking measurement.	4	-	16	16	16	16	19	19	19	19	19		

*Prime Fan-Out.

**Monomentarily apply -0.5 V prior to taking measurement to set flip-flop in desired state.

†Monomentarily ground pin prior to taking measurement to set flip-flop in desired state. Return pin to specified voltage or current for measurement.

‡Release ground on pin 9 prior to taking measurement.

		TEST CURRENT / VOLTAGE VALUES															
		mA						Volts									
		I_{OL}		I_{OH}		I_{in}	$2I_{in}$	$4I_{in}$	V_R	V_{IN}	V_R	$V_{in,1}$	$V_{in,0}$	V_{out}	V_{CC}		
		Pr*	Std	Pr*	Std	I_{in}	$2I_{in}$	$4I_{in}$	V_R	V_{IN}	V_R	$V_{in,1}$	$V_{in,0}$	V_{out}	V_{CC}		
MC2126*, MC2176		-55°C		22.0	12.0	-2.2	-1.1	1.0	2.0	4.0	0.45	2.8	4.5	2.0	0.9	5.5	5.0
		+25°C		22.0	12.0	-2.2	-1.1	1.0	2.0	4.0	0.45	2.8	4.5	1.8	1.1	5.5	5.0
		+125°C		22.0	12.0	-2.2	-1.1	1.0	2.0	4.0	0.45	2.8	4.5	1.5	0.9	5.5	5.0
MC2026*, MC2076		0°C		22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.0	5.5	5.0
		+25°C		22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.1	5.5	5.0
		+75°C		22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.0	5.5	5.0
		TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
Characteristic	Symbol	Pin Under Test	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	$4I_{in}$	V_R	V_{IN}	V_R	$V_{in,1}$	$V_{in,0}$	V_{out}	V_{CC}	**	Grid	
Input Forward Current	J _K	5	-	-	-	-	-	-	-	1, 2, 3, 6, 7, 8, 13, 14	-	-	-	4	11	3, 10	
	K _{Set}	1	-	-	-	-	-	-	-	2, 3, 5, 6, 7, 8, 13, 14	-	-	-	-	11	1, 3, 10	
	Clock	9	-	-	-	-	-	-	3	1, 2, 3, 5, 6, 7, 8, 13, 14	-	-	-	-	11	9, 10	
Leakage Current	J _K	5	-	-	-	-	-	-	-	5	-	-	-	4	11	3, 6, 7, 8, 9, 10	
	K _{Set}	1	-	-	-	-	-	-	-	1	-	-	-	-	11	2, 3, 10, 13, 14	
	Clock	3	-	-	-	-	-	-	3	9†	-	-	-	-	11	3, 10	
Inverse Beta Current	J _L	5	-	-	-	-	-	-	-	5	-	-	-	4	11	10	
	K _{Set}	1	-	-	-	-	-	-	-	9	-	-	-	-	11	-	
	Clock	3	-	-	-	-	-	-	-	3	-	-	-	-	11	-	
Breakdown Voltage	J _{BV in-0†}	1	-	-	5	-	-	-	-	-	-	-	-	4	11	10	
	K _{Set}	9	-	-	9	-	-	-	-	-	-	-	-	-	11	-	
	Clock	3	-	-	3	-	-	-	9	-	-	-	-	-	11	-	
Output Output Voltage	J _{BV in-1†}	5	-	-	5	-	-	-	-	-	-	-	-	4	11	3, 6, 7, 8, 9, 10	
	K _{Set}	1	-	-	1	-	-	-	-	-	-	-	-	-	11	2, 3, 10, 13, 14	
	Clock	3	-	-	9†	-	3	-	-	-	-	-	-	-	11	3, 10	
Leakage Current	V _{out-0}	11	11	-	-	-	-	-	-	-	9	-	-	4	11	3, 10	
	V _{out-1}	11	-	11	-	-	-	-	-	-	-	9	-	4	11	3, 10	
	I _{OLK}	11	-	-	-	-	-	-	-	-	-	-	11	8	-	1, 2, 3, 5, 6, 7, 8, 9, 10, 13, 14	
Short-Circuit Current	I _{SC}	11	-	-	-	-	-	-	-	9	-	-	-	12	4	11	1, 2, 3, 5, 6, 7, 8, 10, 13, 14
	V _{OL}	11	11	-	-	-	-	-	-	9	-	-	-	4	11	1, 2, 3, 5, 6, 7, 8, 9, 10, 12, 13, 14	
	V _{OH}	11	-	11	-	-	-	-	9	-	-	-	-	4	11	3, 10	
Power Requirements Power Supply Drain	I _{PD}	4	-	-	-	-	-	-	-	-	-	-	-	4	-	3, 9, 10	
		4	-	-	-	-	-	-	-	-	-	-	-	4	11	3, 10	
		4	-	-	-	-	-	-	-	-	-	-	-	4	11	3, 10	

Pin-out and Package Information

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
WT	45	L13	nc	103	
X/Y	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Power Supply	Circuit Supplied
63	L8	VCCN	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			