



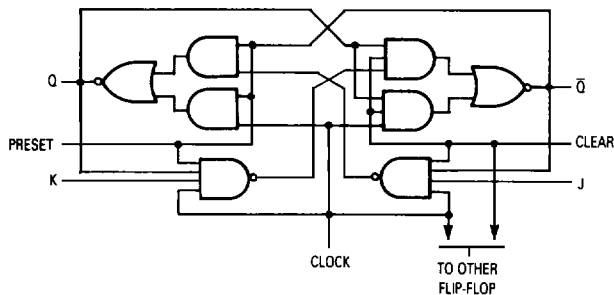
**MOTOROLA**

# Dual J-K Flip-Flop With Preset, Common Clear and Common Clock

**MIL-M-38510/30105**

The 54LS114A offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

**LOGIC DIAGRAM**  
(one half show)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

\*Both outputs will be HIGH while both  $\bar{S}_D$  and  $\bar{C}_D$  are LOW, but the output states are unpredictable if  $\bar{S}_D$  and  $\bar{C}_D$  go HIGH simultaneously.

MODE SELECT — TRUTH TABLE						
Operating Mode	Inputs				Outputs	
	$\bar{P}_R$	$\bar{C}_D$	J	K	Q	$\bar{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\bar{q}$

H, h = HIGH Voltage Level  
L, l = LOW Voltage Level  
X = Don't Care  
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

**Military 54LS114A**



**AVAILABLE AS:**

- 1) JAN: JM38510/30105BXA
- 2) SMD: \*
- 3) 883C: 54LS114A/BXAJC

**X = CASE OUTLINE AS FOLLOWS:**  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2

\*Call Factory for latest update

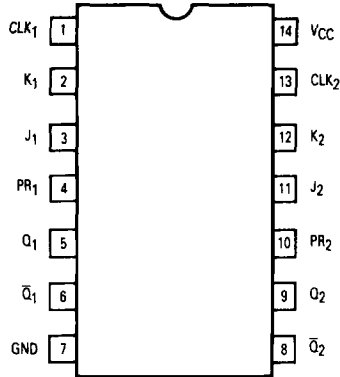
**PIN ASSIGNMENTS**

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
CLR	1	1	2	GND
K <sub>1</sub>	2	2	3	VCC
J <sub>1</sub>	3	3	4	VCC
PR <sub>1</sub>	4	4	6	GND
Q <sub>1</sub>	5	5	8	VCC
$\bar{Q}_1$	6	6	9	VCC
GND	7	7	10	GND
$\bar{Q}_2$	8	8	12	VCC
Q <sub>2</sub>	9	9	13	VCC
PR <sub>2</sub>	10	10	14	GND
J <sub>2</sub>	11	11	16	VCC
K <sub>2</sub>	12	12	18	VCC
CLK	13	13	19	GND
VCC	14	14	20	VCC

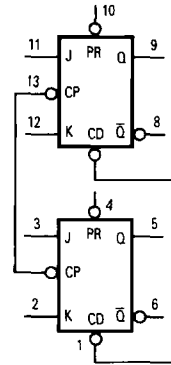
**BURN-IN CONDITIONS:**  
VCC = 5.0 V MIN/6.0 V MAX

# 54LS114A

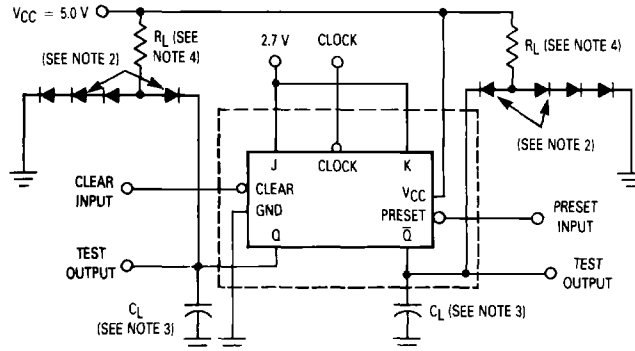
## CONNECTION DIAGRAM



## LOGIC SYMBOL

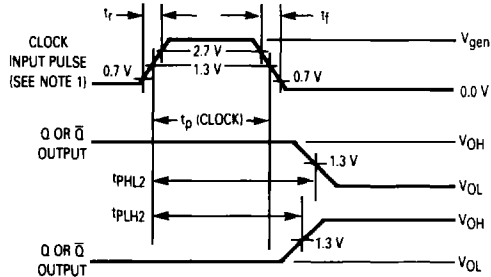


## AC TEST CIRCUIT



Synchronous Switching Test Circuit

## WAVEFORMS



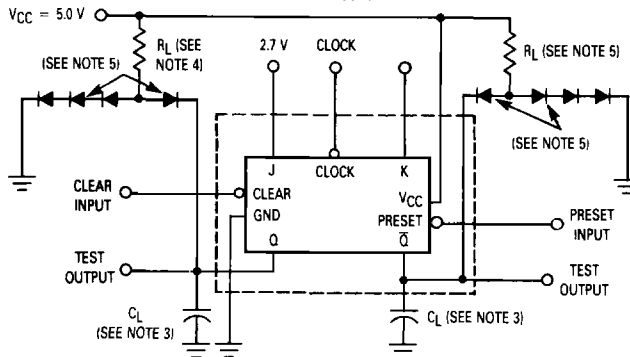
### NOTES:

1. Clock input characteristics for  $t_{PLH}$ ,  $t_{PHL}$  (clock to output):  $V_{gen} = 3.0\text{ V}$ ,  $t_r \approx 15\text{ ns}$ ,  $t_f = 6.0\text{ ns}$ ,  $t_p(\text{clock}) = 25\text{ ns}$  and  $PRR \approx 1.0\text{ MHz}$ . When testing  $t_{MAX}$  the clock input characteristics are:  $V_{gen} = 3.0\text{ V}$ ,  $t_r = t_f \approx 6.0\text{ ns}$ ,  $t_p(\text{clock}) \approx 25\text{ ns}$  and  $PRR =$  (see table 1).
2. All diodes are 1N3064, or equivalent.
3.  $C_L = 50\text{ pF} \pm 10\%$  (including jig and probe capacitance).
4.  $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .

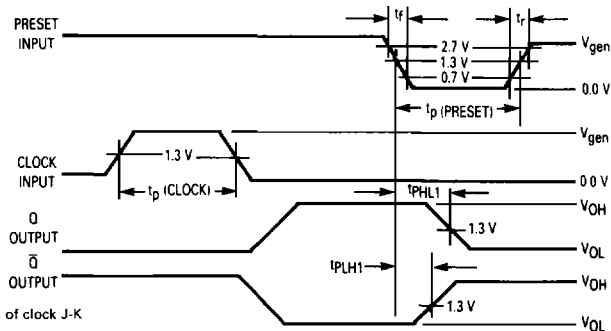
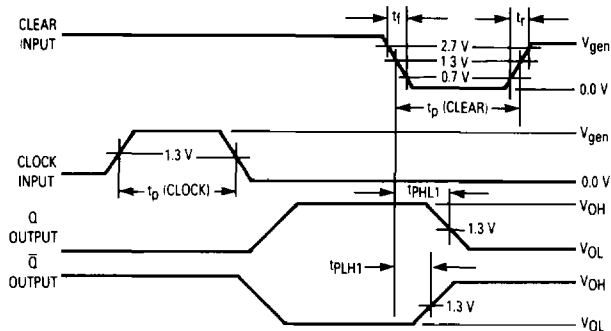
# 54LS114A

## AC TEST CIRCUIT

(CLEAR & PRESET SWITCHING TEST CIRCUIT)



## WAVEFORMS





### NOTES:

1. Clear or preset inputs dominate regardless of the state of clock J-K inputs.
2. Clear or preset input pulse characteristics:  $V_{gen} = 3.0 \text{ V}$ ,  $t_f \leq 15 \text{ ns}$ ,  $t_r \leq 6.0 \text{ ns}$ ,  $PRR \leq 1.0 \text{ MHz}$ ,  $t_p(\text{clear}) = t_p(\text{preset}) = 30 \text{ ns}$ ,  $Z_{out} \approx 50 \Omega$ .
3.  $C_L = 50 \text{ pF} \pm 10\%$  (including jig and probe capacitance).
4.  $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$ .
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table 1).
7. Clock input pulse characteristics:  $t_p(\text{clock}) \geq 25 \text{ ns}$ ,  $V_{gen} = 3.0 \text{ V}$ ,  $PRR \leq 1.0 \text{ MHz}$ .

### 54LS114A

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, V <sub>IN</sub> = 2.0 V, V <sub>IL</sub> = 0.7 V.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.7 V.
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current (J & K inputs)		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other input = GND.
I <sub>IHH</sub>	Logical "1" Input Current (J & K inputs)		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, (CLK, CLR & PR) = GND, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current (PR inputs)		60		60		60	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, (CLK, J & K) = GND, other inputs are open.
I <sub>IHH</sub>	Logical "1" Input Current (PR inputs)		300		300		300	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other inputs = GND.
I <sub>IH</sub>	Logical "1" Input Current (CLR inputs)		120		120		120	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs = GND.
I <sub>IHH</sub>	Logical "1" Input Current (CLR inputs)		600		600		600	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other inputs = GND.
I <sub>IH</sub>	Logical "1" Input Current (CLK inputs)		160		160		160	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs = GND.
I <sub>IHH</sub>	Logical "1" Input Current (CLK inputs)		800		800		800	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other inputs = GND.
I <sub>IL</sub>	Logical "0" Input Current (J & K inputs)	-0.12	-0.36	-0.12	-0.36	-0.12	-0.36	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, CLR = 4.5 V, J = GND, PR = (see note 2), other inputs are open.
I <sub>IL</sub>	Logical "0" Input Current (PR inputs)	-0.12	-0.72	-0.12	-0.72	-0.12	-0.72	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, J & K = 4.5 V, CLK = 4.5 V, other inputs are open.
I <sub>IL</sub>	Logical "0" Input Current (CLK inputs)	-0.24	-1.44	-0.24	-1.44	-0.24	-1.44	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, other inputs = 4.5 V, CLR = (see note 2).
I <sub>IL</sub>	Logical "0" Input Current (CLR inputs)	-0.12	-1.5	-0.12	-1.5	-0.12	-1.5	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, other inputs = 4.5 V.
I <sub>OS</sub>	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, CLR = GND, V <sub>OUT</sub> = 0 V, other inputs are open.
I <sub>CC</sub>	Power Supply Current		8.0		8.0		8.0	mA	V <sub>CC</sub> = 5.5 V, CLK = GND, V <sub>IN</sub> = 5.5 V, (all inputs). V <sub>IN</sub> = 5.5 V, PR = GND.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.

NOTES: 1.  0.0 V      2.  0.0 V

2.5 V min/5.5 V max      2.5 V min/5.5 V max

## 54LS114A

Functional Tests		Subgroup 7	Subgroup 8A	Subgroup 8B	per Truth Table with $V_{CC} = 4.5\text{ V}$ , $V_{INL} = 0.4\text{ V}$ , and $V_{INH} = 2.5\text{ V}$ .				
Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub> t <sub>PHL1</sub>	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0	28 20	5.0	40 35	5.0	40 35	ns ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ . $V_{CC} = 5.0\text{ V}$ , $C_L = 15\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .
t <sub>PLH1</sub> t <sub>PLH1</sub>	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0	21 20	5.0	32 27	5.0	32 27	ns ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ . $V_{CC} = 5.0\text{ V}$ , $C_L = 15\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .
t <sub>PHL2</sub>	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0	30	5.0	42	5.0	42	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .
t <sub>PLH2</sub>	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0	22	5.0	32	5.0	32	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .
f <sub>MAX</sub>	Maximum Clock Frequency	25		25		25		MHz	$V_{CC} = 5.0\text{ V}$ , $V_{IN} = 2.7\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .
f <sub>MAX</sub>	Maximum Clock Frequency	30						MHz	$V_{CC} = 5.0\text{ V}$ , $C_L = 15\text{ pF}$ , $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .

**NOTES:**

1. f<sub>MAX</sub>, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for  $C_L = 15\text{ pF}$  are guaranteed but not tested.