(Separate clock and preset inputs)

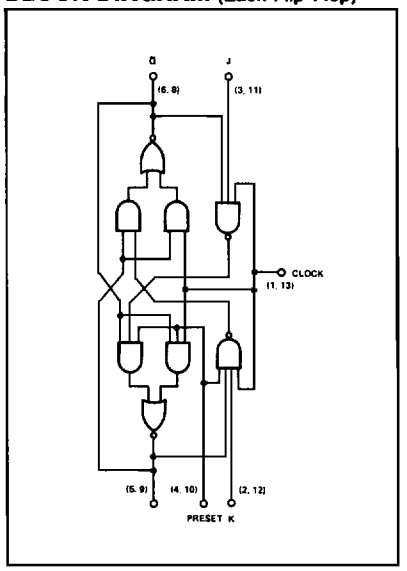
SPEED/PACKAGE AVAILABILITY

54LS F,W	74LS A,F
54S A,F,W	74S A,F

DESCRIPTION

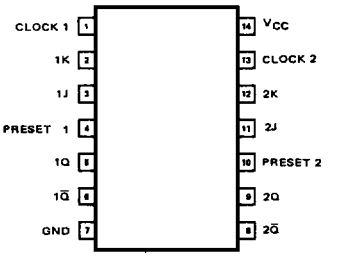
A low level at the preset input sets the Q output high regardless of the levels at the other inputs. When preset is inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION

A,F,W PACKAGE



TRUTH TABLE (Each Flip-Flop)

Inputs				Outputs	
Preset	Clock	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			30	45		80	125		MHz
$t_{w(Clock)}$ Width of Clock pulse			20						ns
Clock high						6			
Clock low						6.5			
$t_{w(Preset)}$ Width of preset pulse			25			8			ns
$t_{w(Clear)}$ Width of clear pulse			25						ns
t_{Setup} Input setup time			20↓			8			ns
t_{Hold} Input hold time			0↓			3↓			ns
Propagation delay time									
t_{PLH} Low-to-high	CLR, PRE or CLK (as appropriate)			11	20	2	4	7	ns
t_{PHL} High-to-low				15	30	2	5	7	

Load circuit and typical waveforms are shown at the front of section.

LOGIC